Hitachi LCD Controller/Driver LSI Data Book

HITACHI

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General Information

Contents

INDEX

Quick Reference Guide

Type		Column Driver							
Type Number		**HD44100H**	**HD66100**	**HD61100A**	**HD61200**	**HD61104**	**HD61104A**	**HD66106**	**HD66107T**
Power supply for internal circuits (V)		5	5	5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	6	17	17	26	28	37	37
Power Dissipation (mW)		5	5	5	5	5	5	5	5
Operating Temperature (°C)		−20 to +75*1	−20 to +75*1	−20 to +75*1	−20 to +75	−20 to +75	−20 to +75	−20 to +75	−20 to +75
Memory	ROM (bit)	–	–	–	–	–	–	–	–
	RAM (bit)	–	–	–	–	–	–	–	–
LCD Driver	Common	20	–	–	–	–	–	80	160
	Column	40 (20)	80	80	80	80	80	80	160
Instraction Set		–	–	–	–	–	–	–	–
Operation Frequency (MHz)		0.4	1	2.5	2.5	3.5	3.5	6	8
Duty		Static-1/32	Static-1/16	Static-1/100	1/32-1/128	1/64-1/200	1/64-1/240	1/100-1/480	1/100-1/480
Package		FP-60	FP-100	FP-100	FP-100	FP-100	FP-100	FP-100	192pin TAB

Type		Column Driver (RAM)			Segment Display			
Type Number		**HD44102CH**	**HD61102**	**HD61202**	**HD61602**	**HD61603**	**HD61604**	**HD61605**
Power supply for internal circuits (V)		5	5	5	3 to 5	3 to 5	3 to 5	3 to 5
Power supply for LCD Drive Circuit (V)		11	15.5	17	5	5	5	5
Power Dissipation (mW)		5	5	5	0.5	0.5	0.5	0.5
Operating Temperature (°C)		−20 to +75	−20 to +75	−20 to +75	−20 to +75*1	−20 to +75*1	−20 to +75*1	−20 to +75*1
Memory	ROM (bit)	–	–	–	–	–	–	–
	RAM (bit)	200×8	512×8	512×8	204	64	204	64
LCD Driver	Common	–	–	–	4	1	4	1
	Column	50	64	64	51	64	51	64
Instraction Set		6	7	7	4	4	4	4
Operation Frequency (MHz)		0.28	0.4	0.4	0.52	0.52	0.52	0.52
Duty		1/8,1/12, 1/16,1/24, 1/32	Static-1/64	1/48,1/64, 1/96,1/128	Static,1/2, 1/3,1/4	Static	Static,1/2, 1/3,1/4	Static
Package		FP-80	FP-100	FP-100	FP-80, FP-80A	FP-80	FP-80	FP-80

*1 -40 to +85°C (Special request). Please contact Hitachi agents.

Quick Reference Guide

Type		Common Driver				
Type Number		**HD44103CH**	**HD44105H**	**HD61103A**	**HD61203**	**HD61105**
Power supply for internal circuits (V)		5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	11	17	17	26
Power Dissipation (mW)		4.4	4.4	5	5	5
Operating Temperature (°C)		−20 to +75	−20 to +75	−20 to +75	−20 to +75	−20 to +75
Memory	ROM (bit)	–	–	–	–	–
	RAM (bit)	–	–	–	–	–
LCD Driver	Common	20	32	64	64	80
	Column	–	–	–	–	–
Instraction Set		–	–	–	–	–
Operation Frequency (MHz)		1	1	2.5	2.5	0.1
Duty		1/8,1/12, 1/16,1/24, 1/32	1/8,1/12, 1/32,1/48	Static-1/10, 1/64	1/32-1/128	1/64-1/200
Package		FP-60	FP-60	FP-100	FP-100	FP-100

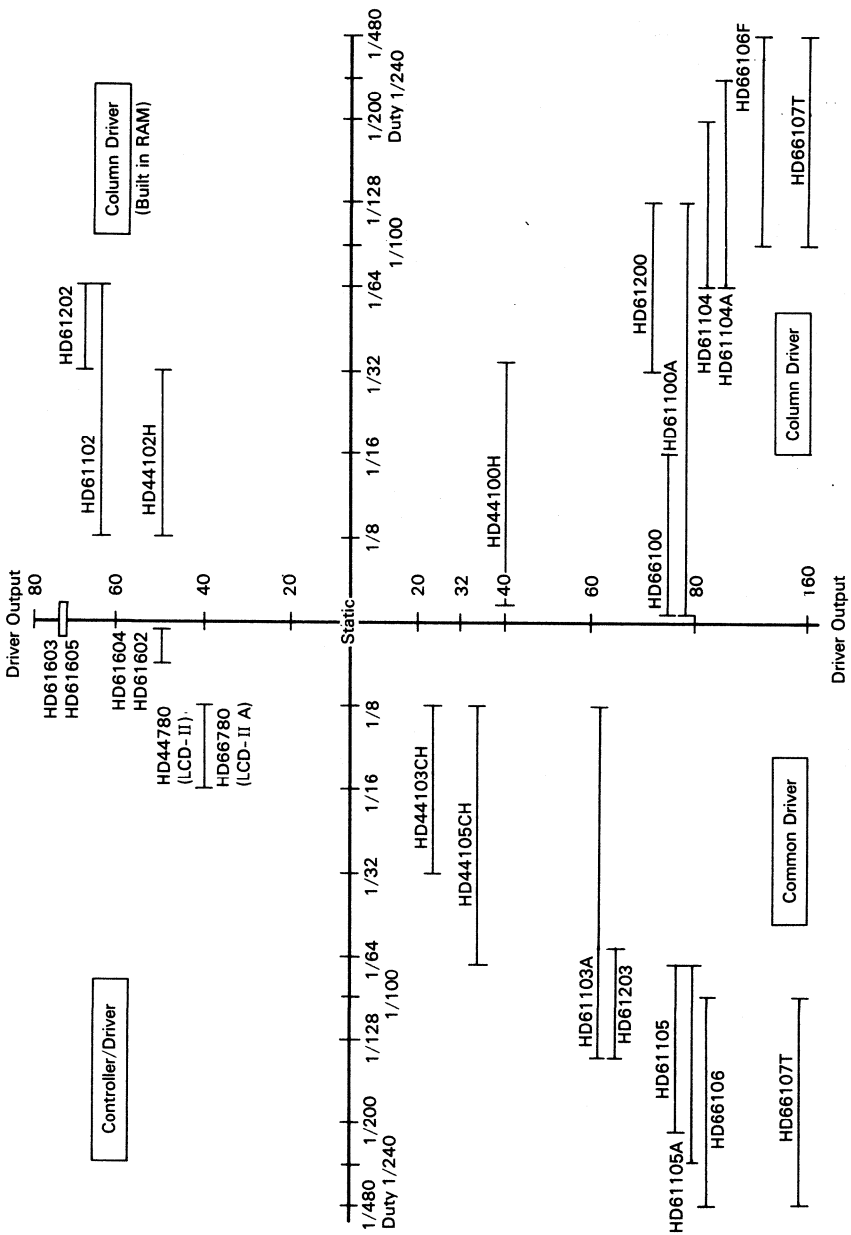
Type		Character Display				Graphic Display			
Type Number		**HD61105A**	**HD43160AH**	**HD44780 (LCD-II)**	**HD66780 (LCD-IIA)**	**HD61830**	**HD61830B**	**HD63645 HD64645 HD64646 LCTC**	**HD66840 LVIC**
Power supply for internal circuits (V)		5	5	5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		28	–	11	5	–	–	–	–
Power Dissipation (mW)		5	10	2	2	30	50	50	250
Operating Temperature (°C)		−20 to +75	−20 to +75	−20 to +75*1	−20 to +75	−20 to +75	−20 to +75*1	−20 to +75	−20 to +75
Memory	ROM (bit)	–	6420	7200	12000	7360	7360	–	–
	RAM (bit)	–	80×8	80×8, 64×8	16	–	–	–	–
LCD Driver	Common	80	–	16	16	–	–	–	–
	Column	–	–	40	40	–	–	–	–
Instraction Set		–	6	11	11	12	12	–	–
Operation Frequency (MHz)		0.1	0.25/0.375	0.25	0.25	1.1	2.4	10	25(30)
Duty		1/64-1/240	1/8,1/12, 1/16	1/8,1/11, 1/16	1/8,1/11, 1/16	Static -1/128	Static -1/128	Static -1/512	4-1/1024
Package		FP-100	FP-54	FP-80, FP-80A	FP-80A FP-80B	FP-60	FP-60	FP-80, FP-80B	FP-100A

*1 -40 to +85°C (Special request). Please contact Hitachi agents.

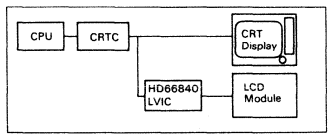
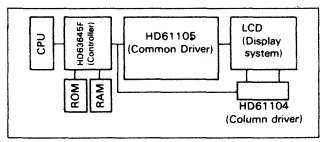
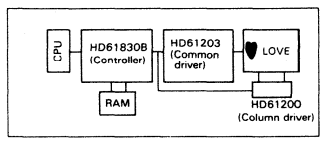
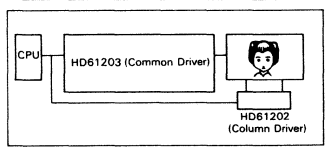
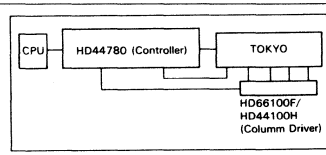
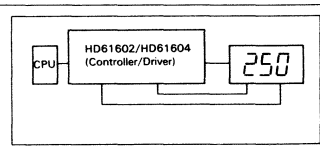
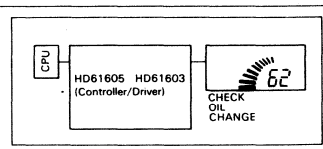
Type Number Order

Type	Function	Reference Page
HD43160AH	LCD Controller	83
HD44100H	LCD Driver with 40 Channel Output	61
HD44102CH	LCD Column Driver with 50 Channel Output	205
HD44103CH	LCD Common Driver with 20 Channel Output	230
HD44105H	LCD Common Driver with 32 Channel Output	239
HD44780 LCD-II	LCD Controller/Driver	98
HD61100A	LCD Column Driver with 80 Channel Output	248
HD61102	LCD Column Driver with 64 Channel Output	261
HD61103A	LCD Common Driver with 64 Channel Output	291
HD61104	LCD Column Driver with 80 Channel Output	388
HD61104A	LCD Column Driver with 80 Channel Output	388
HD61105	LCD Common Driver with 80 Channel Output	433
HD61105A	LCD Common Driver with 80 Channel Output	433
HD61200	LCD Column Driver with 80 Channel Output	316
HD61202	LCD Column Driver with 64 Channel Output	330
HD61203	LCD Common Driver with 64 Channel Output	361
HD61602	Segment Display Type LCD Driver	601
HD61603	Segment Display Type LCD Driver	601
HD61604	Segment Display Type LCD Driver	632
HD61605	Segment Display Type LCD Driver	632
HD61830 LCTC	LCD Timing Controller	450
HD61830B LCTC	LCD Timing Controller	477
HD63645 LCTC	LCD Timing Controller	503
HD64645 LCTC	LCD Timing Controller	503
HD64646 LCTC	LCD Timing Controller	542
HD66100	LCD Driver with 80 Channel Output	71
HD66106F	LCD Column/Common Driver with 80 Channel Output	398
HD66107T	LCD Column/Common Driver with 160 Channel Output	413
HD66780 LCD-IIA	LCD Controller/Driver	156
HD66840F LVIC	LCD Video Interface Controller	552

Selection Guide



Hitachi LCD Driver System

Type	Reference Figure	Screen Size (max)	Lineup	Application
Video to LCD converter		720×512 dots	HD66840, HD66106(Driver) HD66107(Driver), HD61104(Column) HD61105(Common)	Personal Computer, Terminal, OHP
Display System for CRT Compatible		640×400 dots	HD63645/64645/ 64646(Controller) HD61104(Column)/ 61105(Common) HD66106(Driver)	Personal Computer, Word-processor, Terminal
Graphic Display System		Character 80×16 Graphic 480×128 dots	HD61100A(Column), HD61830B(Controller) HD61200(Column) HD61103A(Common), HD61203(Common)	Laptop Computer, Facsimile, Telex, Copy machine
Graphic Display System (Bitmap)		480×128 dots	HD44102CH(Column)/ 61102(Column) HD44103CH(Common) HD61202(Column) HD44105H(Common)/ 61103A(Common) HD61203(Common)	Laptop Computer, Handy Word-processor, Toy
Character Display System		40 Characters ×2 Columns 80 Characters ×1 Column	HD44780(LCD-II) (Controller/Driver) HD66780(LCD-IIA) (Controller/Driver) HD44100H(Column) HD66100F(Column)	Electrical Typewriter, Multifunction Telephone, Handy Terminal
Segment Display System		25 Digits ×1 Column	HD61602 (Controller/Driver) HD61604 (Controller/Driver)	ECR, Measurement System, Telephone
Static Display System		64 Segments	HD61603 (Controller/Driver) HD61605 (Controller/Driver)	Industrial Measurement System

Application

Character and Graphic Display

1 character=7 × 8dot (15× 7 dot +cursor)

Character / Line	8	16	20	24	32	40	Over 80
1		HD66100					
2							
3				HD44100H			
4							
6 to 8							
12 to 15	HD61200 (Column) + HD61203 (Common)						
16 to 25	HD61104 (Column) + HD61105 (Common)						
26 to 50	HD66106, HD66107						

Graphic Display

Horizontal / Vertical	48	96	120	180	240	480	Over 640
16	HD61202 (Column) + HD61203 (Common)						
32							
48							
64							
128	HD61104 (Column) + HD61105 (Common)						
400							
Over 400	HD66106, HD66107						

Note: Applications in this page are mere example, and this combination of devices is not the best.

Differences Between Products

1. HD66100F and HD44100H

	HD66100F	HD44100H
LCD drive circuits	80	20×2
Power supply for internal logic (V)	3 to 6	4.5 to 11
Display duty	Static to 1/16	Static to 1/32
Package	100 pin plastic QFP	60 pin plastic QFP

2. HD61100A and HD61200

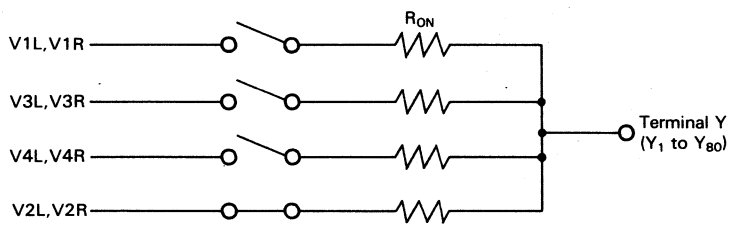
		HD61100A	HD61200
LCD drive circuits	common	–	–
	column	80	80
Display duty		static to 1/128	1/32 to 1/128
Power supply for LCD drive circuits (V)		0 to 17	8 to 17
Power supply limits of LCD driver circuit voltage		V_{CC} to V_{EE} (no limit)	shown in figures below

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y_1 to Y_{80}. This value is specified under the following condition.

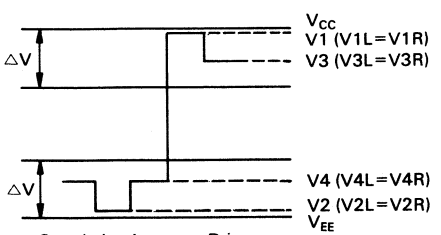
$V_{CC}-V_{EE}=17V$

$V1L=V1R$, $V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$

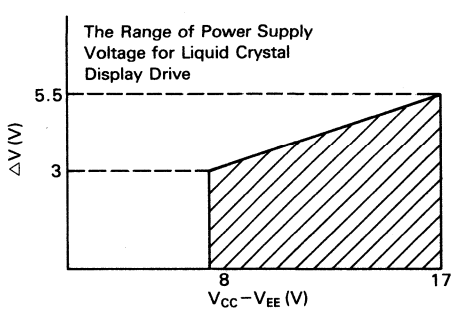
$V2L=V2R$, $V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$



Here is a description of the range of power supply voltage for linquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice the ΔV depends on power supply voltage $V_{CC}-V_{EE}$.



Correlation between Driver Output Waveform and Power supply Voltages for Liquid Crystal Display Drive



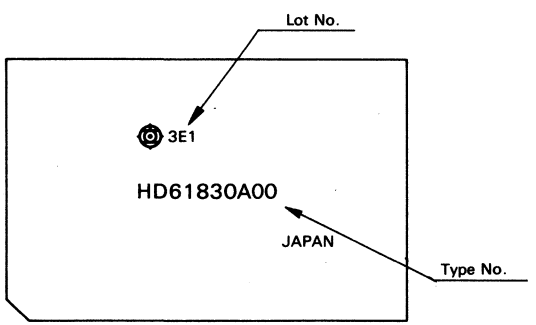
Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

3. HD66100F and HD61100A

		HD66100F	HD61100A
LCD driver circuits	common	–	–
	column	80	80
Power supply for LCD drive circuits (V)		3 to 6	5.5 to 17.0
Display duty		static to 1/16	static to 1/128
Operating frequency (MHz)		1.0 MHz (max)	2.5 MHz (max)
Data fetch method		Shift	Latch
Package		100 pin Plastic QFP (FP-100)	100 pin plastic QFP (FP-100)

4. HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal	External
Operating frequency (MHz)	1.1 MHz	2.4 MHz
Display duty	static to 1/128	static to 1/128
Programmable screen size (Max)	64×240 dots (1/64 duty)	128×480 dots (1/64 duty)
Other	pin 6:C pin 7:R pin 9:CPO	pin 6:$\overline{CE}$ pin 7:$\overline{OE}$ pin 9:NC
Package Marking	Ⓐ	Ⓑ



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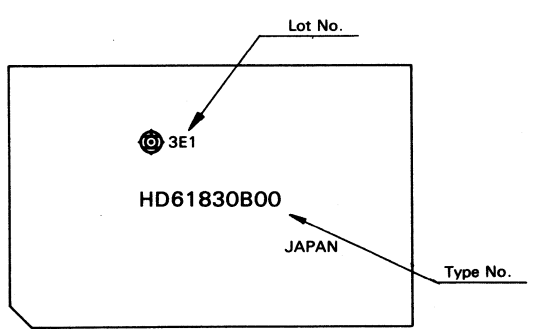

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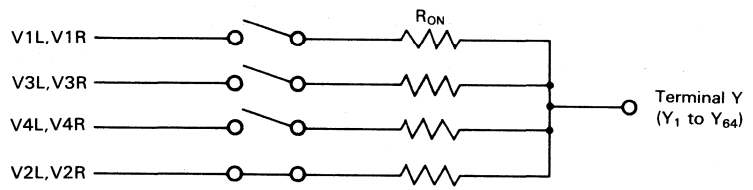
5. HD61102 and HD61202

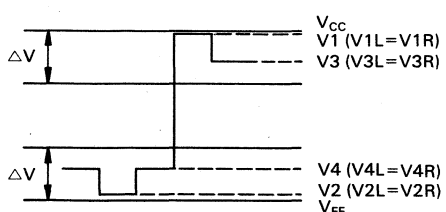
	HD61102	HD61202
Display duty	static to 1/64	1/32 to 1/64
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 15.5	8 to 17
Power supply limits of LCD driver circuits voltage	V_{CC} to V_{EE} (no limit)	shown following figure
Pin 88	DY (output)	NC (non connection)
Absolute maximum rating of V_{EE} (V)	$V_{CC}-17.0$ to $V_{CC}+0.3$	$V_{CC}-19.0$ to $V_{CC}+0.3$

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y_1 to Y_{64}. This value is specified under the following condition.

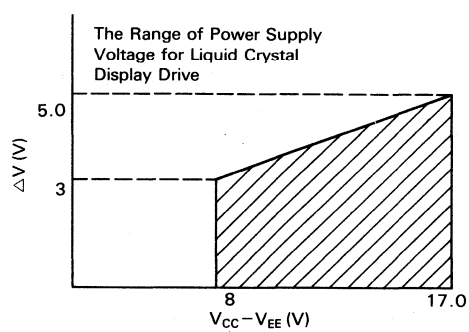
$V_{CC}-V_{EE}=15.5V$
$V1L=V1R$, $V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V3L =V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.



Correlation between Driver Output Waveform and Power supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

6. HD61103A and HD61203

	HD61103A	HD61203
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 17	8 to 17
Power supply limits of LCD drive circuits voltage	V_{CC} to V_{EE} (no limit)	shown in figures below
Output terminal	shown in following figure 4	shown in following figure 5

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

$V_{CC}-V_{EE}=17V$
$V1L=V1R$, $V6L=V6R=V_{CC}-1/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V5L=V5R=V_{EE}+1/7\ (V_{CC}-V_{EE})$

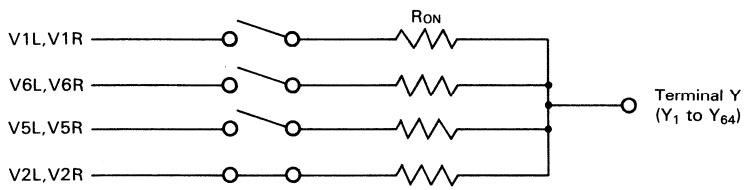
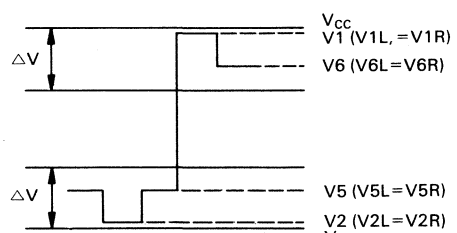


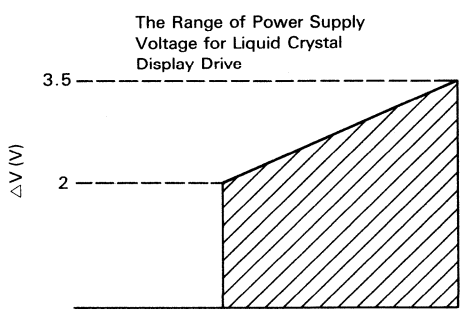
Figure 1.

Here is a description of the range of power supply voltage for liquid crystal display drive. Apply postive voltage to V1L=V1R and V6L=V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

Figure 2.



Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

Figure 3.

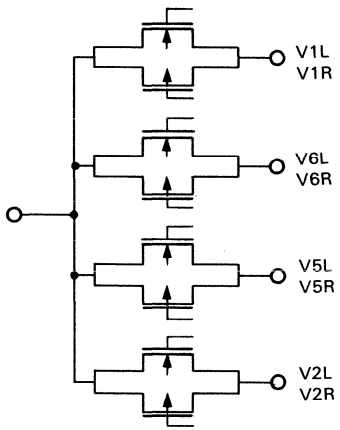


Figure 4.

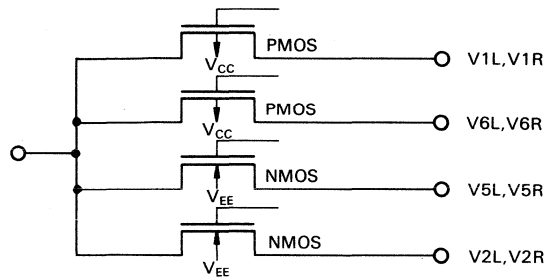


Figure 5.

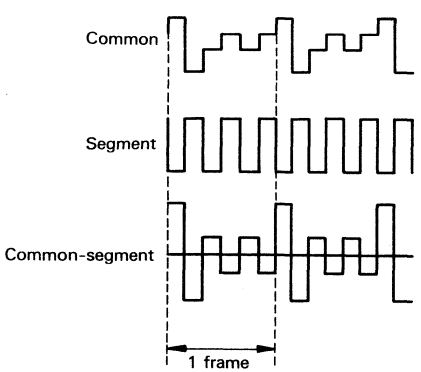
7. HD66106F and HD61104

	HD66106F	HD61104
LCD drive circuits voltage	+14 to +35 (V_{LCD}-GND)	-10 to -26 (V_{CC}-V_{EE})
Display Duty	1/100 to 1/400	1/64 to 1/200
Operating frequency (MHz)	6.0 MHz	3.5 MHz
Function	column and common driver	column driver

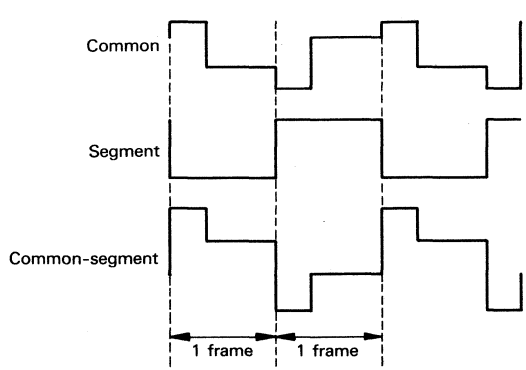
8. HD44780 LCD-II and HD66780 LCD-II A

Item		LCD-II (HD44780)	LCD-II A (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	Same as LCD-II	
*Character generator ROM (kinds of characters)		7200 bits 192 characters 5×7;160 characters 5×10;32 characters	12000 bits 240 characters 5×10;240 Characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	Same as LCD-II	
LCD driving terminals (Maximum number of display characters/ unit)		16 COMs 40 SEGs (16 characters)	Same as LCD-II	
Character font (with a cursor)		5x8 dots 5×11 dots	Same as LCD-II	
Multiplexing duty ratio		1/8, 1/11, 1/16	Same as LCD-II	
*LCD driving voltage	1/4 bias	3.0 to 11 (V)	3.0 to V_{CC} (V)	V_{CC} to V_5
	1/5 bias	4.6 to 11 (V)	3.0 to V_{CC} (V)	
*LCD driving waveform		waveform A	waveform B	Shown following figures
*Bus timing		1, 1.5MHz	2MHz	
Instruction codes		11 instructions	Same as LCD-II	
Power-on reset circuit		Yes	Same as LCD-II	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	Same as LCD-II	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A	Same as LCD-II	

Note: *Indicates the modified items in LCD-II A.



Waveform A (1/3 Duty, 1/3 Bias)



Waveform B (1/3 Duty, 1/3 Bias)

9. HD61104 and HD61104A

	HD61104	HD61104A
LCD Drive Circuits	80	80
Data Transfer Rate (MHz)	3.5	3.5
Power Supply for LCD drive circuits (V)	10 to 26	10 to 28

10. HD61105 and HD61105A

	HD61105	HD61105A
LCD Drive Circuits	80	80
Power Supply for LCD drive circuits (V)	10 to 26	10 to 28

11. HD66106F and HD66107T

	HD66106F	HD66107T
LCD drive circuits	80	160
Data transfer	4-bits	4-bits/8-bits
Operating frequency (MHz)	6	8
Power supply for LCD drive circuits	14 to 37	14 to 37
Packge	100-Pin plastic QFP (FP-100A)	192-pin TAB

12. HD63645, HD64645 and HD64646

	HD63645	HD64645	HD64646
CPU interface	68 family	80 family	80 family
Package	80-pin plastic QFP (FP-80)	80-pin Plastic QFP (FP-80)	80-pin plastic QFP (FP-80A)
Other	–	–	HD64646 has another LCD drive interface in HD64645

Package Information

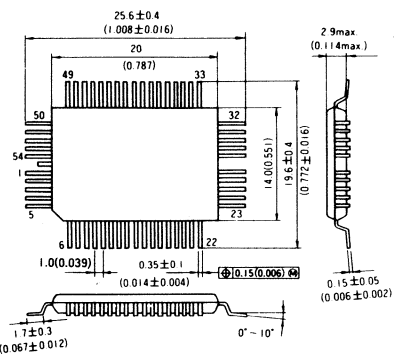
Packge Information

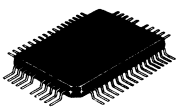
The Hitachi LCD driver devices use plastic flat packages to make compact equipment in which they are incorporated and provide higher dencity mounting by utilizing the features of thin liquid crystal display elements.

Package Dimention

Scale: 3/2

FP-54

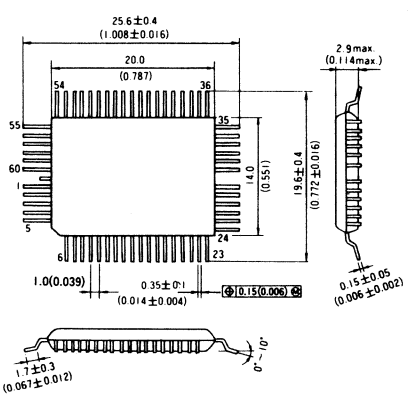


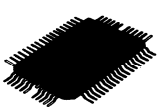


Code	FP-54
EIAJ	——
JEDEC	——

Applicable LSI	HD43160AH

FP-60

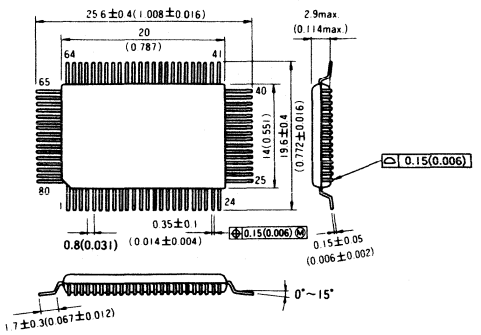


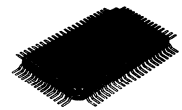


Code	FP-60
EIAJ	——
JEDEC	——

Applicable LSI	HD44100H, HD44103CH, HD44105H HD61830, HD61830B

FP-80

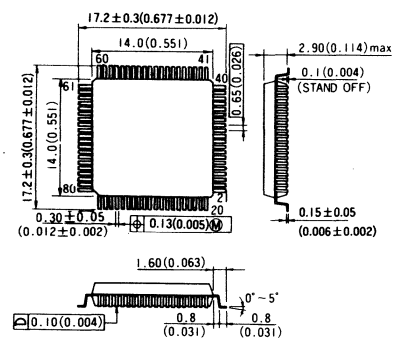




Code	FP-80
EIAJ	——
JEDEC	——

Applicable LSI	HD61602, HD61603, HD61604, HD61605 HD44780, HD66780, HD63645, HD64645 HD64646, HD44102CH

FP-80A

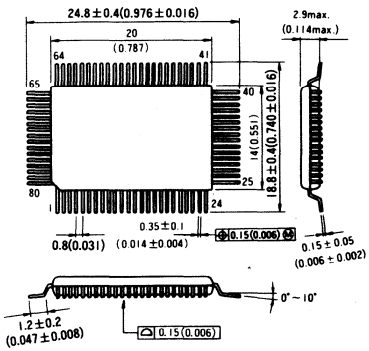


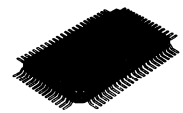
Code	FP-80A
EIAJ	——
JEDEC	——

Applicable LSI	HD66780, HD44780, HD61602

Package Information

FP-80B

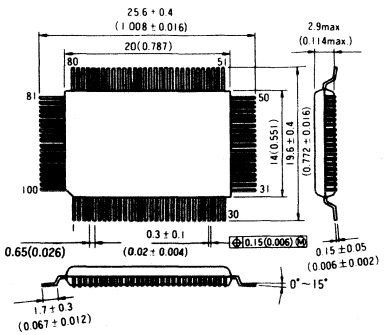


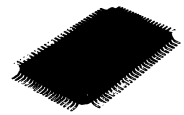


Code	FP-80B
EIAJ	——
JEDEC	——

Applicable LSI	HD64646, HD66780

FP-100

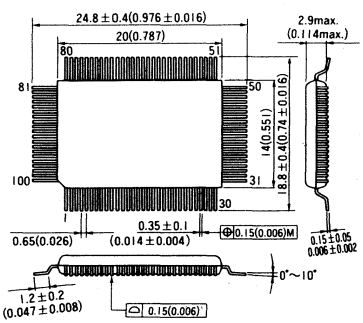


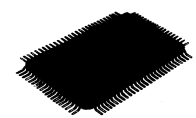


Code	FP -100
EIAJ	——
JEDEC	——

Applicable LSI	HD61100A, HD61102, HD61103A, HD61104 HD61105, HD61200, HD61202, HD61203 HD66100

FP-100A





Code	FP-100A
EIAJ	——
JEDEC	——

Applicable LSI	HD66106, HD66840

Reliability and Quality Assurance

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual user's purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize such quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance moral for quality.

In addition, quality required by users on semiconductor devices is going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.

(2) Build the quality at the sources of manufacturing process.

(3) Execute the harder inspection and reliability confirmation of final products.

(4) Make quality level higher with field data feed back.

(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the

semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices, only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode
   - Analysis of relation between failure mode and manufacturing process condition
   - Search for failure mechanism analysis
   - Establishment of QC point in manufacturing
2. Effectiveness of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.

- Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
- Able to analyze relation between failure causes and manufacturing factors.
- Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competitive power of products, the major purpose of design review is to ensure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.

(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub-program of calculation, experiments, investigation, etc. will be carried out.

(3) Determine contents of reliability and methods, etc. based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Discussion about preparation for production.

(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.

(7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.

(2) Feedback of information should be made to ensure satisfied level of process ability.

(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

(1) The third party performs approval objectively from the standpoint of customers.

(2) Fully consider past failure experiences and information from field.

(3) Approval is needed for design change and work change.

(4) Intensive approval is executed on parts material and process.

(5) Study process ability and fluctuation factor, and set up control points at mass production stage.

Considering the views mentioned above, quality approval shown in Fig. 1 is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are getting higher, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows:

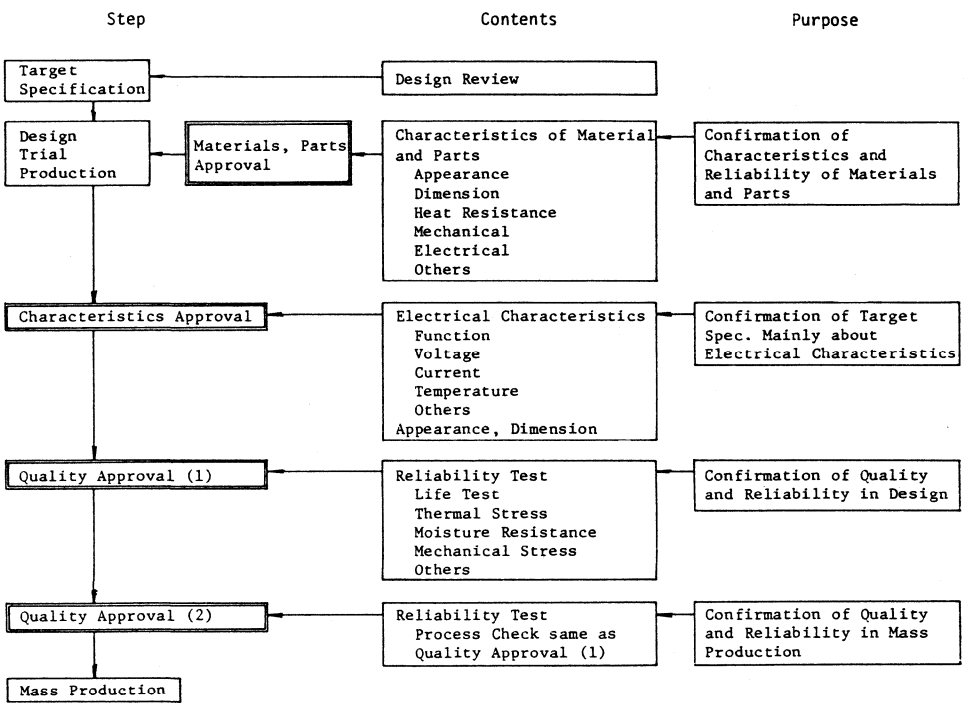


Fig. 1 Flow Chart of Quality Approval

(1) Outside Vendor Technical Information Meeting

(2) Approval on outside vendors, and guidance of outside vendors

(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub-materials. The quality control in the manufacturing process is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and the quality control in the manufacturing process is tightly executed - rigid check in each process and each lot, 100% inspection in appropriate ways to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of counter-measures
- Transmission of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Equipments for manufacturing semiconductor devices have been developing extraordinarily with necessary high performance devices and improvement

of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain proper operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and

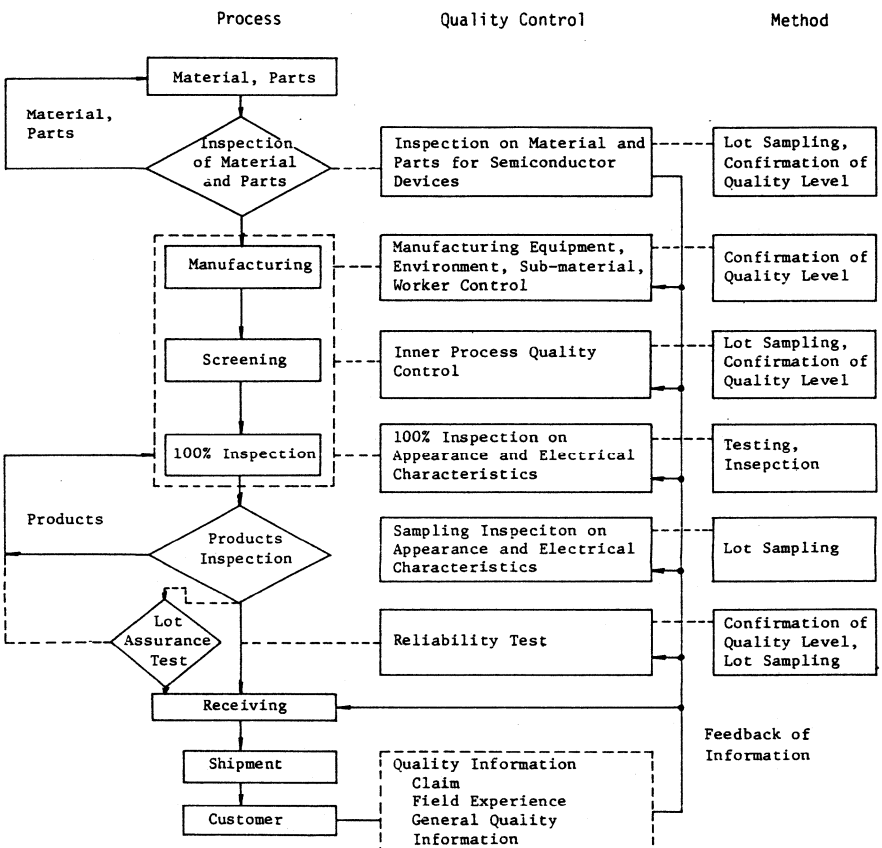


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Submaterials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances - temperature, humidity, dust - and the control of submaterials - gas, pure water - used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, airconditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, parts	Important control items	Point for check
Wafer	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratch
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratch, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratch
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratch
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

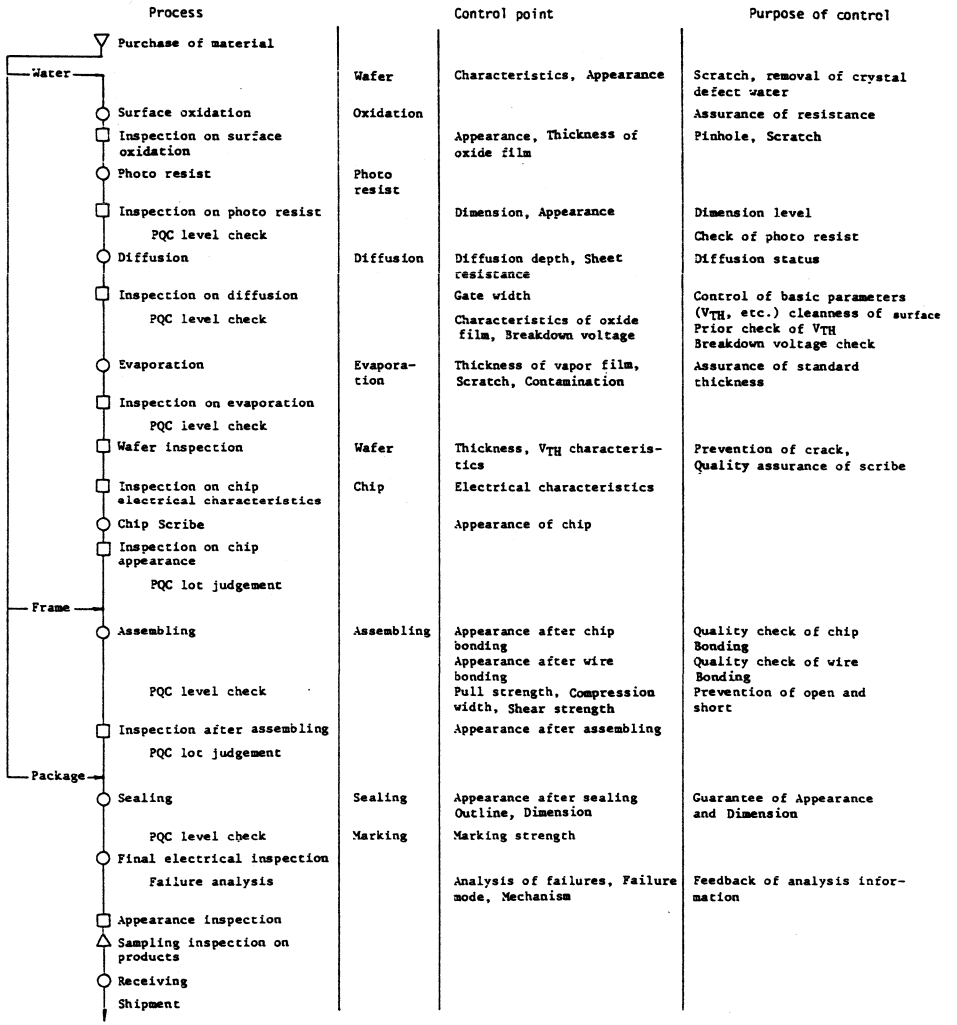


Fig. 3 Example of Inner Process Quality Control

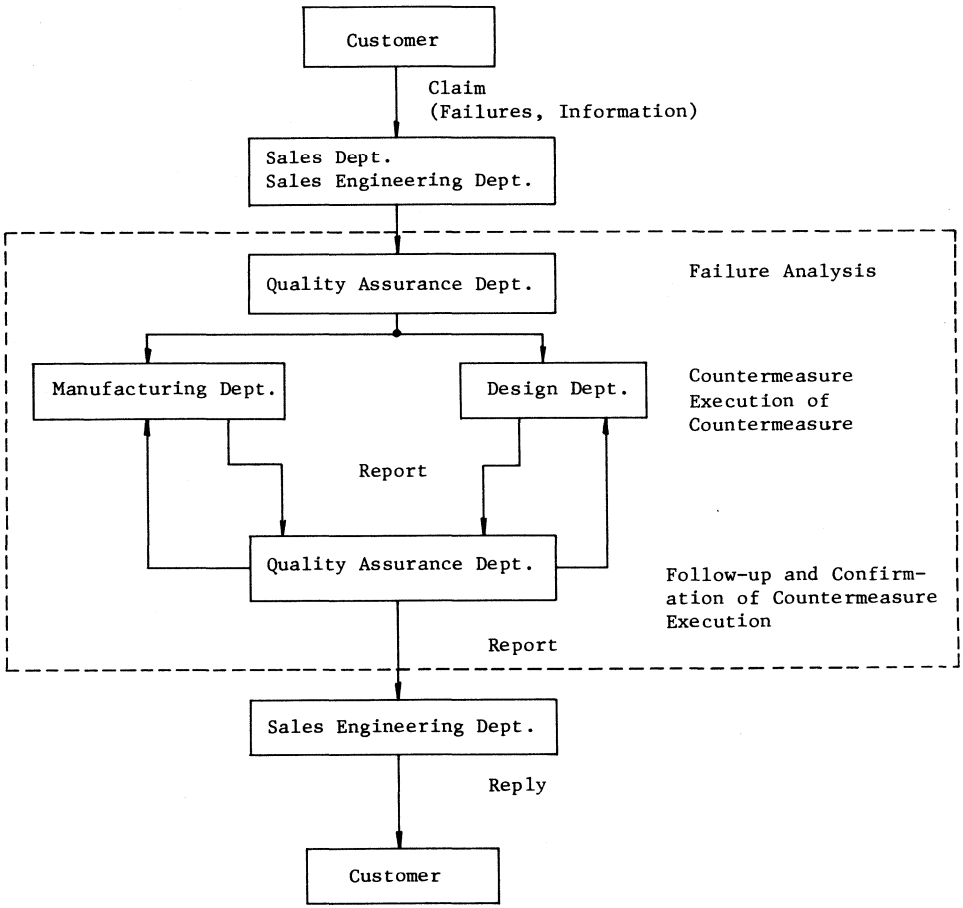


Fig. 4 Process Flow Chart of Field Failure

RELIABILITY TEST DATA OF LCD DRIVERS

1. INTRODUCTION

The use of liquid crystal displays with microcomputer application systems has been increasing, because of their merits such as low power consumption, freedom in display pattern design, and thin shape. Low power consumption and high density packaging have been achieved through the use of the CMOS process and the flat plastic packages, respectively.

This chapter describes reliability and quality assurance data for Hitachi LCD driver LSIs based on test data and failure analysis results.

2. CHIP AND PACKAGE STRUCTURE

Hitachi LCD driver LSI family are produced in low power CMOS technology and flat plastic package. Si-gate process is used for high reliability and high density. Chip structure and basic circuit are shown in Fig. 1, and package structure is shown in Fig. 2.

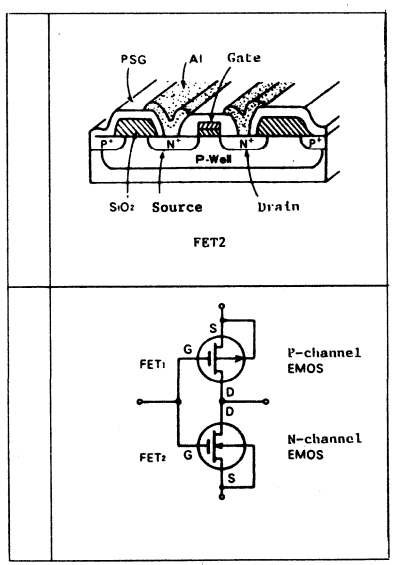


Fig. 1 Chip Structure and Basic Circuit

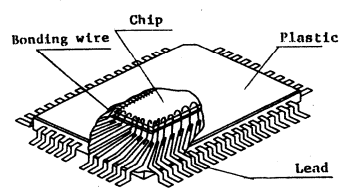


Fig. 2 Package Structure

3. RELIABILITY TEST RESULTS

The test results of LCD Driver LSI family are shown in Table 1, 2 and 3.

Table 1 Test Result (1), High Temperature Operation
(Ta=125°C, V_{CC}=5.5V)

Device	Sample size	Component hour	Failure
HD44100H	40	40,000	0
HD44102CH	40	40,000	0
HD44103CH	40	40,000	0
HD44780	90	90,000	0
HD66100F	45	45,000	0
HD61100A	80	80,000	0
HD61102	50	50,000	0
HD61103A	50	50,000	0
HD61200	40	40,000	0
HD61202	50	50,000	0
HD61203	40	40,000	0
HD61104	45	45,000	0
HD61105	45	45,000	0
HD61830	40	40,000	0
HD61830B	40	40,000	0
HD63645	32	32,000	0
HD64645	32	32,000	0
HD61602	38	38,000	0
HD61603	32	32,000	0
HD61604	32	32,000	0
HD61605	32	32,000	0

Table 2 Test Result (2)

Test item	Test condition	Sample size	Component hour	Failure
High temp, storage	Ta=150°C, 1000 hrs.	180	1,800,000	0
Low temp, storage	Ta=-55°C, 1000 hrs.	140	1,400,000	0
Steady state humidity	65°C, 95% RH, 1000 hrs.	860	860,000	1*1
Steady state humidity biased	85°C, 90% RH, 1000 hrs.	165	170,000	2*2
Pressure cooker	121°C, 2 atm.100 hrs.	200	20,000	0

*1, *2: Aluminum corrosion

Table 3 Test Results (3)

Test items	Test condition	Sample size	Failure
Thermal shock	0 to 100°C 10 cycles	108	0
Temperature cycling	-55°C to 150°C 10 cycles	678	0
Soldering heat	260°C 10 sec.	283	0
Solderability	230°C 5 sec.	140	0

4. QUALITY DATA FROM FIELD USE

Field failure rate is estimated in advance through production process evaluation and reliability tests. Past field data on similar devices provides the basis for this estimation. Quality information from the users are indispensable to the improvement of products quality. Therefore, field data on products delivered to the users are followed up carefully. On the basis of information furnished by the user, failure analysis is conducted and the results are quickly fed back to the design and production divisions.

Failure analysis result on MOS LSI returned to Hitachi is shown in Fig. 3.

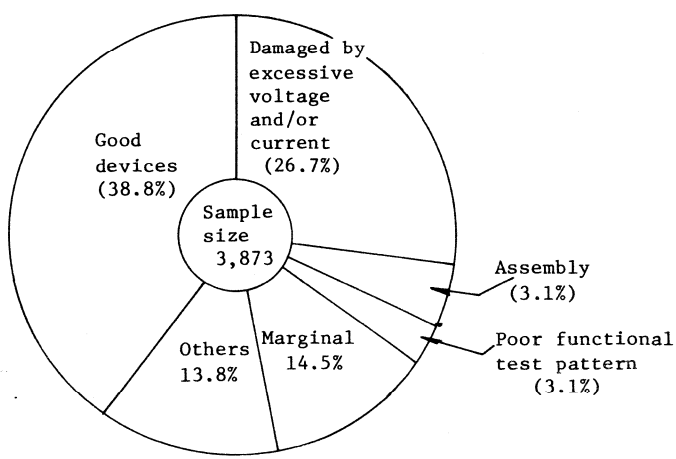


Fig. 3 Failure Analysis Result

5. PRECAUTION

5.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent detrioration in their electrical characteristics, solderability, and appearance, or breakage.

(1) Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.

(2) Store in a clean air environment, free from dust and active gas.

(3) Store in a container which does not induce static electricity.

(4) Store without any physical load.

(5) If semiconductor devices are stored for a long time, store them in the unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.

(6) If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpacked devices must not be stored for over 3 months.

(7) Take care not to allow condensation during storage due to rapid temperature changes.

5.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be given, too:

(1) Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.

(2) In order to prevent device breakage from clothes-induced static electricity, workers should be properly grounded with a resistor while handling devices. The resistor of about 1 M ohm must be provided near the worker to protect from electric shock.

(3) When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is

prevented by shorting terminal circuit. When a belt conveyor is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.

(4) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

5.3 Handling for Measurement

Avoid static electricity, noise and surge-voltage when semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open to provide the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will fail if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings.

Especially, while the devices are being tested, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source.

During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that no soldering bridge of foreign matter exists before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

FLAT PLASTIC PACKAGE (QFP) MOUNTING METHODS

The QFP can obtain better space factors than DIP type because the board occupying area and thickness can be reduced. No through holes nor lead forming is required for mounting the board. Therefore, the QFP can be mounted as it is, and is suitable for automatic mounting, providing remarkable reduction of manpower.

Various mounting methods are provided and can be used for each purpose. The typical example of mounting are given below.

1. Individual Mounting with Soldering Iron

   A method used mainly in the trial and small-scale production of circuits. The QFP can be soldered by fixing it on the mounting part of the printed circuit board with flux or adhesive agent while pressing it. For mounting, sharpen the tip of soldering iron or make it in a block shape so that more than one pin can be heated simultaneously. Use a fine solder (about ϕ 0.5mm). Solder within 10 seconds per IC at the maximum temperature of 260°C for lead and 235°C for resin part (lead bottom) as the heating conditions.

2. Reflow Soldering

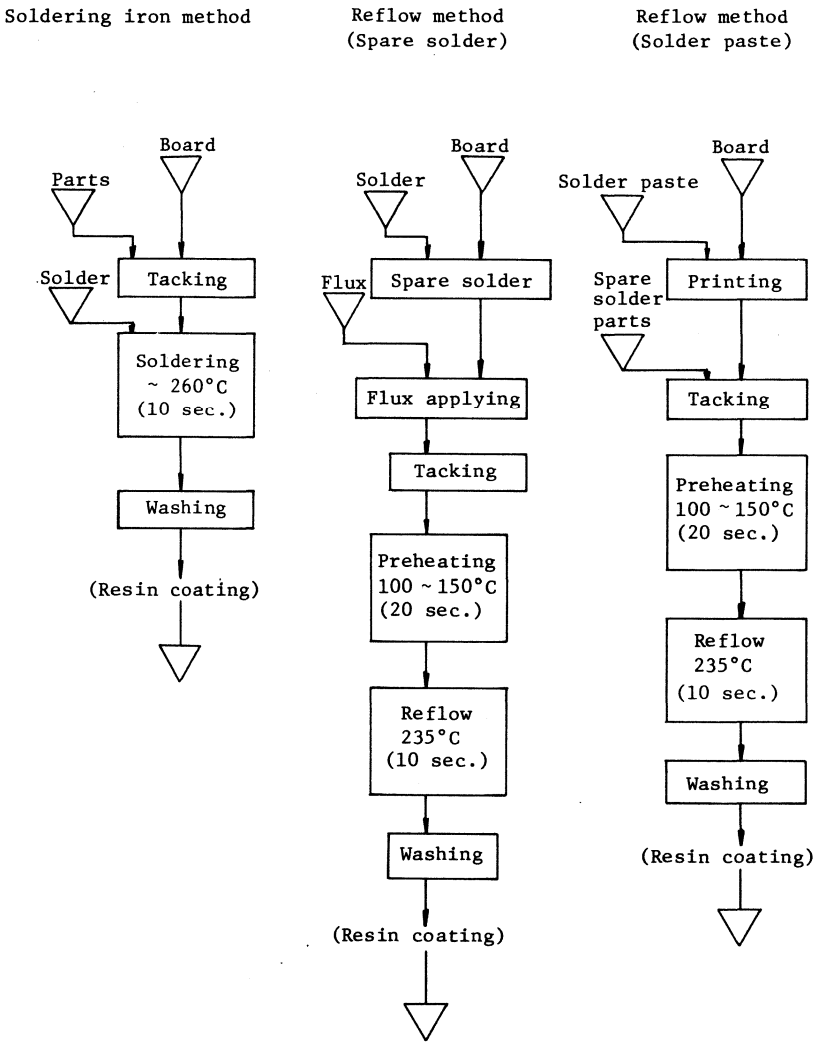
   The reflow soldering is the most general method in which the chips such as a transistor, a resistor and a capacitor are mounted on a hybrid IC. It can be also applied to the QFP. (Note) In addition, there are methods in which spare soldering and flux are applied to a printed circuit board in advance and in which solder paste is selectively applied to a printed circuit board by screen process printing.

   The QFP is tacked at a specified position with flux or solder paste. However, a small amount of adhesive can be applied to the rear of QFP for temporary fixing. Spare solder is melted by passing the board whose parts are tacked, through a temperature-controlled hot plate or conveyor type heater. Then the board can be soldered. In this case, preheat thoroughly to eliminate the thermal distortion of board and mounted parts. Pay attention to temperature control in consideration of the heat absorption of black plastic caused by an infrared-ray heater. As the heating conditions, preheat the board and parts for 20 seconds at a temperature of 100 to 150°C. Then heat them within 10 seconds at the maximum temperature of

235°C as a resin surface temperature . If the board is directly heated from the upper side of QFP with an infrared-ray heater, the temperature of resin surface becomes higher than the lead. Therefore, a shielding plate or similar thing must be used so that the temperature of resin surface can be 235°C or below.

(Note) Reflow soldering can be applied to the 2.9 mm (Max.) thick QFP used in the LCD driver series. However, the QFPs of 2.4 mm (Max.) and 1.5 mm (Max.) in thickness cannot be used for reflow soldering under the above conditions.

Flowcharts of Mounting Methods



Liquid Crystal Driving Methods

Driving a liquid crystal at direct current triggers electrode reaction inside the liquid cell, deteriorating display quality rapidly. The liquid crystal must be driven at alternating current. The AC driving method includes the static driving method and the multiplex driving method, each of which has the features and can be used for applications. Hitachi has been developping the LCD driver devices corresponding to the static driving method and the multiplex driving method. The following sections describe the features of each driving method, the driving waveforms and how to apply bias.

STATIC DRIVING METHOD

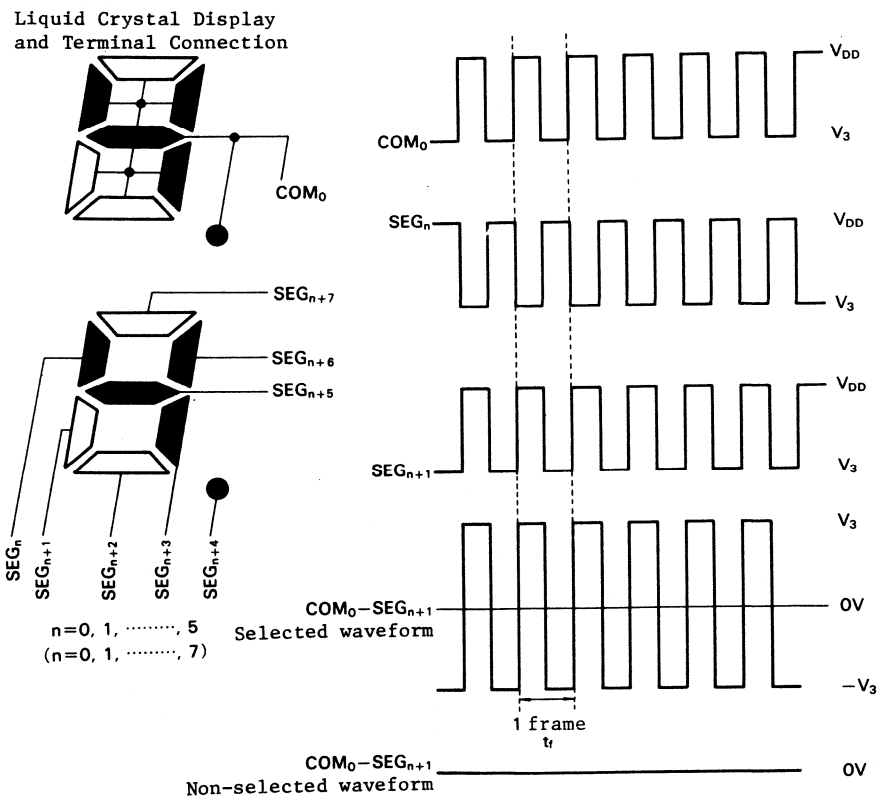


Fig. 1 Example of Static Drive Waveforms
(Example of HD61602/HD61603)

Fig. 1 shows the driving waveforms of the static driving method and an example in which "4" is displayed in the segment method. The static driving method is the most basic method in which good display quality can be obtained. However, it is not suitable for the display of the liquid crystal with many segments because one liquid crystal driver circuit is required per segment. The static driving method is used at the frame frequency ($1/t_f$) of several tens to several hundreds Hz.

MULTIPLEX DRIVING METHOD

The multiplex driving method is effective in reducing the number of driver circuits, the number of connections between the circuit and the display cell, and the cost when driving many display picture elements. Fig. 2 shows the comparision of the static drive with the multiplex drive (1/3 duty) in 8-digit numeric display. The number of liquid crystal driver circuits required is 65 for the former and 27 for the latter. The multiplex drive reduces the number of driver circuits. However, the more multiplexed, the

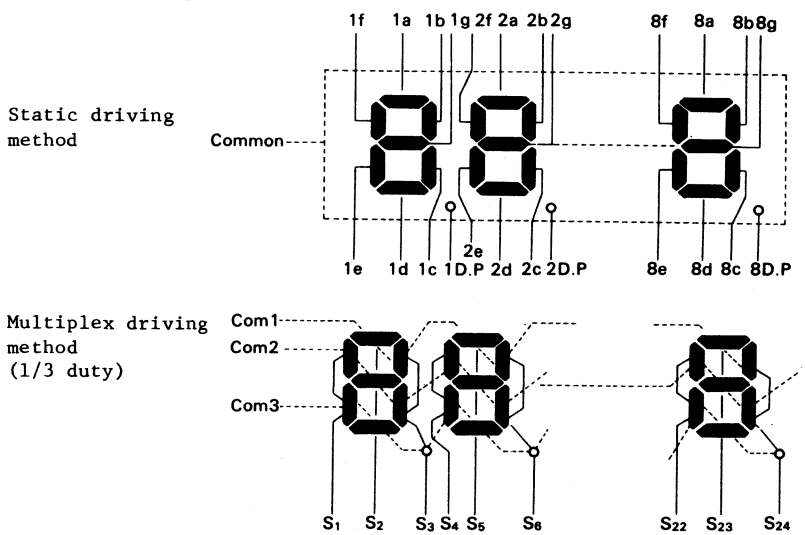


Fig. 2 Example of Comparision of Static Drive with Multiplex Drive

smaller the driving voltage tolerance. Thus, there are limits to extent of multiplexing.

There are two types of multiplex drive waveforms: A type and B type. A type, shown in Fig. 3, is used for alternation in 1 frame. B type is used for alternation in between 2 frames. B type has better display quality than A type in high multiplex drive.

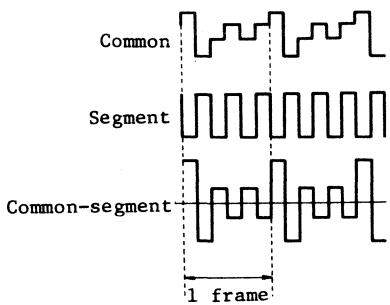


Fig. 3 A Type Waveforms (1/3 duty, 1/3 bias)

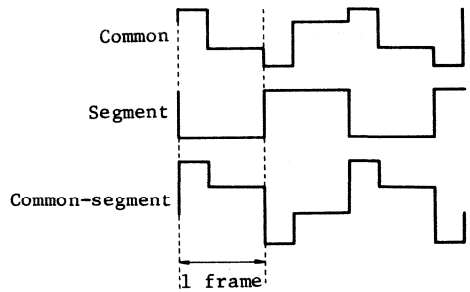


Fig. 4 B Type Waveforms (1/3 duty, 1/3 bias)

● 1/2 Bias, 1/2 Duty Drive

In the 1/2 duty drive, 1 driver circuit drives 2 segments. Fig. 5 shows an example of the connection in displaying '4' on the liquid crystal display of 7-segment type, and the output waveforms.

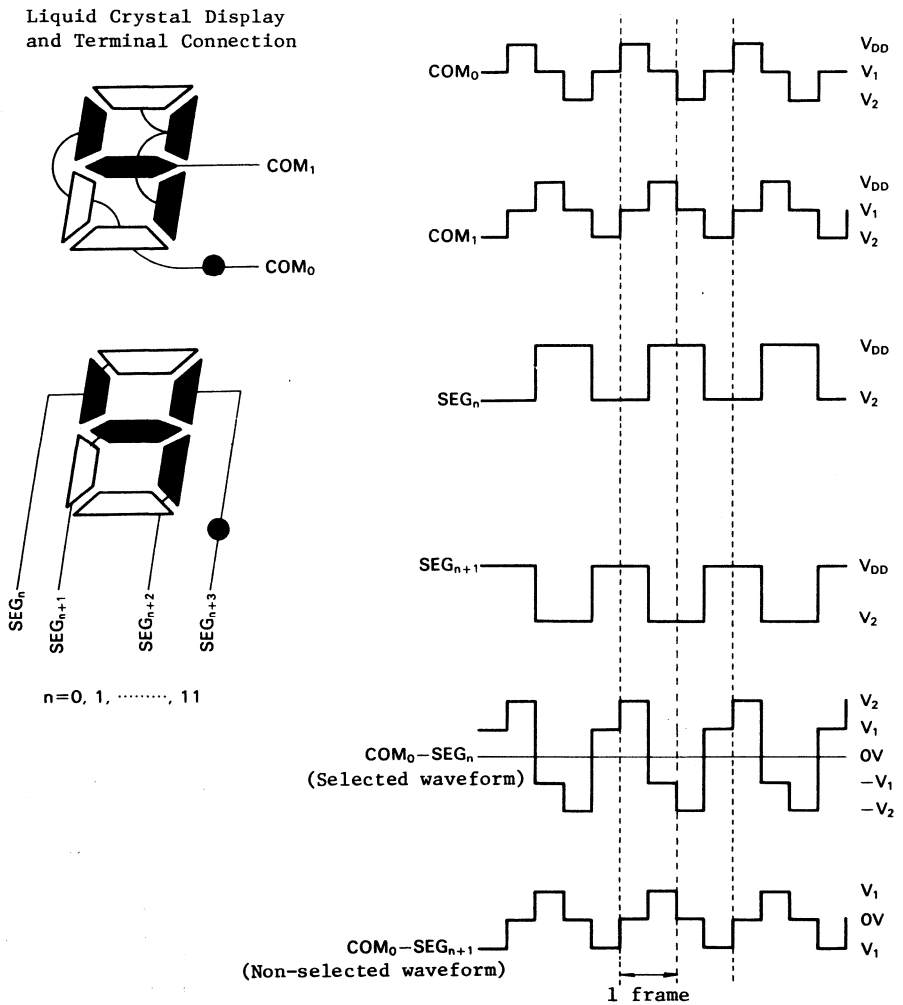


Fig. 5 Example of Waveforms in 1/2 Duty Drive (B type)
(Example of HD61602)

● 1/3 Bias, 1/3 Duty Drive

In the 1/3 duty drive, 3 segments are driven by 1 segment output driver. Fig. 6 shows an example of the connection in displaying '4' on the liquid crystal display of 7-segment type, and the output waveforms.

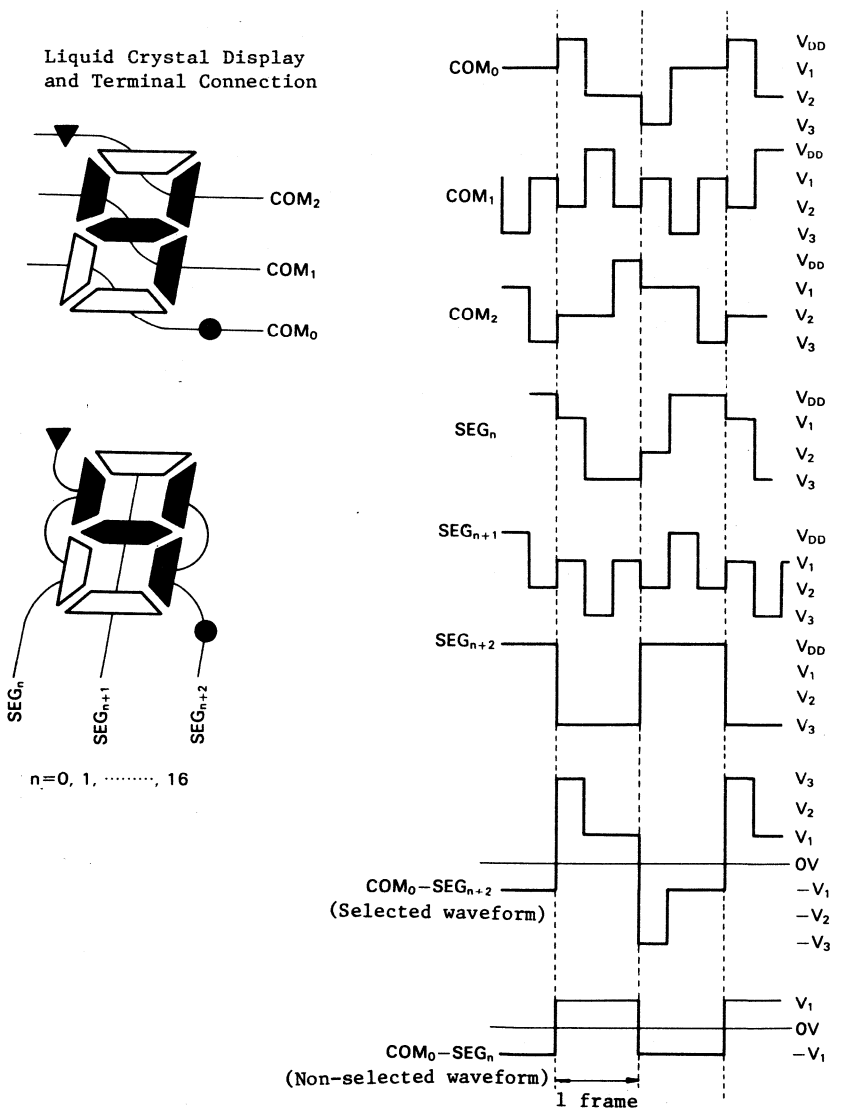


Fig. 6 Example of Waveforms in 1/3 Duty Drive (B type)
(Example of HD61602)

● 1/3 Bias, 1/4 Duty Drive

In the 1/4 duty drive, 4 segments are driven by 1 segment output driver. Fig. 7 shows an example of the connection in displaying '4' on the liquid crystal of 7-segment type, and the output waveforms.

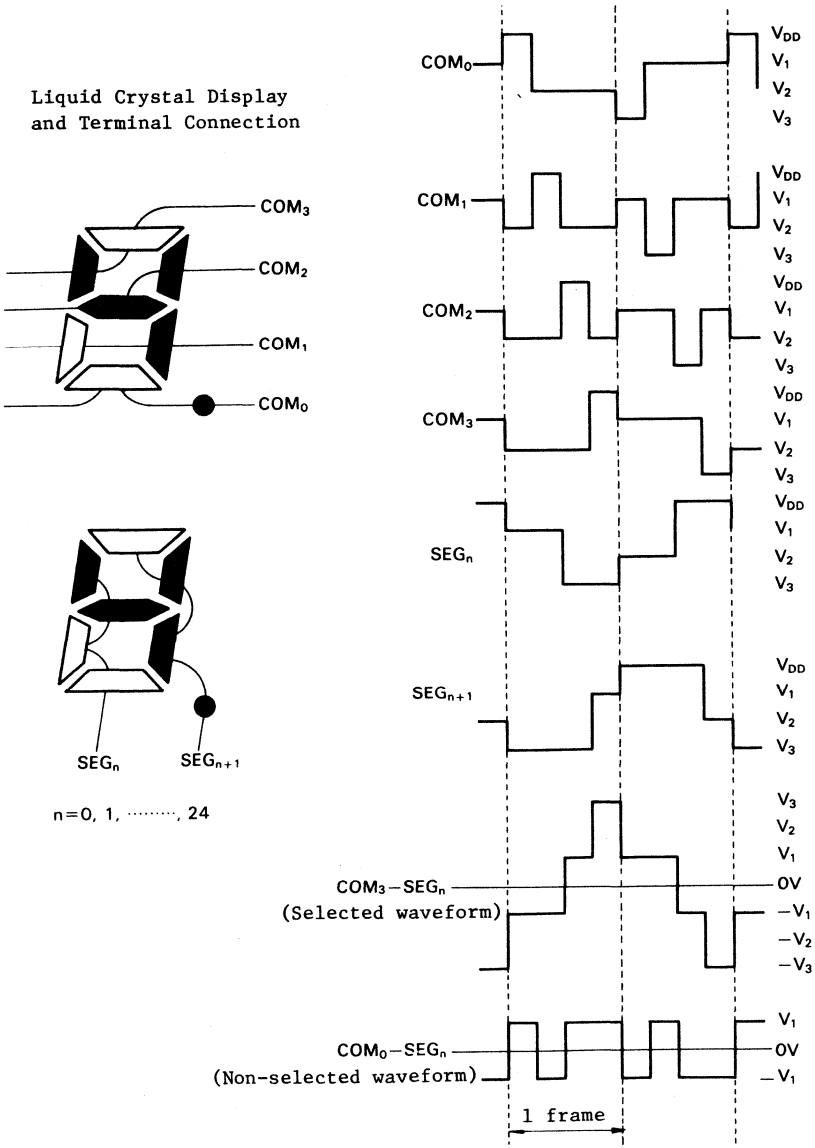
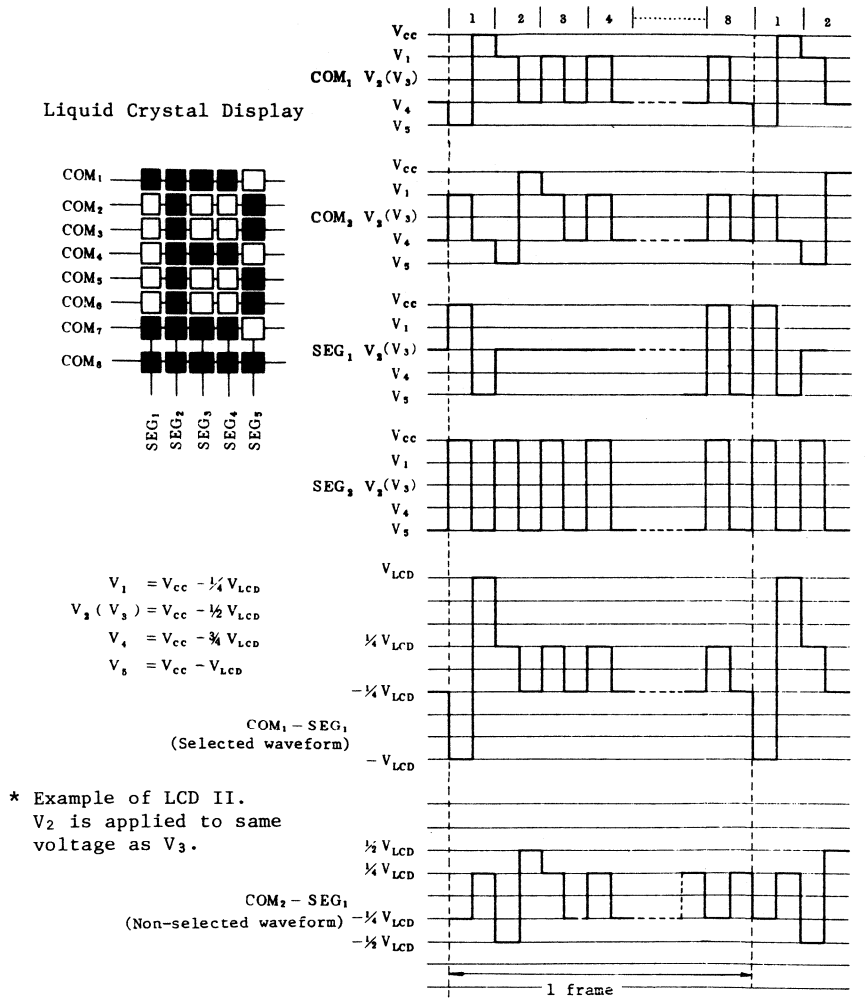


Fig. 7 Example of Waveforms in 1/4 Duty Drive (B type)
(Example of HD61602)

● 1/4 Bias, 1/8 Duty Drive



* Example of LCD II.
V_2 is applied to same voltage as V_3.

Fig. 8 Example of Waveforms in 1/8 Duty Drive (A type)
(Example of LCD-II)

● 1/5 Bias, 1/8 Duty Drive

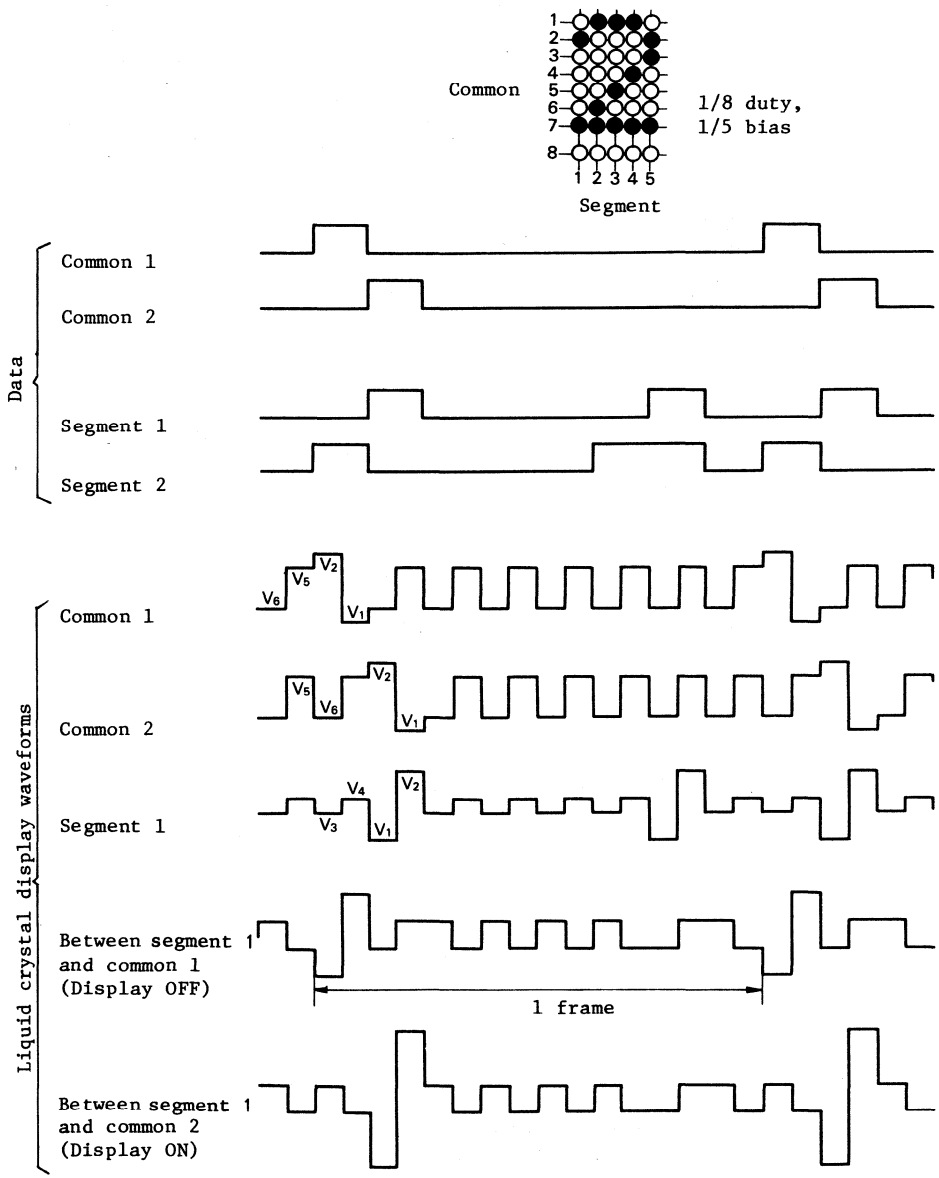


Fig. 9 Example of Waveforms in 1/8 Duty Drive (A type)
(Example of HD44100H)

● 1/5 Bias, 1/16 Duty Drive

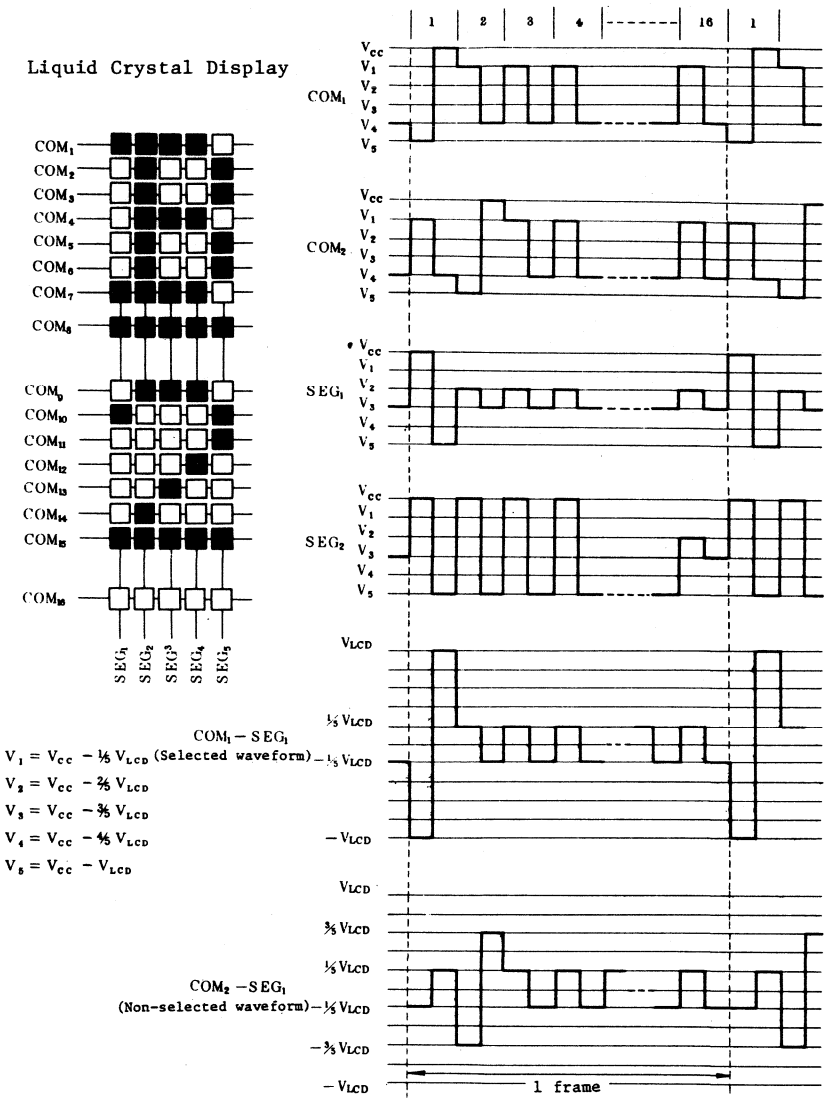


Fig. 10 Example of Waveforms in 1/16 Duty Drive (A type)
(Example of LCD-II)

● 1/5 Bias, 1/32 Duty Drive

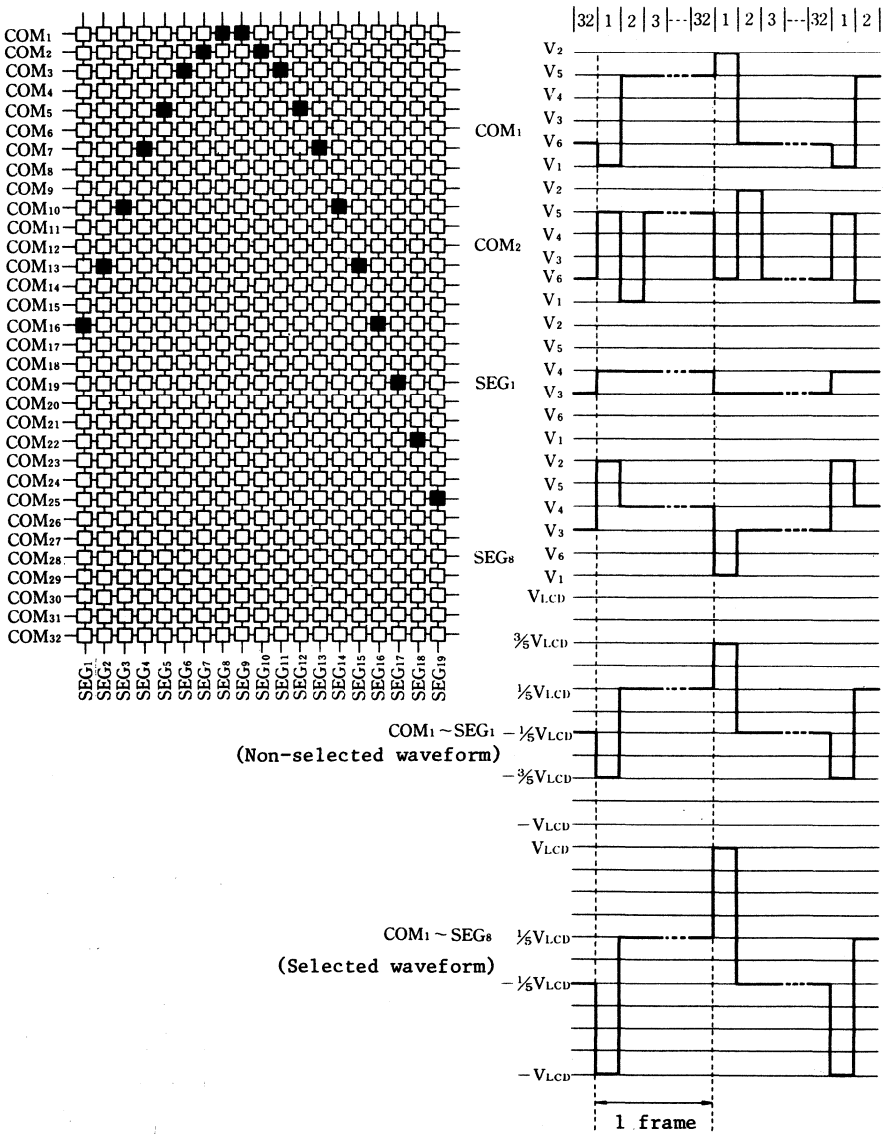


Fig. 11 Example of Waveforms in 1/32 Duty Drive
(Example of HD44102CH, HD44103CH)

■ POWER SUPPLY CIRCUIT FOR LIQUID CRYSTAL DRIVE

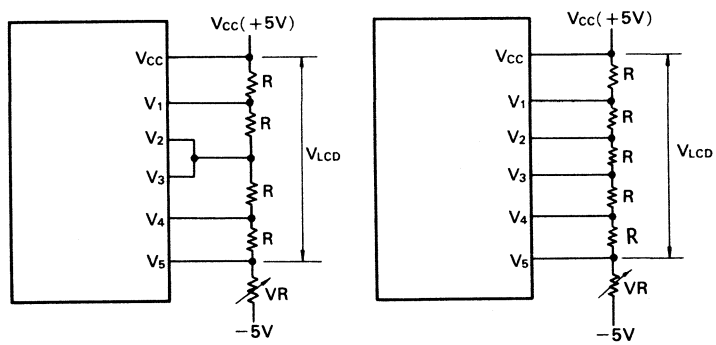
Table 1 shows the relationship between the number of driving biases and display duty ratios.

Table 1 Relationship between the Number of Dispaly Duties Ratio and the Number of Driving Biases

Display duty ratio	Static	1/2	1/3	1/4	1/7	1/8	1/11	1/12	1/14	1/16	1/24	1/32	1/64
Number of driving biases	2	3 (1/2 bias)	4 (1/3 bias)		5 (1/4 bias)				6 (1/5 bias)				

● Drive in Resistance Dividing

A driving bias is generally generated in resistance dividing.



(a) 1/4 Bias (1/8, 1/11 duty) (b) 1/5 Bias (1/16 duty)

Fig. 12 Example of Driving Voltage Supply

The setting of resistance value is determined by considering of operation margine and power consumption. Since the liquid crystal display load is capacitive, the drive waveform itself is distorted due to charge/discharge current when the liquid crystal display drive waveform is applied. To reduce distortion, the resistance value should be decreased but the power consumption increases because of the increase of the current through the dividing resistors. Since larger liquid crystal display panels have larger capacitance, the resistance value must be decreased.

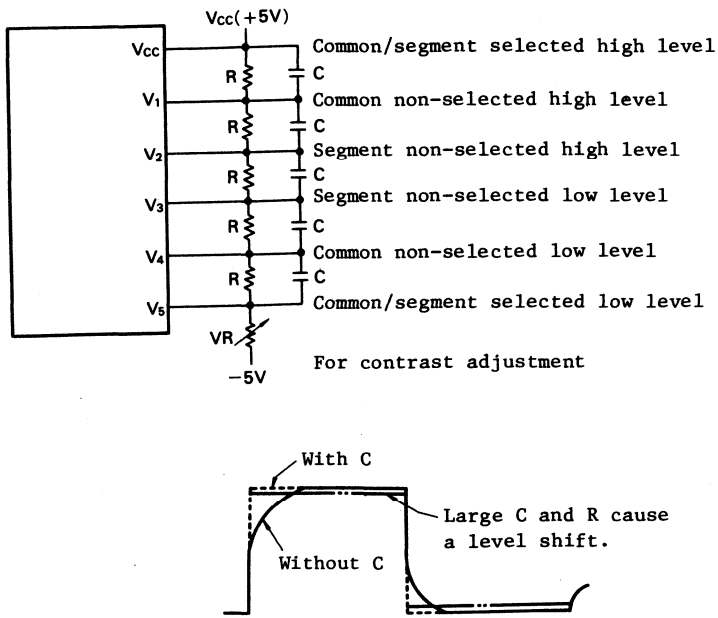


Fig. 13 Example of Capacitor Connection for Improvement of Liquid Crystal Display Drive Waveform Distortion (1/5 bias) (Example of LCD-II)

It is efficient to connect a capacitor to the resistors in parallel as shown in Fig. 13 in order to improve charge/discharge distortion. However, the effect is limited. Even if it is attempted to reduce the power consumption with a large resistor and improve waveform distortion with a large capacitor, a level shift occurs and the operating margine is not improved.

Since the liquid crystal display load is of matrix configuration, the path of the charge/discharge current through the load is complicated. Moreover, it varies depending on display condition. Thus, a value of resistance cannot be simply determined from the load capacitance of liquid crystal display. It must be experimentally determined according to the demand for the power consumption of the equipment in which the liquid crystal display is incorporated.

Generally, R is 1kΩ to 10kΩ, and VR is 5kΩ to 50kΩ. No capacitor is used. A capacitor of 0.1μF is usually used if necessary.

● Drive by Operational Amplifier

In graphic display, the size of liquid crystal becomes larger and the display duty ratio becomes smaller, then the stability of liquid crystal drive level is more important than small display system.

Since the liquid crystal for graphic display is large and has many picture elements, the load capacity becomes large. The high impedance of the power supply for liquid crystal drive produces distortion in the drive waveforms, and deteriorates display quality. For this reason, the liquid crystal drive level should be low impedance with operational amplifiers. Fig. 14 shows an example of operational amplifier configuration.

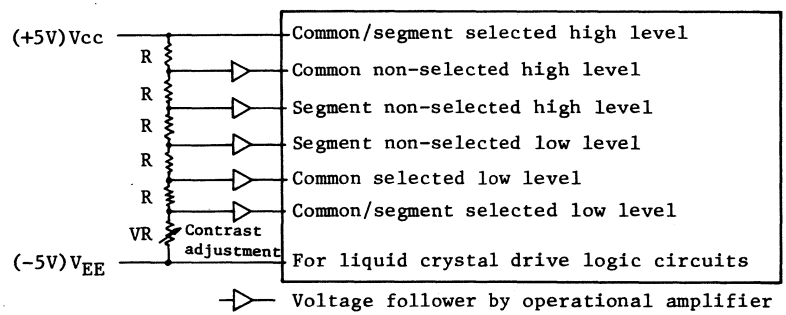


Fig. 14 Drive by Operational Amplifier (1/5 bias)

No load current flows through the dividing resistors because of the high input impedance of operational amplifier. A high resistance of R = 10kΩ and VR = 50kΩ can be used.

● Generation of Liquid Crystal Drive Level in LSI

The power supply circuit for liquid crystal drive level may be incorporated in the LSI such as for portable calculator with liquid crystal display.

HD61602, HD61603 for small display system has built-in power supply circuit for liquid crystal drive level.

● Precaution on Power Supply Circuit

The LCD driver LSI has two types of power supplies: the one for logical circuits and the other for liquid crystal display drive circuit. The power supply system is complicated because of several liquid crystal drive levels.

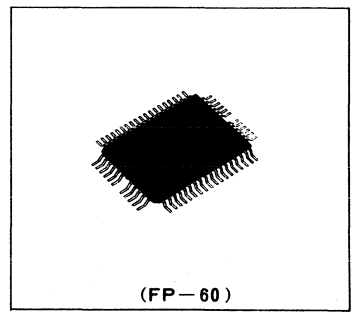
For this reason, in the power supply design, take care not to deviate from the voltage range assured in the maximum rating at the rise of power supply and from the potential sequence of each power supply. If the input terminal level is indefinite, through current flows and the power consumption increases because of the use of CMOS process in the LCD driver. Simultaneously, the potential sequence of each power supply becomes wrong, and a latch-up phenomenon may be caused.

Data Sheet

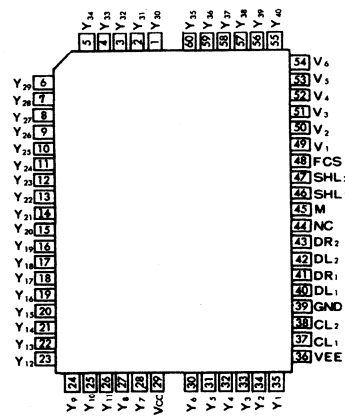
HD44100H
(LCD Driver with 40-Channel Outputs)

The HD44100H has two sets of 20-bit bidirectional shift registers, 20 data latch flip flops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

The HD44100H is a liquid crystal display driver with high generalizability, which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied to a common driver or segment driver.


(FP—60)

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830), LCD Ⅱ(HD44780), LCDⅢ (HD44790).
- Internal liquid crystal display driver ... 40 drivers
- Internal serial/parallel conversion circuits
  20-bit shift register × 2
  20-bit data latch × 2
- Display bias: Static ∿ 1/5

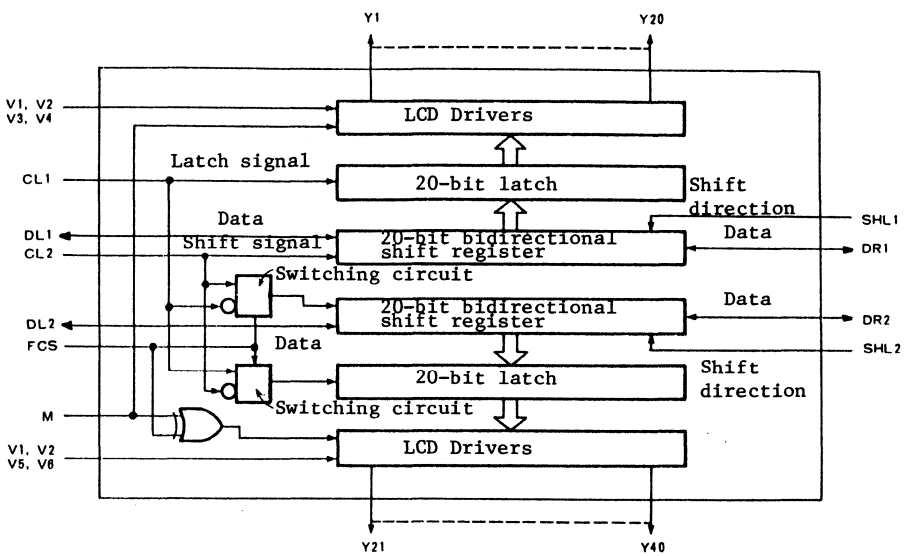
- Power supply

  Internal logic: +5V

  Liquid crystal display driver circuit: -5V

- The separation of internal logic from liquid crystal display driver circuit allows applicable controllers and liquid crystal types to increase.
- CMOS process
- 60-pin flat plastic package

■BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Value	Unit
Supply voltage	Logic	V_{CC} *1	- 0.3 to +7.0	V
	LCD drivers	V_{EE} *2	V_{CC} - 13.5 to V_{CC} +0.3	V
Input voltage		V_{T1} *1	- 0.3 to V_{CC} + 0.3	V
Input voltage		V_{T2} *3	V_{CC} +0.3 to V_{EE} -0.3	V
Operating temperature		T_{opr}	- 20 to +75	°C
Storage temperature		T_{stg}	-55 to +125	°C

*1 All voltage values are referred to GND.

*2 Connect a protection resistor of 220Ω ± 5% to V_{EE} power supply in series.

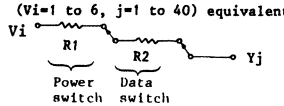
*3 Applies to V_1 to V_6

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, V_{EE} = -5V ± 10%, GND = 0V, Ta = -20 to + 75°C)

Item	Symbol	Applicable terminal	Test condition	min	typ	max	Unit
Input voltage	V_{IH}	CL1,CL2,DL1,DL2,DR1,DR2, M,SHL1,SHL2,FCS		0.7 V_{CC}	-	V_{CC}	V
	V_{IL}			0	-	0.3 V_{CC}	V
Output voltage	V_{OH}	DL1,DL2,DR1,DR2	I_{OH} = -0.4mA	V_{CC} - 0.4	-	-	V
	V_{OL}		I_{OL} = +0.4mA	-	-	0.4	V
Vi-Yj voltage descending	V_{D1}	*1	I_{ON} = 0.1mA for one of Yj	-	-	1.1	V
	V_{D2}		I_{ON} = 0.05mA for each Yj	-	-	1.5	V
Input leakage current	I_{IL}	CL1,CL2,DL1,DL2,DR1,DR2, M,SHL1,SHL2,FCS,NC	Vin = 0 to V_{CC}	-5.0	-	5.0	μA
Vi leakage current	I_{VL}	*3	V_{in} = V_{CC} to V_{EE}	-10.0	-	10.0	μA
Power supply current	ICC	*2	f_{CL2} = 400kHz	-	-	1.0	mA
	IEE		f_{CL1} = 1kHz	-	-	10	μA

*1 Vi - Yj (Vi=1 to 6, j=1 to 40) equivalent circuit



R1= 1kΩ max.
R2=10kΩ max.

*2 Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

*3 Output Y1 to Y40 open.

■ TIMING CHARACTERISTICS
(V_{CC} = 5V ± 10%, V_{EE} = -5 ± 10%, GND = 0V, Ta = -20 to + 75°C)

Item		Symbol	Applicable terminal	Test condition	min	typ	max	Unit
Data shift frequency		f_{CL}	CL2		-	-	400	kHz
Clock width	High level	t_{CWH}	CL1,CL2		800	-	-	ns
	Low level	t_{CWL}	CL2		800	-	-	ns
Data set-up time		t_{SU}	DL1,DL2,DR1,DR2,FLM		300	-	-	ns
Clock set-up time		t_{SL}	CL1,CL2	(CL2→CL1)	500	-	-	ns
Clock set-up time		t_{LS}	CL1,CL2	(CL1→CL2)	500	-	-	ns
Data delay time		tpd	DL1,DL2,DR1,DR2	C_L = 15 pF	-	-	500	ns
Clock rise/fall time		tct	CL1,CL2		-	-	200	ns
Data Hold time		t_{DH}	DL1,DL2,DR1,DR2,FLM		300	-	-	ns

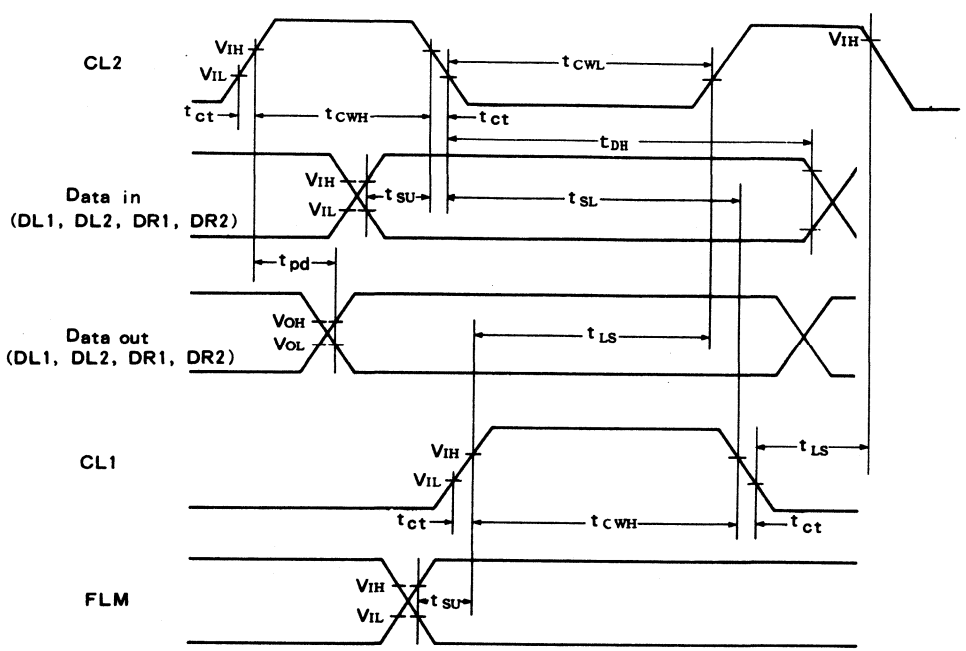


Fig. 1 Timing Waveform

■TERMINAL FUNCTION

Table 1 Fucntional Description of Terminals

Signal name	Number of lines	Input/ Output	Connected to	Function
V_{CC}	1		Power supply	Power supply for logical circuit
GND	1		Power supply	0V
V_{EE}	1		Power supply	Power supply for liquid crystal display drive
$Y_1 \sim Y_{20}$	20	Output	Liquid crystal	Liquid crystal driver output (Channel 1)
$Y_{21} \sim Y_{40}$	20	Output	Liquid crystal	Liquid crystal driver output (Channel 2)
V_1, V_2	2	Input	Power supply	Power supply for liquid crystal display drive (Select level)
V_3, V_4	2	Input	Power supply	Power supply for liquid crystal dispaly drive (Non-select level for channel 1)
V_5, V_6	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 2)
SHL1	1	Input	V_{CC} or GND	Selection of the shift direction of channel 1 shift register SHL1 / DL1 / DR1 V_{CC} / OUT / IN GND / IN / OUT
SHL2	1	Input	V_{CC} or GND	Selection of the shift direction of channel 2 shift register SHL2 / DL2 / DR2 V_{CC} / OUT / IN GND / IN / OUT
DL1, DR1	2	Input/ output	Controller or HD44100H	Data input/output of channel 1 shift register
DL2, DR2	2	Input/ output	Controller or HD44100H	Data input/output of channel 2 shift register
M	1	Input	Controller	Alternated signal for liquid crystal driver output
CL1	1	Input	Controller	Latch signal for channel 1 (⌐L) *1 This is used for channel 2 when FCS is GND.
CL2	1	Input	Controller	Shift signal for channel 1 (⌐L) *1 This is used for channel 2 when FCS is GND.
FCS	1	Input	V_{CC} or GND	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2. Thus, this signal exchanges the purpose of channel 2.
NC	1			Don't connect any wires to this terminal.

FCS level	Channel 2		M polarity	Purpose
	Latch signal	Shift signal		
V_{CC}	CL2 ⌐	CL1 ⌐	$\overline{M}$	For common drive
GND	CL1 ⌐	CL2 ⌐	M	For segment drive
	*1	*1		*2

*1 ⌐ and ⌐ indicate the latches at rise and fall times respectively.

*2 The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

FCS	Data	M	Output level	
			Channel 1 ($Y_1 \sim Y_{20}$)	Channel 2 ($Y_{21} \sim Y_{40}$)
V_{CC} ("1")	"1" (Select)	"1"	V_1	V_2
		"0"	V_2	V_1
	"0" (Non-select)	"1"	V_3	V_6
		"0"	V_4	V_5
GND ("0")	"1" (Select)	"1"	V_1	V_1
		"0"	V_2	V_2
	"0" (Non-select)	"1"	V_3	V_5
		"0"	V_4	V_6

"1" and "0" indicate a high and low levels, respectively.

■ APPLICATIONS

• Segment Driver

When the HD44100H is used as a segment driver, the FCS is set to GND to transfer display data in the timing shown in Fig. 2. In this case, both of channel 1 and channel 2 shift data at the fall of CL2 and latch it at the fall of CL1. V_3 and V_5, V_4 and V_6 of power supply for liquid crystal display driver are short-circuited respectively.

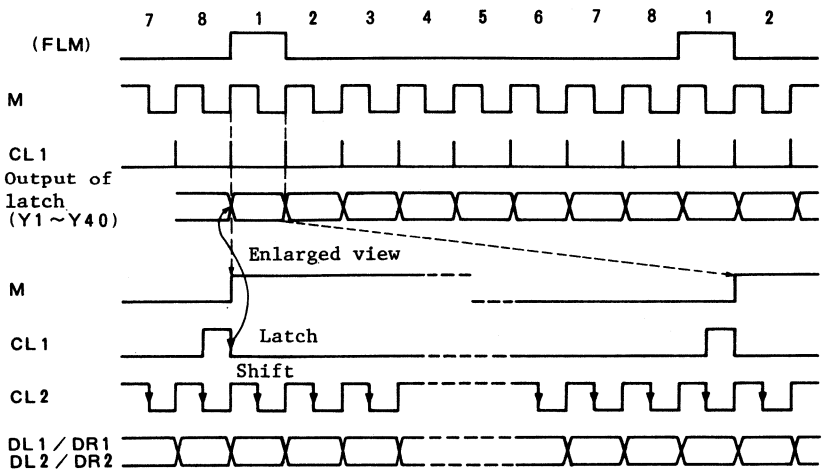


Fig. 2 Segment Data Waveforms (A type waveforms 1/8 duty)

● Common Driver

When channel 1 is used as a segment driver and channel 2 as a common driver.

When channel 2 of HD44100H is used as a common driver, the FCS is set to V_{CC} level to transfer display data in the timing shown in Fig. 3.

In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 shifts and latches as shown in Fig. 2.

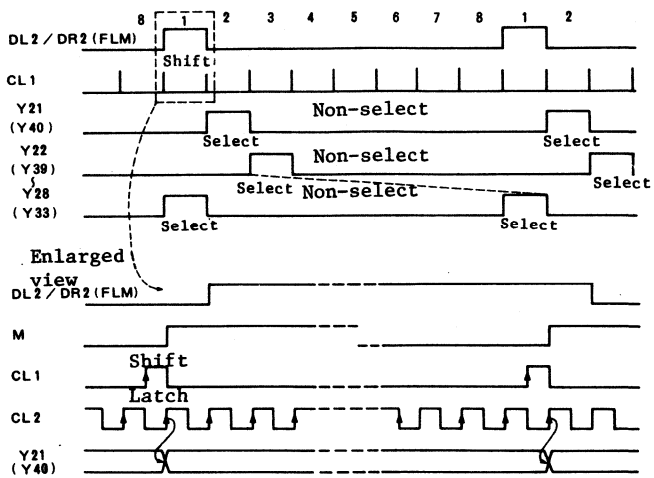


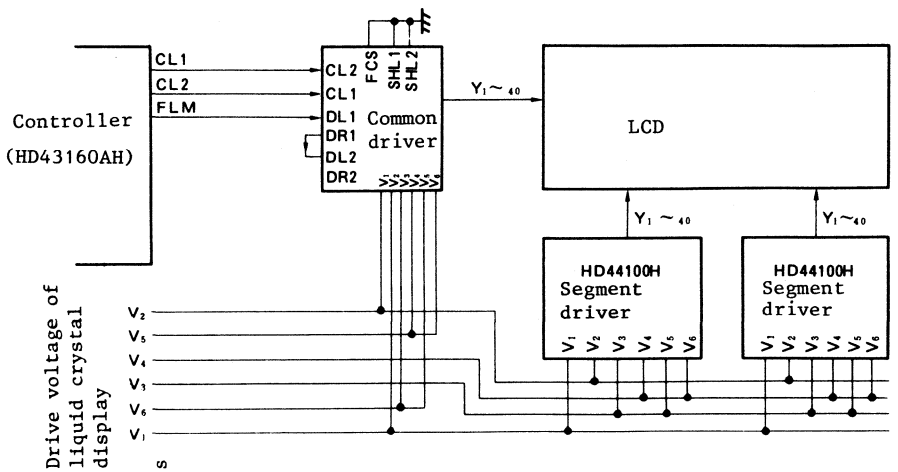
Fig. 3 Common Data Waveforms (A type waveforms of channel 2, 1/8 duty)

- When both Channel 1 and Channel 2 used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100H are used a common driver, the FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected as shown in following figure.

In this case, connection of power supply for liquid crystal display driver is different from that of segment driver, so refer to following figure.

V_1, V_2 ..... Select level of segment and common
V_3, V_4 ..... Non-select level of segment
V_5, V_6 ..... Non-select level of common

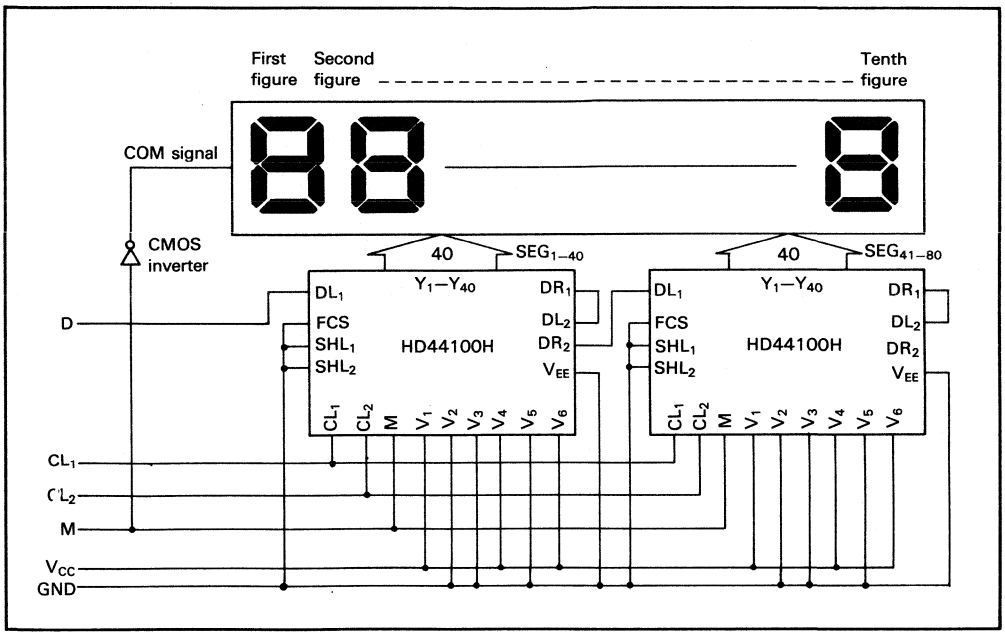


- Static Drive

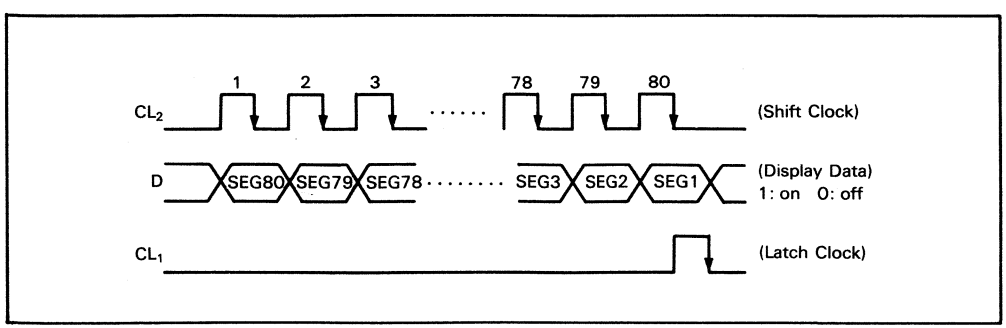
When the HD44100H is used in the static drive, data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of liquid crystal display driver. The signal applied into terminal M must be one that has the frequency twice that of CL1 and is synchronized at the fall of CL1. The power supply for liquid crystal display driver is used by short-circuiting three of V_1, V_4 and V_6, and three of V_2, V_3 and V_5 respectively.

One of liquid crystal display driver output terminals can be used for a common output. In this case, the FCS is set to GND and data is transferred so that "0" can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is "1", the segments of LCD light. They also light with common side = "1", and segment side "0".

Static Drive

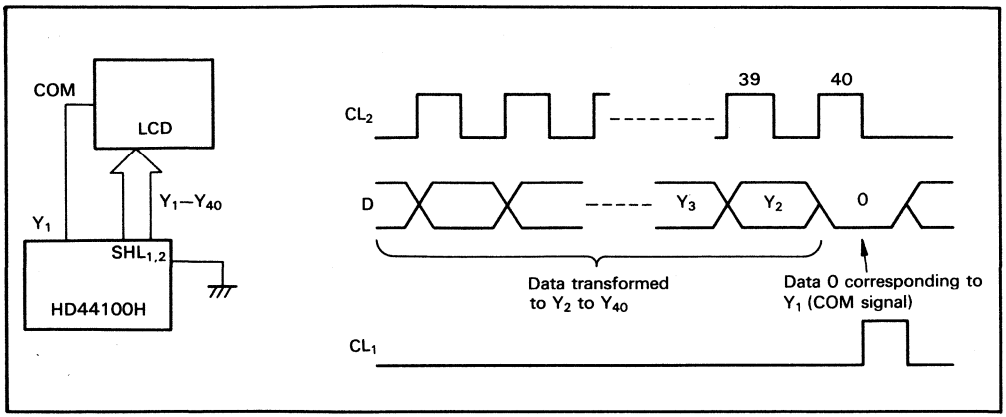


Timing Chart of Input Waveforms



Notes:

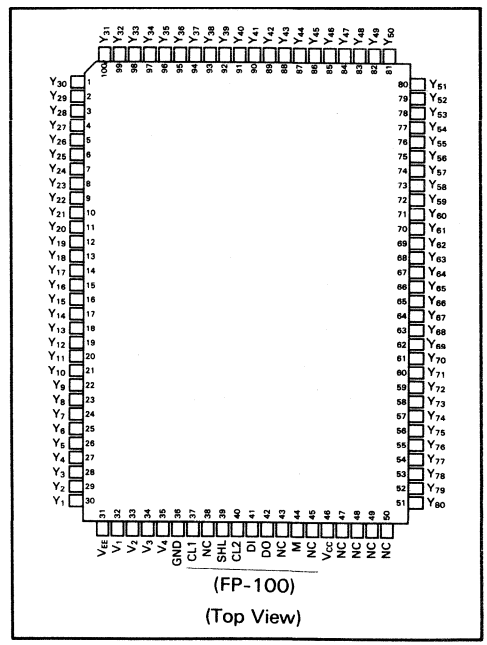
1. Input square waves of 50% duty (about 30-500 Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data output at the fall of CL1. Therefore, when the alternating signal M and CL1 donot fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g.display of hours, minutes, and seconds of a clock). To avoid it, set CL1 falling synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of a large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD44100H outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.


COM
LCD
Y_1–Y_{40}
Y_1
$SHL_{1,2}$
HD44100H
CL_2
39
40
D
Y_3
Y_2
0
Data transformed to Y_2 to Y_{40}
Data 0 corresponding to Y_1 (COM signal)
CL_1

HD66100

(LCD Driver with 80-Channel Outputs)

The HD66100 is a segment driver with 80 LCD drive circuits and is the improved version of the current LCD driver HD44100H with 40 circuits.
It is composed of a shift register, a 80-bit latch circuit, and 80 LCD drive circuits. Its interface is compatible with the HD44100H.
It enables lessening the number of LSI's and lowering cost of a LCD module.



Features

- LCD driver with serial/parallel converting function
- Interface compatible with the HD44100H; connectable with HD43160AH, HD61830, HD61830B, LCD-II (HD44780), LCD-III (HD44790)
- Internal output circuits for LCD drive-80
- Internal serial/parallel converting circuits;
  - 80-bit bidirectional shift register
  - 80-bit latch circuit
- Power supply
  Internal logic circuit; +5 V ±10%
  LCD drive circuit; 3.0 V to 6.0 V
- CMOS process
- 100-pin plastic QFP (FP-100)

Comparison with HD44100H

Table 1 shows the main differences between HD66100 and HD44100H.

Table 1. Comparison of HD66100 and HD44100H

	HD66100	HD44100H
LCD Drive Outputs	80×1 Channel	20×2 channels
Supply Voltage for LCD Drive Circuits	3 to 6V	4.5 to 11V
Multiplexing Duty Ratio	Static to 1/16 duty	static to 1/32 duty
Package	100-pin flat Plastic package	60-pin flat plastic package

Pin Description

V_{CC}, GND, V_{EE}: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground. V_{EE} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1 to V_4 supply power for driving an LCD (figure 2).

CL1: Latches data at the negative adge of CL1.

CL2: Receives shift data at the negative edge of CL2.

M: Changes LCD drive outputs to AC.

DI: Receives data of the shift register.

DO: Output data of the shift register.

SHL: Selects a shift direction of serial data. When the serial data is input in order of D_1, D_2 .....D_{79}, D_{80}, the relation between the data and the output Y is as table 3.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels-V_1, V_2, V_3, or V_4-according to the combination of M and display data (figure 2).

NC: Do not connect any wire with these terminals.

Table 2. Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	46	V_{CC}	–
GND	36	Ground	–
V_{EE}	31	V_{EE}	–
V_1	32	V_1	–
V_2	33	V_2	–
V_3	34	V_3	–
V_4	35	V_4	–
CL1	37	Clock 1	I
CL2	40	Clock 2	I
M	44	M	I
DI	41	Date In	I
DO	42	Date Out	O
SHL	39	Shift Left	I
Y_1-Y_{80}	1-30,51-100	Y_1-Y_{80}	O
NC	38,43,45,47-50	Non Connection	–

Table 3. Relation Between SHL and Data Output

SHL	Y_1	Y_2	Y_3....Y_{79}	Y_{80}
High	D1	D2	D3..... D79	D80
Low	D80	D79	D78..... D2	D1

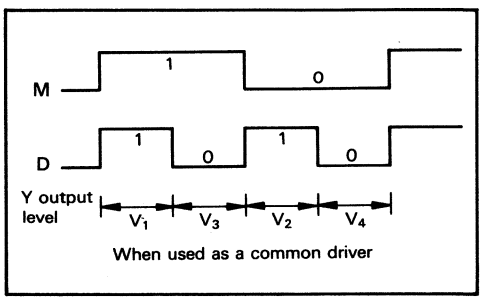


Figure 1. Selection of LCD Drive Output

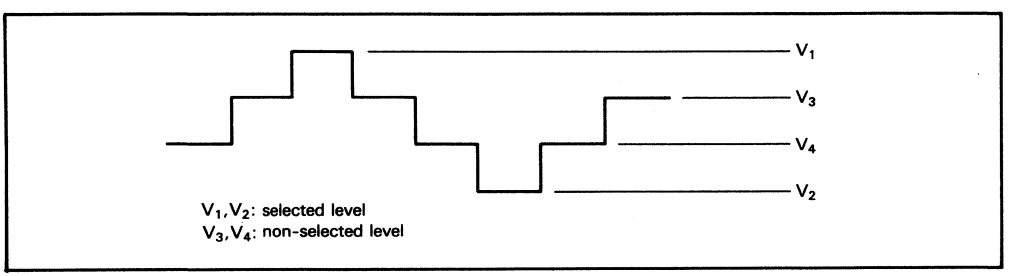


Figure 2. Power Supply for Driving an LCD

Block Functions

LCD Drive Circuits

These circuits select one of four levels of voltage V_1, V_2, V_3, and V_4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

Latch Circuit

This circuit latches the data input from the bidirectional shift register at the fall of CL1 and transfer its outputs to the LCD drive circuits.

Bidirectional Shift Reigster

This register shifts the serial data at the fall of CL2 and transfer the output of each bit of the register to the latch circuit. When SHL = GND, the data input from DI shifts from the bit 1 to the bit 80 in order of entry. On the contrary, when SHL = V_{CC}, the data shifts from the bit 80 to the bit 1. In both cases, the data of the last bit of the register is latched to be output from DO at the rise of CL2.

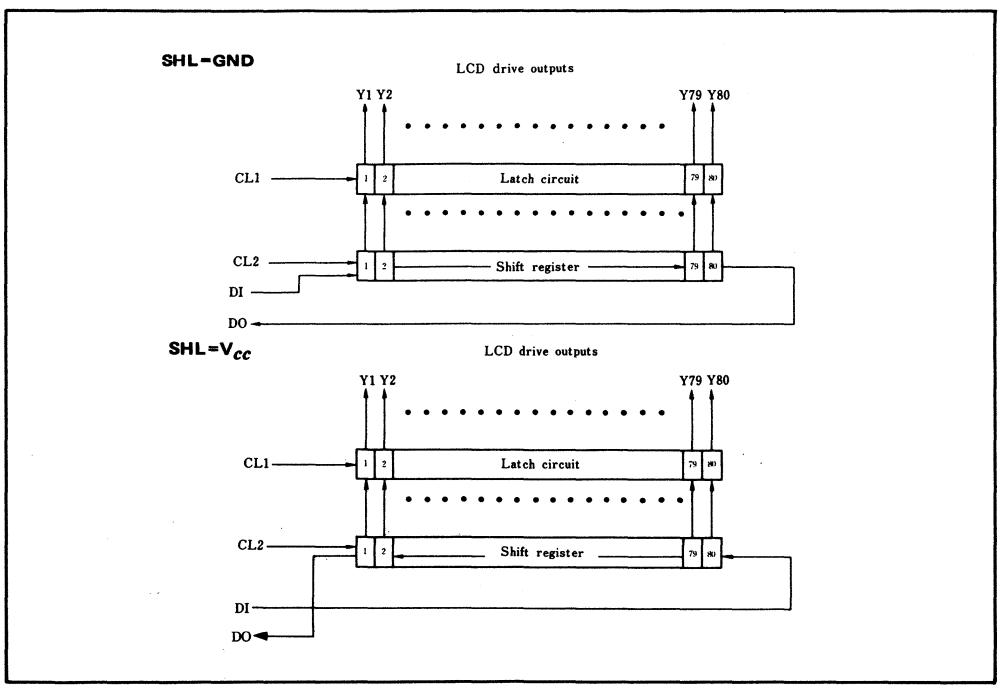


Figure 3. Relation between SHL and the Shift Direction

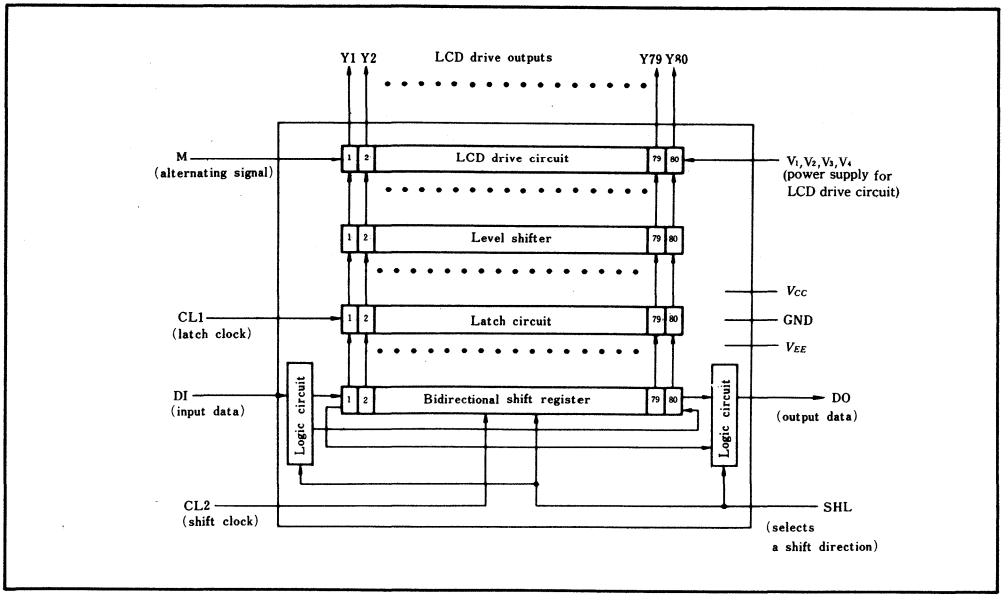


Figure 4. Block Diagram

Primary Operations

Shifting Data

The input data DI shifts at the fall of CL2 and the data delayed 80 bits by the shift register outputs from the DO terminal. The output of DO changes synchronously with the rise of CL2. This operation is completely unaffected by the latch clock CL1.

Latching Data

The data of the shift register is latched at the negative edge of the latch clock CL1. Thus, the outputs Y_1-Y_{80} change synchronously with the fall of CL1.

Switching Data Shift Direction

When the shift direction switching signal SHL is connected with GND, the data D80, immediately before the negative edge of CL1, outputs from the output terminal Y_1 and when SHL is connected with V_{CC}, it outputs from Y_{80}.

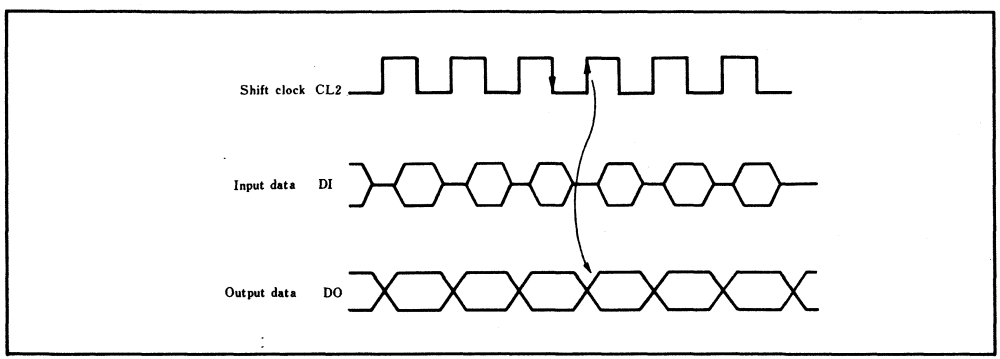


Figure 5. Timing of Receiving and Outputting Data

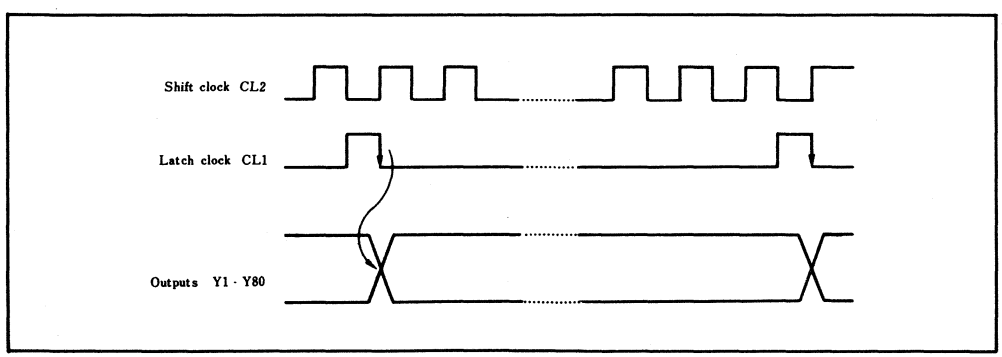


Figure 6. Timing of Latching Data

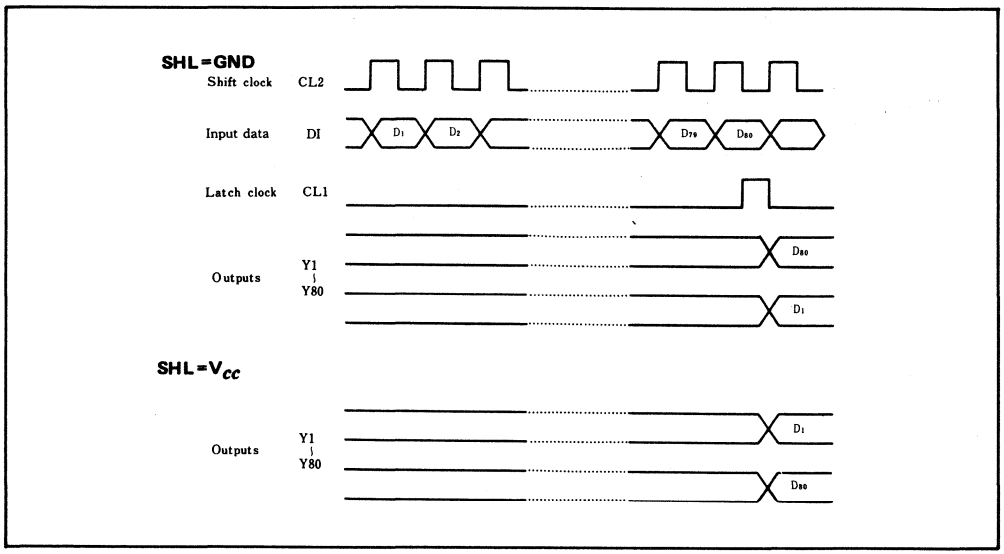


Figure 7. SHL and Waveforms of Data Shift

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Supply Voltage	Logic Circuits	V_{CC}	−0.3 to +7.0	V	*1
	LCD Drive Circuits	V_{CC}-V_{EE}	−0.3 to +7.0	V	
Input Voltage (1)		V_{T1}	−0.3 to V_{CC}+0.3	V	*1
Input Voltage (2)		V_{T2}	V_{CC}+0.3 to V_{EE}−0.3	V	*2
Operation Temperature		T_{opr}	+20 to +75	°C	
Storage Temperature		T_{stg}	−55 to +125	°C	

*1 A reference point is GND (=0V.)
*2 Applies to $V_1 - V_4$.
Note) If used beyond the absolute maximum ratings, LSI's may be permanently destroyed. It is desired to use ones on the electrical characteristics for normal operations, and if not used on these conditions, it may affect the reliability of the device.

Electrical Characteristics

1. DC Characteristics
(V_{CC}=5V±10%, V_{CC}-V_{EE}=3.0 to 6.0V, GND=0V, T_a=−20 to +75°C)

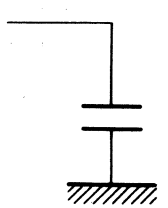
Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Test condition	Note
Input High Voltage	V_{IH}	CL1,CL2	0.8×V_{CC}	–	V_{CC}	V		
Input Low Voltage	V_{IL}	M,DI,SHL	0	–	0.2×V_{CC}	V		
Output High Voltage	V_{OH}	DO	V_{CC}-0.4	–	–	V	I_{OH}=-0.4mA	
Output Low Voltage	V_{OL}		–	–	0.4	V	I_{OL}=+0.4mA	
ON Resistance Vi-Vj	R_{ON1}	Y_1-Y_{80}	–	–	11	kΩ	I_{ON}=0.1mA to one of Y terminals	
	R_{ON2}	V_1-V_4	–	–	30	kΩ	I_{ON}=0.05mA to each Y terminal	
Input Leakage Current	I_{IL}	CL1, CL2, M, DI, SHL	−5.0	–	5.0	μA	V_{in}=0V to V_{CC}	
Vi Leakage Current	I_{VL}	V_1-V_4	−5.0	–	5.0	μA	Output Y_1-Y_{80} open V_{in}=V_{CC} to V_{EE}	
Current Dissipation	I_{GND}		–	–	2.0	mA	f_{CL2}=1.0MHz	*1
	I_{EE}		–	–	0.1	mA	f_{CL1}=2.5kHz	

*1 Input/output currents are excluded; when an input is at the intermediate level in CMOS, the excessive current flows from the power supply through the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed at V_{CC} and GND level respectively.

2. AC Characteristics
(V_{CC}=5V±10%, V_{CC}-V_{EE}=3.0 to 6.0V, GND=0V, T_a=−20 to +75°C)

Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Note
Data Shift Frequency	f_{CL}	CL2	–	–	1	MHz	
Clock High level Width	t_{CWH}	CL1,CL2	450	–	–	ns	
Clock Low level Width	t_{CWL}	CL2	450	–	–	ns	
Data Set-up Time	f_{SU}	DI	100	–	–	ns	
Clock Set-up Time (1)	t_{SL}	CL2	200	–	–	ns	*1
Clock Set-up Time (2)	t_{LS}	CL1	200	–	–	ns	*2
Output Delay Time	t_{pd}	DO	–	–	250	ns	*3
Data Hold Time	t_{DH}	DI	100	–	–	ns	
Clock Rise/Fall Time	f_{CT}	CL1,CL2	–	–	50	ns	

*1 Set-up time from the fall of CL2 to that of CL1.
*2 Set-up time from the fall CL1 to that of CL2.
*3 Test terminal



C_L (Load capacitance on outputs)=30pF
(Including jig capacitance)

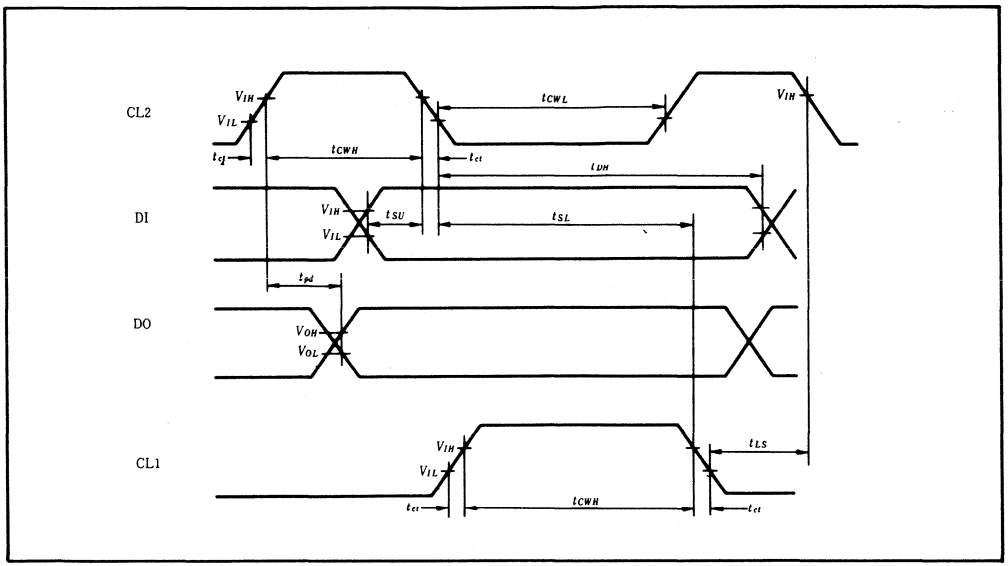


Figure 8. Timing Chart of HD66100F

Typical Applications

1. Connection with the LCD Controller HD44780

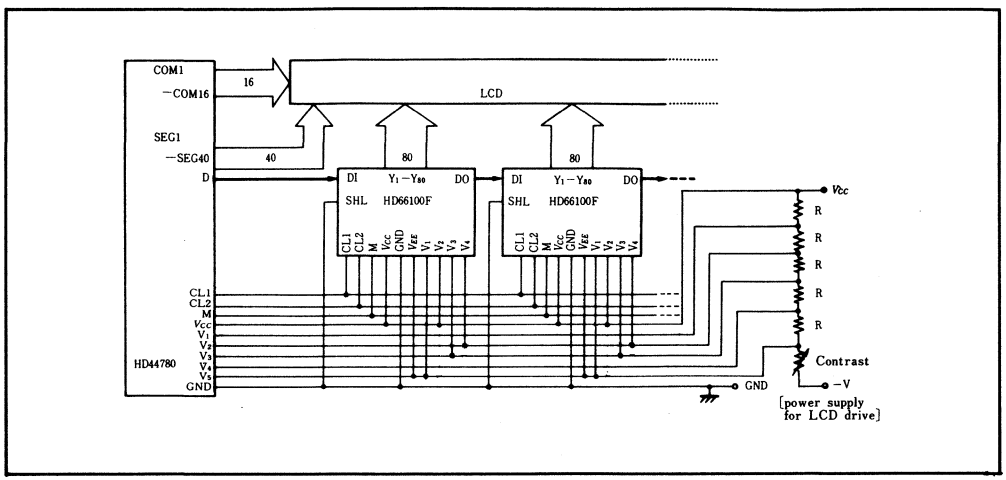


Figure 9. Example of Connection (1/16 duty, 1/5bias)

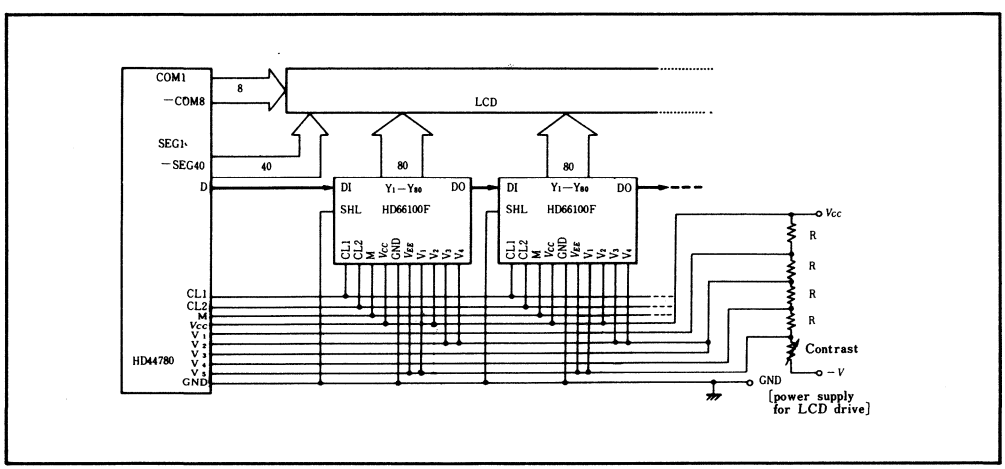


Figure 10. Example of Connection (1/8 duty, 1/4bias)

2. Connection with LCD III (HD44790)

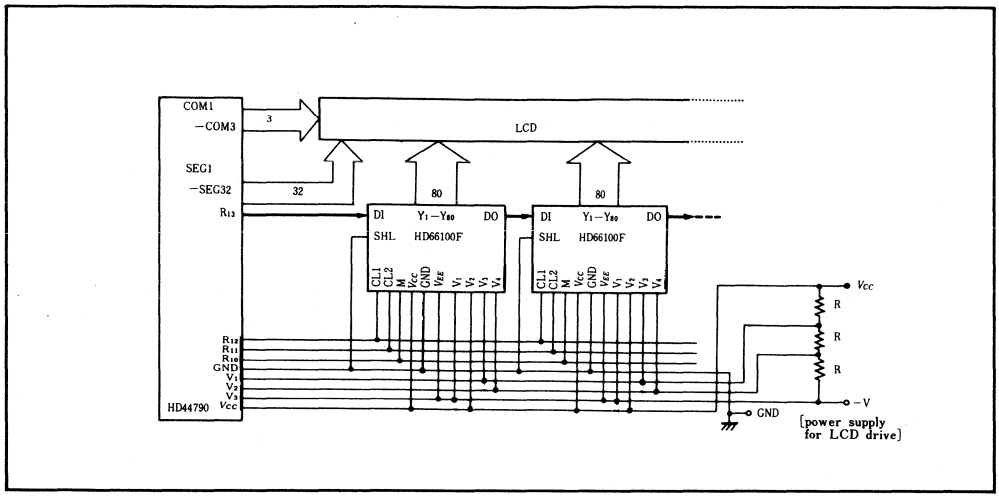


Figure 11. Example of Connection (1/3 duty, 1/3bias)

3. Static Drive

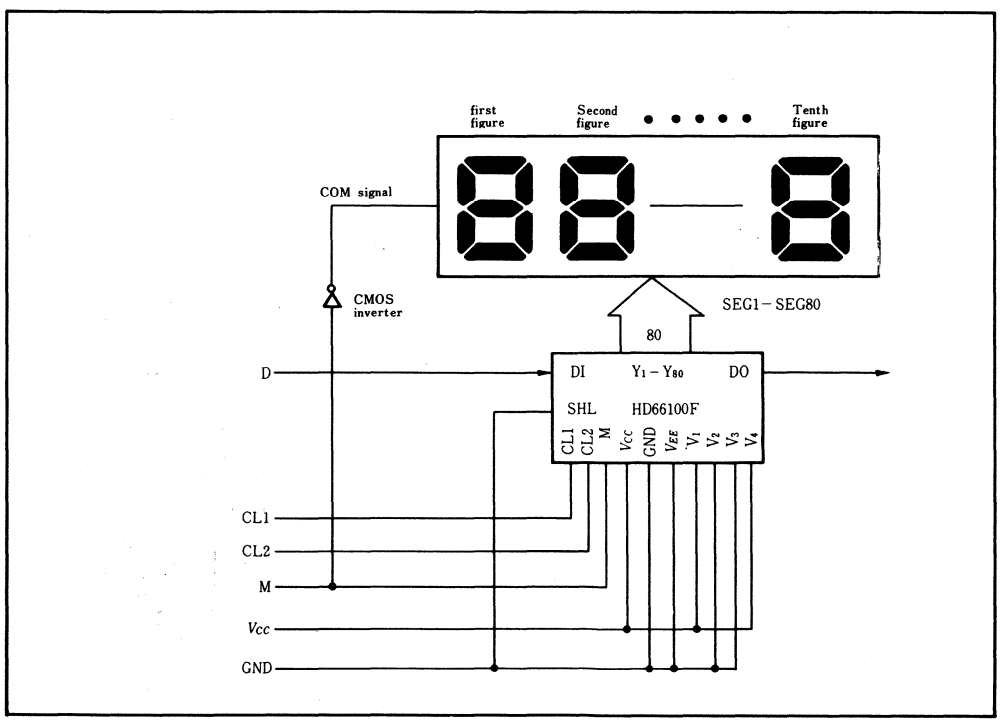


Figure 12. Example of Connection (80-segment display)

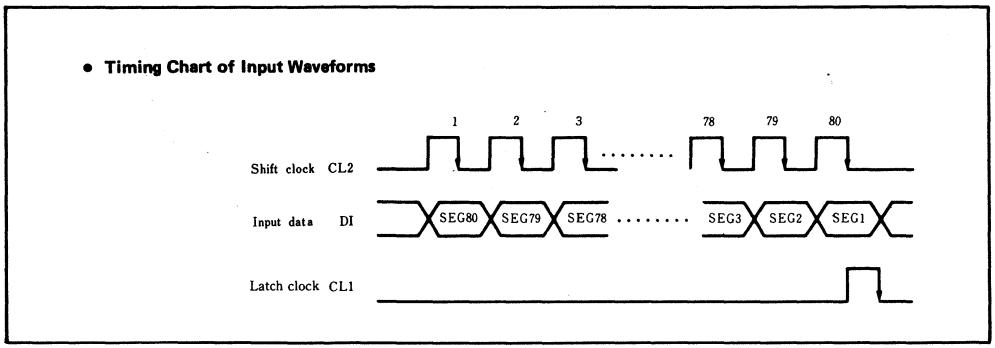


Figure 13. Timing Chart of Input Waveforms

Notes

(a) Input square waves of 50% duty (about 30-500Hz) to M. The frequency depends on the specifications of LCD panels.

(b) The drive waveforms corresponding to the new displayed data output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid it, set CL1 falling synchronously with the one edge of M.

(C) In this example, the CMOS inverter is used as a COM signal driver in consideration of a large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
Usually, one of the HD66100F outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

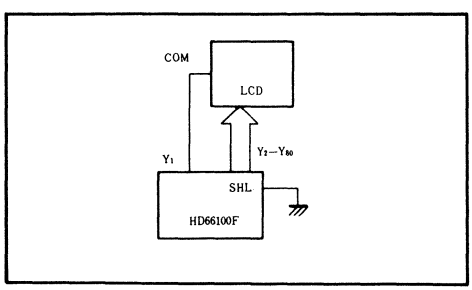


Figure 14. Example of Connection

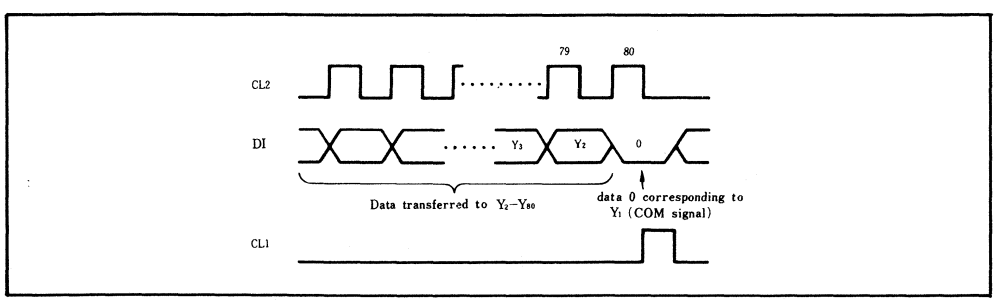


Figure 15. Timing Chart (When Y_1 is used as a COM signal)

HD43160AH
(Controller with Built-in Character Generator)

DISPLAY CONTROLLER AND CHARACTER GENERATOR
FOR DOT MATRIX LIQUID CRYSTAL DISPLAY SYSTEM

The HD43160AH receives character data written in the ASCII code or JIS code from microcomputer and stores them in its RAM which has 80 words capacity.

The HD43160AH converts these data into serial character pattern, then transfers them to LCD drivers.

It also generates other control signals for LCD. Available LCD driver for combination with this is HD44100H.

(FP-54)

■ SORTS OF DISPLAY CHARACTERS

- Alphanumeric character; A ~ Z, a ~ z, @, #, %, &, etc.
- Japanese Character (katakana)
- 160 characters by internal character generator (ROM). (Max 256 characters by external ROM)

■ NUMBER OF CHARACTERS

- 4, 8, 16, 24, 32, 40, 64 or 80 characters in 1 or 2 lines

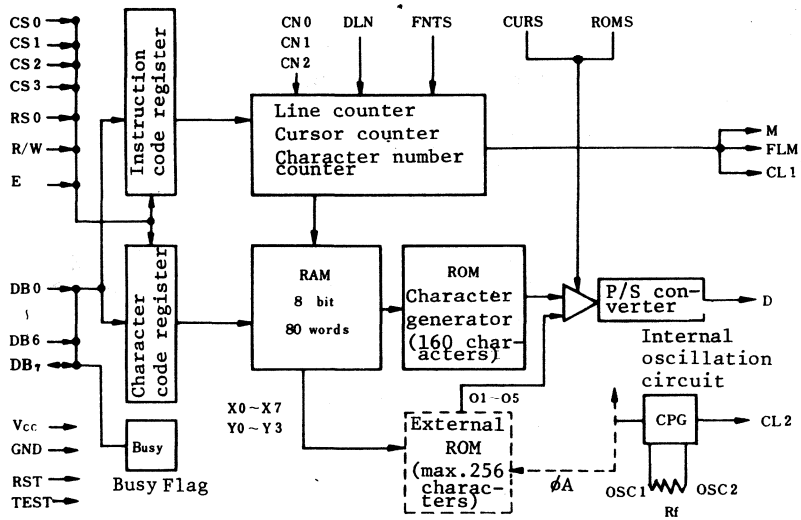
■ FONT

- 5 × 7 + Cursor or 5 × 11 + Cursor

■ OTHER FUNCTION CONTROLLED BY MICROCOMPUTER

- Display clear
- Cursor ON/OFF
- Cursor position preset (Character position)
- Cursor return

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_T	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, GND=0V, Ta=-20 to +75°C)

Item	Symbol	Terminal No.	Test condition	min	typ	max	Unit
Input voltage (TTL compatible)	V_{IH}	CS0 ~ CS3, E, R/W, DB0 ~ DB7, RS0		2.0	-	V_{CC}	V
	V_{IL}			0	-	0.8	V
Input voltage	V_{IHC}	OSC1, TEST, RST, FNTS, CURS, DLN, ROMS, CN0 ~ CN2, O_1 ~ O_5		0.7 V_{CC}	-	V_{cc}	V
	V_{ILC}			0	-	0.3 V_{CC}	V
Output voltage (TTL compatible)	V_{OH}	DB7	I_{OH}=-0.205mA	2.4	-	-	V
	V_{OL}		I_{OL}=1.6mA	-	-	0.4	V
Output voltage	V_{OHC}	FLM, M, D, CL1, CL2, X0 ~ X7, Y0 ~ Y3	I_{load}=±0.4mA	V_{CC}-1.0	-	-	V
	V_{OLC}			-	-	1.0	V
Input leak current	I_{in}	All inputs		-5	-	5	μA
Output leak current	I_{LO}	DB7		-10	-	10	μA
Oscillation frequency	f_{CP1}		R_f=200kΩ±2%, 5×7+Cursor	130	192	250	kHz
	f_{CP2}		R_f=130kΩ±2%, 5×11+Cursor	200	288	375	kHz
Input pull up current	I_{PL}	CS0 ~ CS3, RS0, R/W, DB0 ~ DB7	V_{in}=0V	2	10	20	μA
Power dissipation	P_T	*	Ta=25c, f_{CP}=400kHz (external clock)	-	-	10	mW

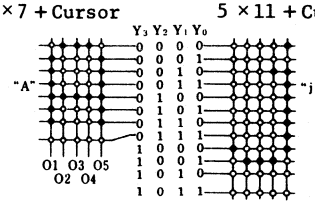
* Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low, but CS0 ~ CS3, RS0, R/W, DB0 ~ DB7 are excluded.

■ PIN ARRANGEMENT

Pin No.	Power sup. OSC.	Input	Output	Pin No.	Power sup. OSC.	Input	Output	Pin No.	Power sup. OSC.	Input	Output
1	GND (-)			19			D	37		DB3	
2			X4	20			FLM	38		DB4	
3			X3	21			φA	39		DB5	
4			X2	22	OSC1			40		DB6	
5			X1	23	OSC2			41		DB7	DB7
6			X0	24		RST		42		ROMS	
7		N.C.		25		TEST		43		O5	
8		N.C.		26		E		44		O4	
9		N.C.		27	V_{CC}(+)			45		O3	
10		CURS		28		R/W		46		O2	
11		FNTS		29		RS0		47		O1	
12		DLN		30		CS0		48			Y3
13		CN0		31		CS1		49			Y2
14		CN1		32		CS2		50			Y1
15		CN2		33		CS3		51			Y0
16			CL2	34		DB0		52			X7
17			CL1	35		DB1		53			X6
18			M	36		DB2		54			X5

■ PIN FUNCTION

Pin name	Number of terminals	Connected to	I/O	Function
V_{CC} GND	2	Power supply		+5V ± 10% Power supply 0V
CN0 CN1 CN2	3	GND or V_{CC}	I	Total displayed character number select. No. 4 8 16 24 32 40 64 80 CN0 GND V_{CC} GND V_{CC} GND V_{CC} GND V_{CC} CN1 GND GND V_{CC} V_{CC} GND GND V_{CC} V_{CC} CN2 GND GND GND GND V_{CC} V_{CC} V_{CC} V_{CC}
CURS	1	GND or V_{CC}	I	Cursor select V_{CC}: 5 dots. ●●●●● GND: 1 dot. ●
DLN	1	GND or V_{CC}	I	Display line number select. V_{CC}: 2 lines. GND: 1 line.
FNTS	1	GND or V_{CC}	I	Font select. V_{CC}: 5 ×11 + Cursor. GND: 5 ×7 + Cursor.
RST	1	V_{CC}	I	Only for test. Normally V_{CC}
TEST	1	GND	I	Only for test. Normally GND
E	1	MPU	I	Strobe signal. Write mode: The HD43160AH latches the data on DB0 ~ DB7 at the falling edge of this signal. Read mode: Busy/Ready signal is active on DB7 while this signal is 'H'. (L:Ready, H:Busy)
R/W	1	MPU	I	Read/Write signal L: HD43160AH gets the data from MPU. H: MPU gets the Busy/Ready signal from HD43160AH.
CS0 CS1 CS2 CS3	4	MPU	I	Chip select When all of CS0 ~ CS3 are 'H', HD43160AH is selected.
RS0	1	MPU	I	Register select. HD43160AH has 2 registers. One is for Character code and another is for instruction code. Each register latches the data on DB0 ~ DB7 at the falling edge of 'E', when CS0 ~ CS3 are 'H' and R/W is 'L'. H; Character code register is selected. L; Instruction code register is selected.
DB0 ~ DB7	8	MPU	I I/O (DB7)	Data bus. Inputs for Character code and Instruction code from MPU. Output for Busy/Ready flag (DB7).
D	1	HD44100H	O	Serial dot data of characters for LCD drivers
CL2	1	HD44100H	O	Dot data shift signal for LCD drivers.
CL1	1	HD44100H	O	Dot data latch signal for LCD drivers.

M	1	HD44100H	O	Alternate signal for LCD drivers.
FLM	1	HD44100H	O	Signal for common plates scanning.
XO 〜 X7	8	ROM	O	Character code outputs for External character generator. (for Ext ROM) X7: MSB XO: LSB ex: character 'A' MSB 0 1 0 0 0 0 0 LSB 1 '1'='H' '0'='L'
YO Y1 Y2 Y3	4	ROM	O	Character row code for External character generator. 5 × 7 + Cursor 5 × 11 + Cursor 
φA	1	ROM	O	Clock signal for External character generator (dynamic ROM etc.) if necessary.
O1 〜 O5	5	ROM	I	Dot data inputs from External character generator. 1(H): ON 0(L): OFF
ROMS	1	GND or V_{CC}	I	Select Internal or External ROM. H: External ROM L: Internal ROM
OSC1 OSC2	2		(I) (O)	Oscillator. 5 × 7 + Cursor : R_f=200kΩ (typ) 5 × 11 + Cursor: R_f=130kΩ (typ)
NC	3			Don't connect any wire to these terminals.

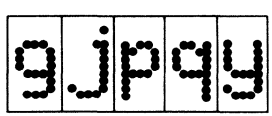
■ CHARACTER DOT PATTERNS

- 5 × 7

The bottom lines of the English small characters "g, i, p, q, y," are on the cursor line.

- 5 × 11

Only English small character "g, j, p, q, y," are displayed as below, the others are in the same way as that of 5 × 7.



- Cursor 5 dots: ●●●●●

  1 dot : ●

The cursor is displayed on the 8th or 12th line.

■ APPLICATION

• Setting Up

a) Total character number ..... (CN0 ~ CN2)

b) Cursor pattern ..... (CURS)

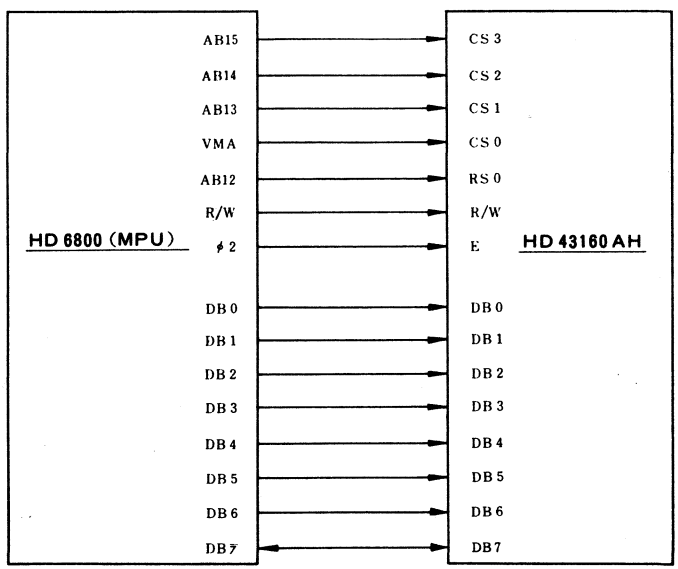
c) Display line number ..... (DLN)

d) Font ..... (FNTS)

These terminals should be connected to V_{CC} or GND according to the LCD display system. RST and TEST should be connected to V_{CC} and GND respectively.

• Interface to the Controller

a) Example 1 Interface to HD6800

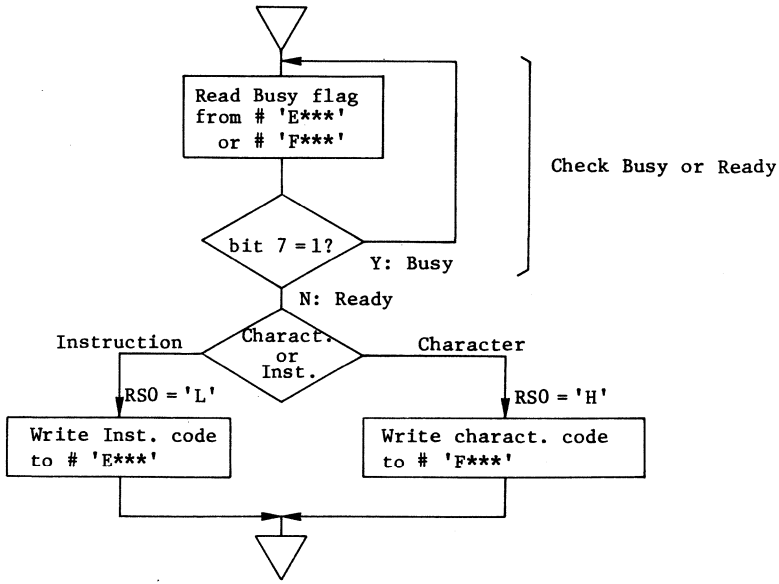


In this example, the addresses of HD43160AH in the address area of the HD6800 microcomputer are

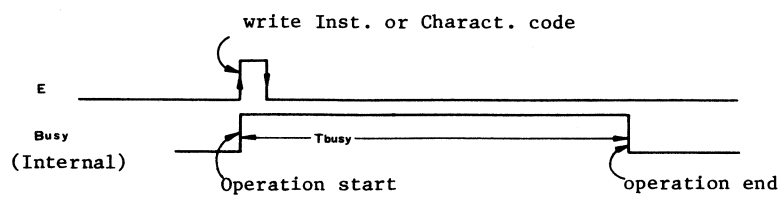
Instruction code register	#'E***'	(R/W=0)
Character code register	#'F***'	(R/W=0)
Busy flag	#'E***' or #'F***'	(R/W=1).

*: don't care
#'': hexadecimal

b) Example of display program



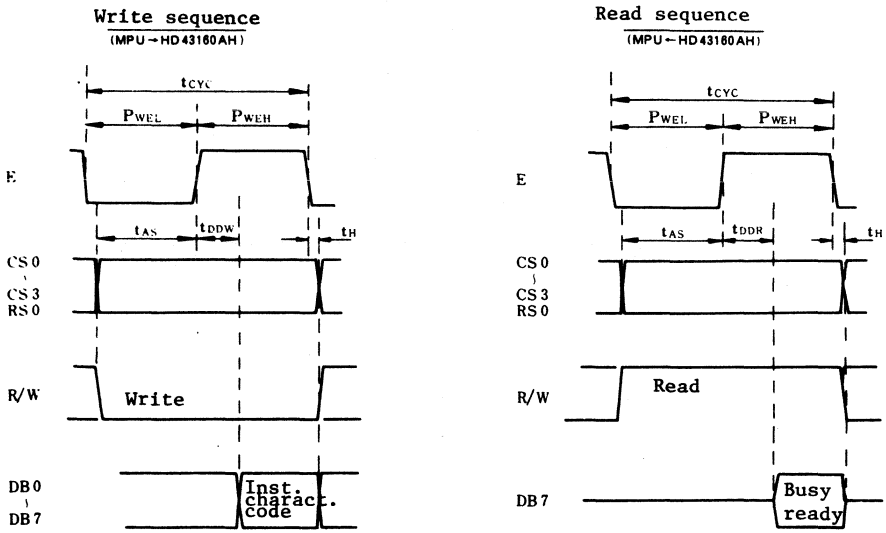
c) Time length of Busy



	T busy		
	MIN	MAX	Unit
Display clear	$\frac{400}{f_{cp}}$	$\frac{410}{f_{cp}}$	sec
Other function	$\frac{10}{f_{cp}}$	$\frac{20}{f_{cp}}$	sec

HD43160AH begins the operation from the rising edge of 'E'.
Instruction code register and Character code register latch the data on DB0 ~ DB7 at the falling edge of 'E'.

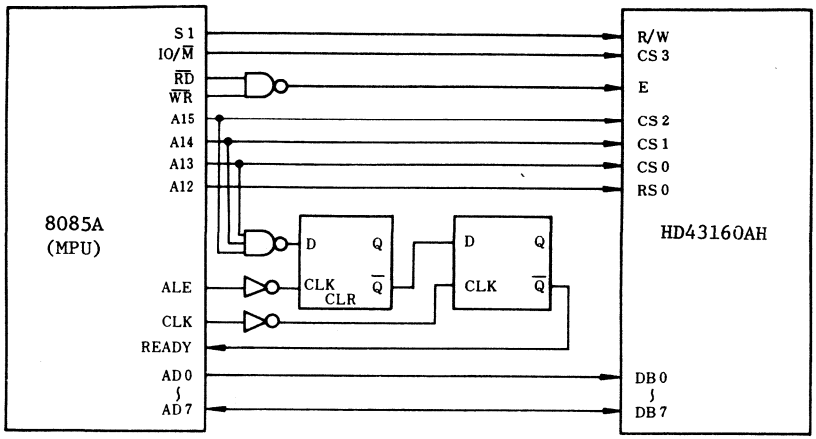
d) Timing chart



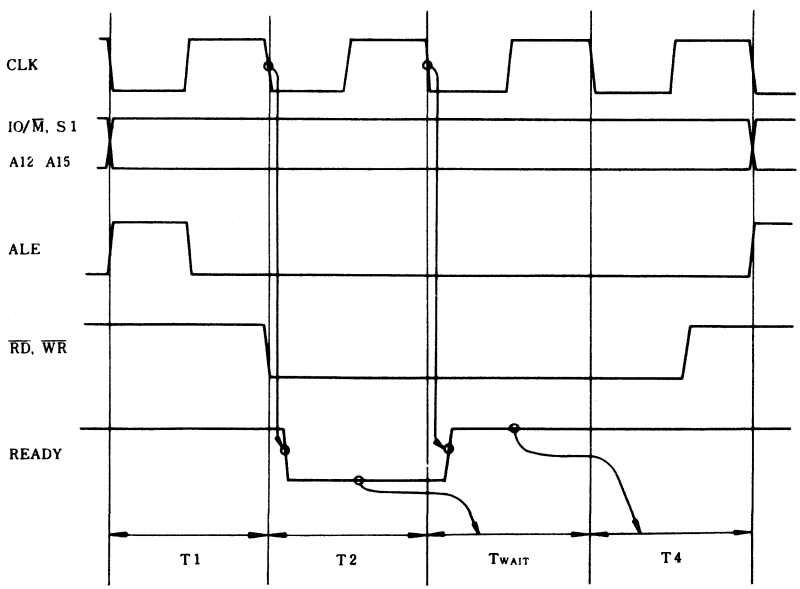
e) Timing characteristics

		Symbol	min	typ	max	Unit
Cycle time of 'E'		t_{cyc}	1.0	-	-	µs
Pulse width of 'E'	H level	P_{WEH}	0.45	-	25	µs
	L level	P_{WEL}	0.45	-	-	µs
Set up time of CS	Write	t_{AS}	140	-	-	ns
Deta delay time	Write	t_{DDW}	-	-	225	ns
	Read	t_{DDR}	-	-	300	ns
Hold time		t_H	10	-	-	ns

f) Example 2 Interface to 8085A (Intel)



g) Timing chart



Pulse widths of $\overline{RD}$ and $\overline{WR}$ signals of the 8085A are 400ns MIN, while the pulse width of E signal of the HD43160AH is 450 ns min. Therefore, in this example, $\overline{RD}$ and $\overline{WR}$ signal pulse widths are widened by using T_{WAIT} cycle.

■ DISPLAY COMMANDS

● Display Controll Instructions

These instructions should be written into the instruction register of HD43160AH by the microcomputer. (RS0='L', R/W='L')

a) Display clear

	MSB							LSB
Code:	0	0	0	0	0	0	0	1

Operation: The screen is cleared and the cursor returns to the 1st digit.

b) Cursor return

	MSB							LSB
Code:	0	0	0	0	0	0	1	0

Operation: The cursor returns to the 1st digit and the characters being displayed do not change.

c) Cursor ON/OFF

	MSB							LSB	
Code:	0	0	0	0	0	1	0	0	(ON)
	0	0	0	0	0	1	0	1	(OFF)

Operation: The cursor appears (ON) or disappears (OFF).

d) Set cursor position

			MSB		LSB
Code:	1 line		1		(N-1) binary
	2 lines	upper	1	0	(n-1) binary
		lower	1	1	(m-1) binary

N,n,m: digit number

Operation: The cursor moves to the Nth (nth, mth) digit.

N ≦ the total character number;

n,m ≦ 1/2 total character number.

ex 1 *1 line*

Set the cursor at 55 digit. The code is '10110110'.

ex 2 *2 lines*

Set the cursor at 35 digit of upper or lower line.

The code is '10100010' (upper).

'11100010' (lower).

- Display Character Command

When the character code is written into the character register of HD43160AH, the character of this code appears where the cursor was displayed and the cursor moves to the next digit. (RS0='H', R/W='L')

MSB LSB

code: (CHARACTER CODE)

ex. 1

before ABCD_

after ABCDE_

- Read Busy Flag

When CS0 ~ CS3='H', R/W='H' and E='H' (RS0='don't care'), the Busy/Ready signal appears on DB7.

DB7 'H': BUSY

'L': READY

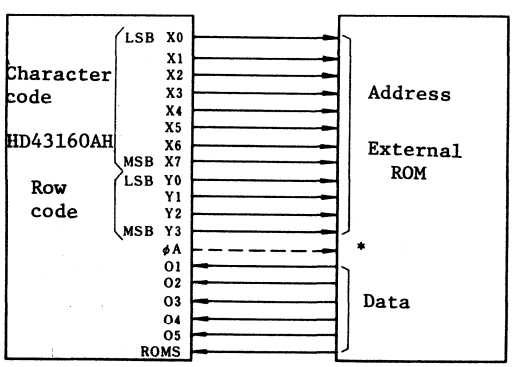
Time Length of Busy (oscillation frequency=200kHz)

	MIN	MAX	
Display clear	2.0	2.05	ms
Other operations	50	100	µs

(depends on the operating frequency)

- Interface to External ROM

a) Example

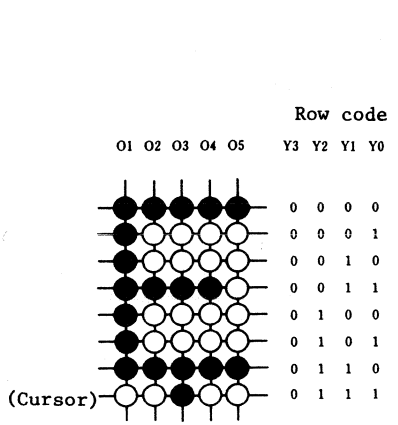


ROMS
1: Ext.
0: Int.

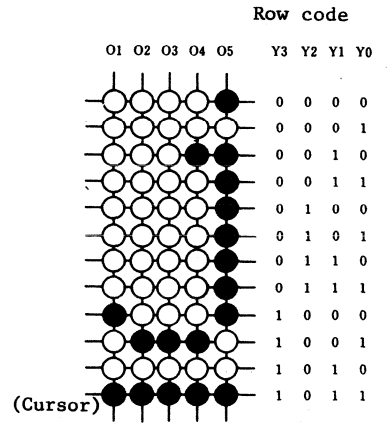
*φA is used as the precharge signal for Dynamic ROM if necessary.

Interface to External ROM

b) Row code

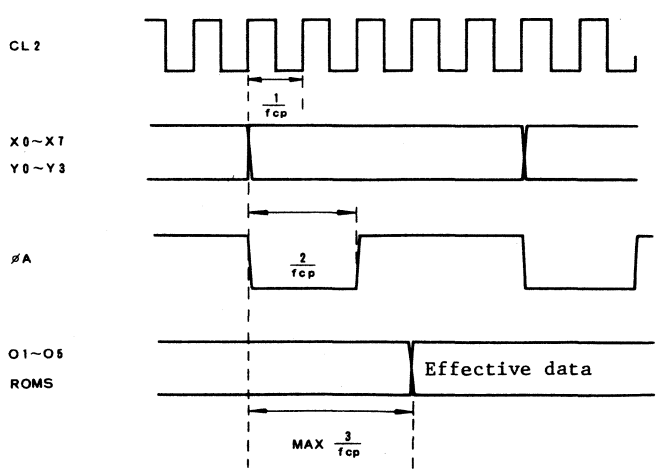


5 × 7 + Cursor



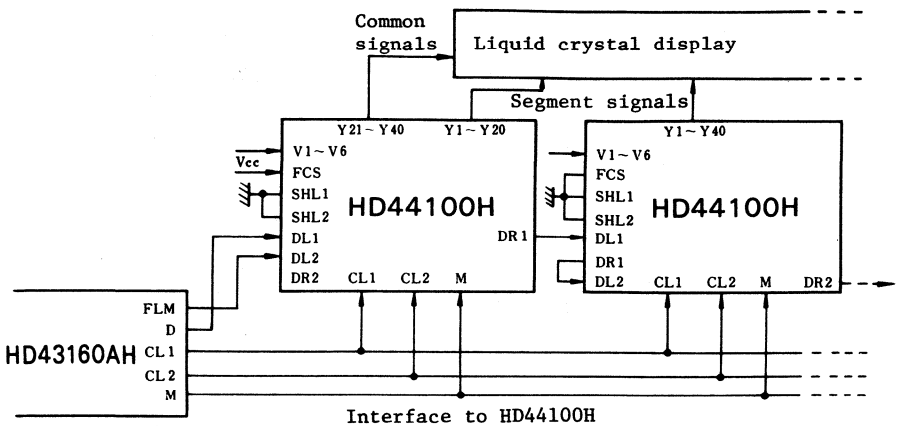
5 × 11 + Cursor

c) Timing chart

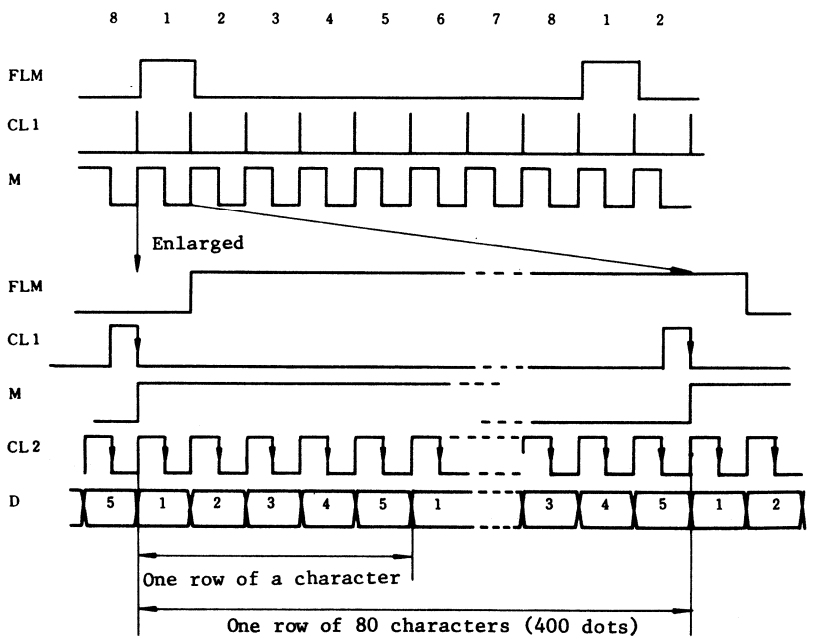


- Interface to LCD Drivers

a) Example



b) Wave forms (5 × 7 + Cursor 1 line)

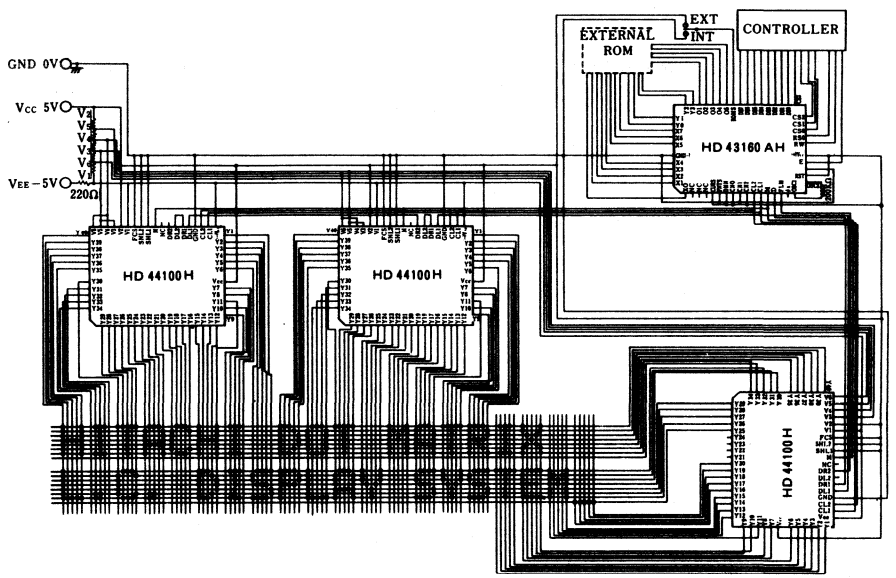


■ DOT MATRIX LIQUID CRYSTAL DISPLAY SYSTEM

Typical Application

5 × 7 + Cursor

2 Lines 40 Characters



HD44780, HD44780A (LCD-II)

(Dot Matrix Liquid Crystal Display Controller & Driver)

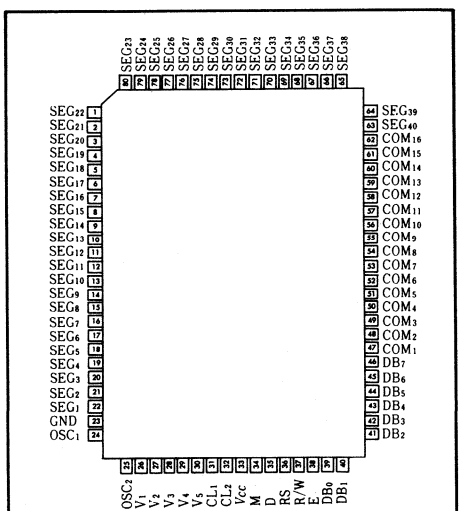
The LCD-II (HD44780, HD44780A) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip. The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780, HD44780A). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

■ FEATURES

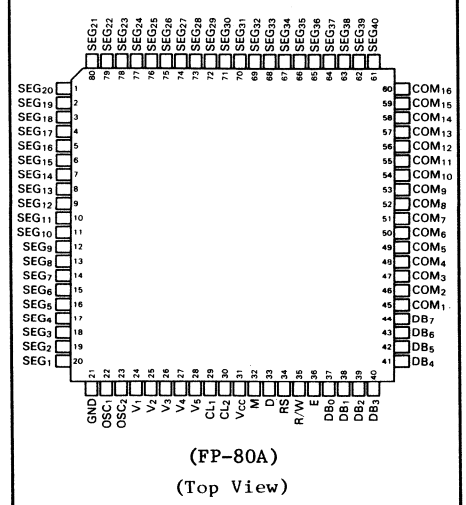
- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM ... 80 × 8 bits (80 characters, max.)
- Character generator ROM ...
  Character font 5 × 7 dots: 160 characters
  Character font 5 × 10 dots: 32 characters

■ PIN ARRANGEMENT



(FP-80)

(Top View)



(FP-80A)

(Top View)

HITACHI

- Both display data and character generator RAMs can be read from the MPU.
- Internal liquid crystal display driver .....
  16 common signal drivers
  40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H)
- Duty factor selection (selected by program) .....
  1/8 duty: 1 line of 5 × 7 dots + cursor
  1/11 duty: 1 line of 5 × 10 dots + cursor
  1/16 duty: 2 lines of 5 × 7 dots + cursor

Maximum number of display characters

No. of display lines	Duty factory	Extension	LCD-II	HD44100H	No. of display characters
1-line display	1/8 1/11 duty	Not provided	1 pc.	—	8 characters ×1 line
		provided	1 pc.	9 pcs. (8 characters/pc.)	80 characters ×1 line
2-line display	1/16 duty	Not provided	1 pc.	—	8 characters ×2 lines
		provided	1 pc.	4 pcs.(8 characters ×2 lines/pc)	40 characters ×2 lines

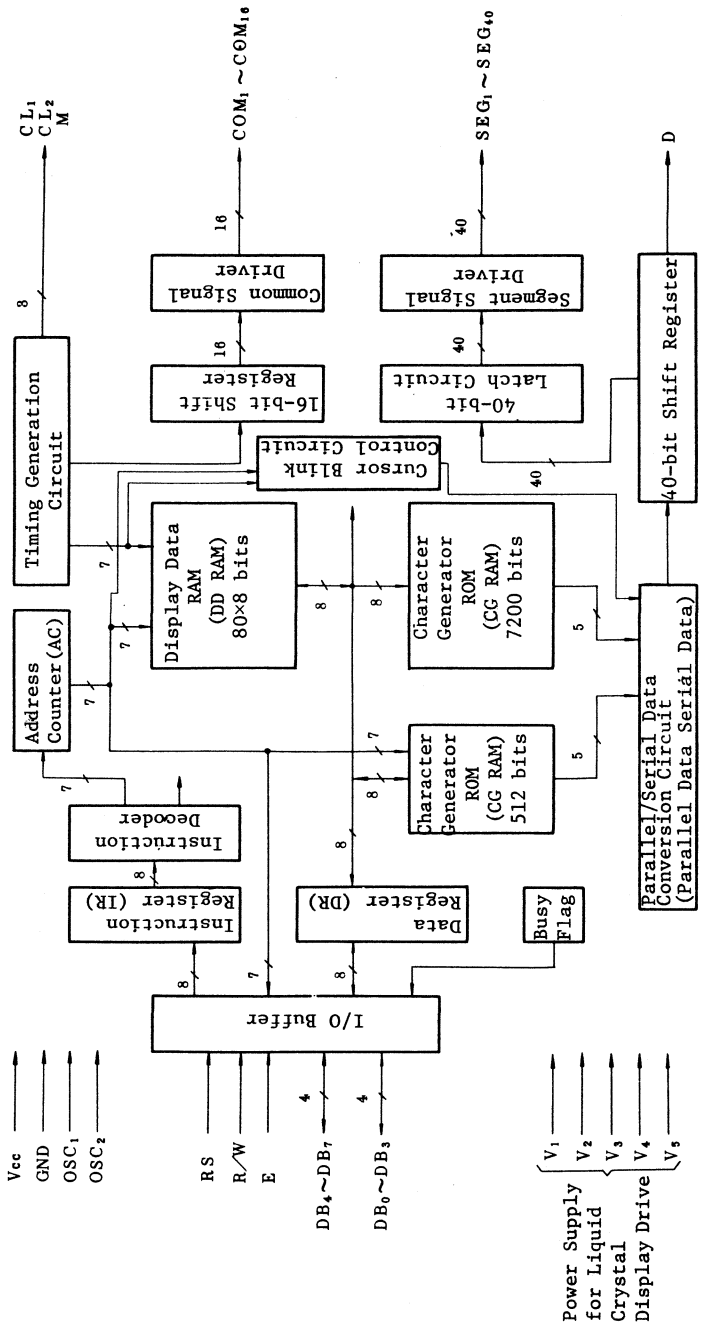
- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)
- Internal oscillation circuit (with external resistor or ceramic filter)
  (External clock operation possible)
- CMOS process
- Logic power supply: A single + 5V (excluding power for liquid crystal display drive)
- Operation temperature range: -20 ~ +75°C
  (Device for -40 ~ +85°C available upon request)
- 80-pin plastic QFP (FP-80, FP-80A)

■ ORDERING INFORMATION

Type No.	Operation Frequency	Package
HD44780SA**H	1.0 MHz	80-Pin plastic QFP (FP-80)
HD44780SA**FH		80-Pin plastic QFP (FP-80A)
HD44780SA**FA	1.5 MHz	80-Pin plastic QFP (FP-80)

Note: ** = ROM Code No.

■ BLOCK DIAGRAM (LCD-II INTERIOR)



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}-13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	-0.3 to V_{CC}+0.3	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-55 to +125	°C	

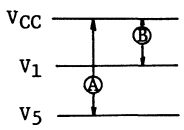
Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND=0V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$

(high ← → low)

● Electrical Characteristics (V_{CC} = 5V±10%, Ta = -20 to +75°C)



Ⓐ = $V_{CC}-V_5$
Ⓑ = $V_{CC}-V_1$
Ⓐ ≧ 1.5V
Ⓑ ≦ 0.25 ×A

The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

HD44780

Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	V_{CC}	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
Output "High" Voltage (1)(TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	0.9V_{CC}	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	L_{OL}=0.04mA	-	-	0.1V_{CC}	V	(4)
Driver Voltage Descending (COM)	V_{COM}	Id=0.05mA	-	-	2.9	V	(10)
Driver Voltage Descending (SEG)	V_{SEG}	Id=0.05mA	-	-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	µA	(5)
Pull up MOS Current	$-I_p$	V_{CC}=5V	50	125	250	µA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}= 250kHz	-	0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}= fcp=270kHz	-	0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	270	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}		-	-	0.2	µs	(7)
External Clock Fall Time	t_{fcp}		-	-	0.2	µs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	-	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage	V_{LCD1}	$V_{CC}-V_5$ 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	$V_{CC}-V_5$ 1/4 bias	3.0	-	11	V	(13)

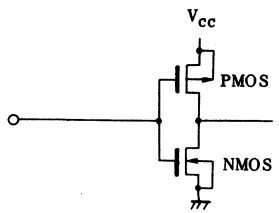
HD44780A

Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	V_{CC}	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
Output "High" Voltage (1)(TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	$0.9V_{CC}$	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	L_{OL}=0.04mA	-	-	$0.1V_{CC}$	V	(4)
Driver Voltage Descending (COM)	V_{COM}	Id=0.05mA	-	-	2.9	V	(10)
Driver Voltage Descending (SEG)	V_{SEG}	Id=0.05mA	-	-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	µA	(5)
Pull up MOS Current	$-I_p$	V_{CC}=5V	50	125	250	µA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}= 250kHz	-	0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}= fcp=270kHz	-	0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	270	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}		-	-	0.2	µs	(7)
External Clock Fall Time	t_{fcp}		-	-	0.2	µs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	-	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage.	V_{LCD1}	V_{CC}-V5, 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	V_{CC}-V5, 1/4 bias	3.0	-	11	V	(13)

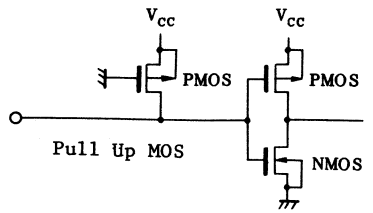
Note 1: The following are I/O terminal configurations except for liquid crystal display output.

- Input Terminal

Applicable Terminals: E (No pull up MOS)

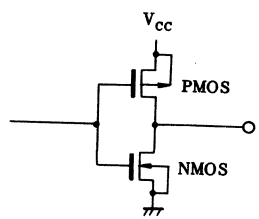


Applicable Terminals: RS, R/W (With pull up MOS)



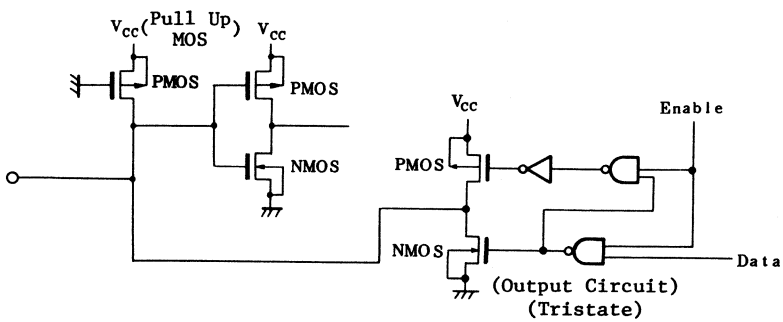
- Output Terminal

Applicable Terminals: CL_1, CL_2, M, D



- I/O Terminal

Applicable Terminals: DB_0 to DB_7



Note 2: Input terminals and I/O terminals. Excludes OSC_1 terminals.

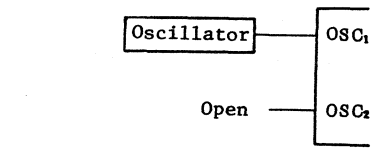
Note 3: I/O terminals.

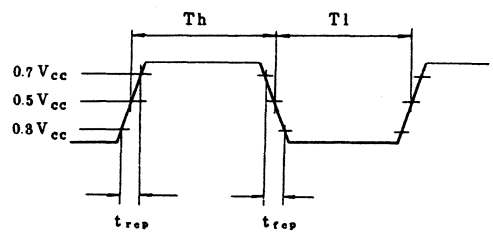
Note 4: Output terminals.

Note 5: Current flowing through pull-up MOS's and output drive MOS's is excluded.

Note 6: Input/Output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

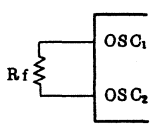
Note 7: External clock operation.





$$Duty = \frac{Th}{Th + Tl} \times 100\%$$

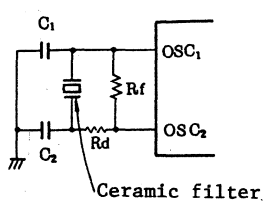
Note 8: Internal oscillator operation using oscillation resistor Rf.



Rf : 91kΩ± 2 %

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length for these terminals should be minimized.

Note 9: Internal oscillator operation using a ceramic filter.is used.



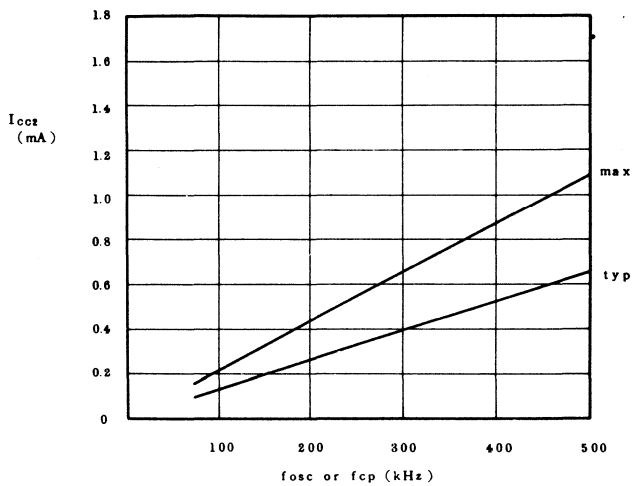
Ceramic filter: CSB250A (Murata)
Rf: 1MΩ ±10%
C_1: 680pF±10%
C_2: 680pF±10%
Rd: 3.3kΩ±5%

Note 10: Applies to both V_{COM} and V_{SEG} voltage drops.

V_{COM}: From poer supply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})

V_{SEG}: From power supply terminal V_{CC}, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

Note 11: Relation between operation frequency and current consumption is shown in this diagram. (V_{CC} = 5V)



Note 12: Applied to OSC_1 terminal.

Note 13: The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

● Timing Characteristics

Write Operation

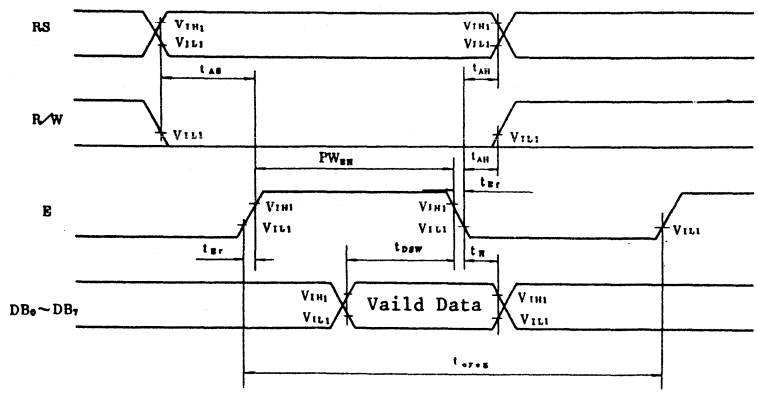


Fig. 1 Bus Write Operation Sequence
(Writing data from MPU to LCD-II)

Read Operation

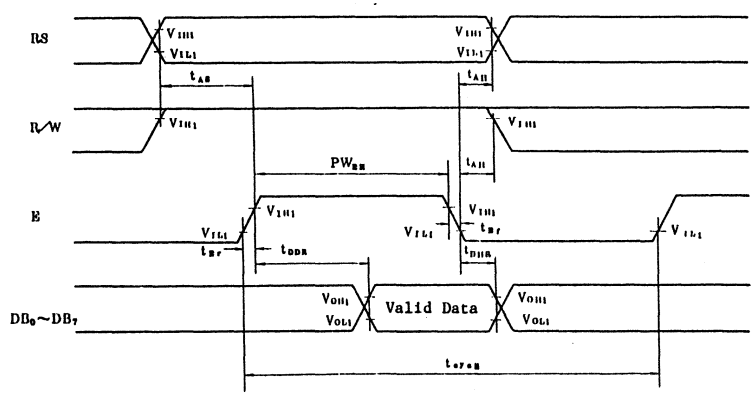


Fig. 2 Bus Read Operation Sequence
(Reading out data from LCD-II to MPU)

Interface Signal with Driver LSI HD44100H

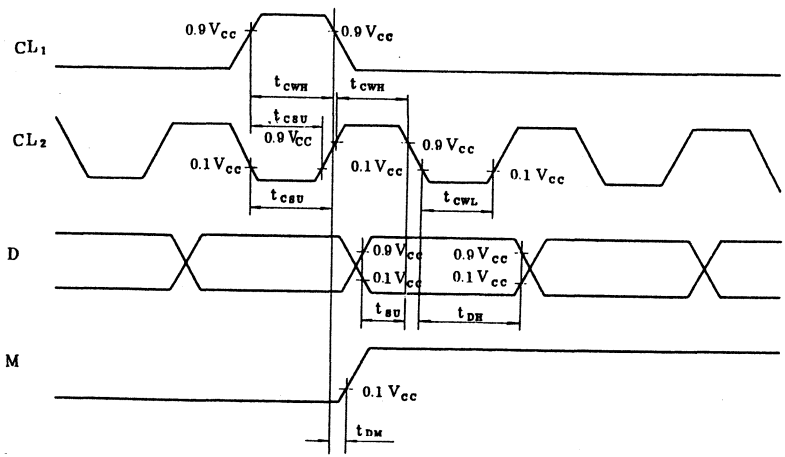


Fig. 3 Sending Data to Driver LSI HD44100H

● Bus Timing Characteristics (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

o HD44780

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		$t_{cyc}E$	Fig. 1	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	450	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	140	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	195	-	ns
Data Hold Time		t_H	Fig. 1	10	-	ns

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		$t_{cyc}E$	Fig. 2	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	450	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	140	-	ns
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	320	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

o HD44780A

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		$t_{cyc}E$	Fig. 1	666	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	300	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	60*1	-	ns
				100*2	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	100	-	ns
Data Hold Time		t_{H}	Fig. 1	10	-	ns

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		$t_{cyc}E$	Fig. 2	666	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	300	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	60*1		ns
				100*2		
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	190	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

Notes: *1. *1, is 8-bit interface mode
*2. *2, is 4-bit interface mode

● Interface Signal with HD44100H Timing Characteristics
(V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

o HD44780

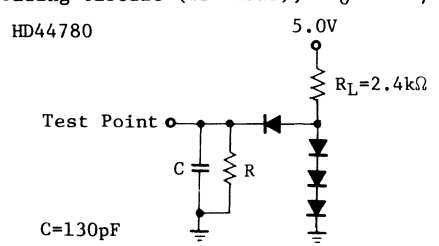
Item		Symbol	Test condition	Limit min	Limit max	Unit
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock Pulse Width	"Low" level	t_{CWL}	Fig. 3	800	-	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	-	ns
Data Set-up Time		t_{SU}	Fig. 3	300	-	ns
Data Hold Time		t_{DH}	Fig. 3	300	-	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

HD44780A

Item		Symbol	Test condition	Limit min	Limit max	Unit
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock Pulse Width	"Low" level	t_{CWL}	Fig. 3	800	-	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	-	ns
Data Set-up Time		t_{SU}	Fig. 3	300	-	ns
Data Hold Time		t_{DH}	Fig. 3	300	-	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

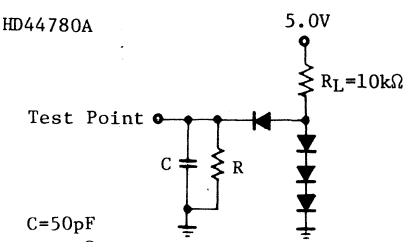
Loading Circuit (TTL Load); DB_0 to DB_7

HD44780



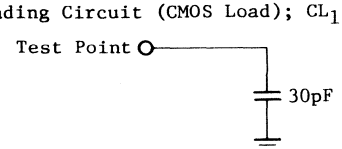
C=130pF
R=11kΩ
All Diodes: 1S2074Ⓗ

HD44780A



C=50pF
R=20kΩ
All Diodes: 1S2074Ⓗ

Loading Circuit (CMOS Load); CL_1, CL_2, D, M

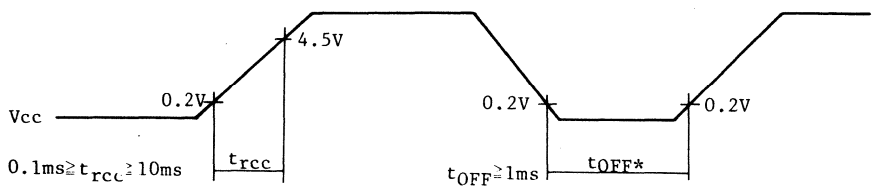


● Power Supply Conditions Using Internal Reset Circuit

LCD-II

Item	Symbol	Test condition	Limit		Unit
			min	max	
Power Supply Rise Time	trcc	-	0.1	10	ms
Power Supply OFF Time	t_{OFF}	-	1	-	ms

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction.
(Refer to "Initializing by Instruction")



(Note) t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.

■ Terminal Function

Table 1 Functional Description of Terminals

Signal name	No. of lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers "0": Instruction register (for write) Busy flag; address counter (for read) "1": Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W) "0": Write "1": Read
E	1	Input	MPU	Operation start signal for data read/ write
DB_4 ~ DB_7	4	Input/ Output	MPU	Higher order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the LCD-II. DB_7 can be used as a BUSY flag.
DB_0 ~ DB_3	4	Input/ Output	MPU	Lower order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the LCD-II. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Character pattern data corresponding to each common signal is serially sent. "0": Non selection "1": Selection
COM_1 ~ COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are charged to non-selection waveforms. That is, COM_9 ~ COM_{16} are in non-selection waveform at 1/8 duty factor, and COM_{12} ~ COM_{16} are in non-selection waveform at 1/11 duty factor.
SEG_1 ~ SEG_{40}	40	Output	Liquid crystal display	Segment signal
V_1 ~ V_5	5		Power supply	Power supply for liquid crystal display drive
V_{CC}, GND	2		Power supply	V_{CC}; +5V, GND; 0V
OSC_1, OSC_2	2			Terminals connected to resister or ceramic filter for internal clock osillation. For external clock operation, the clock is input to OSC_1.

■ FUNCTION OF EACH BLOCK

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 ~ DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 2 shows, the busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

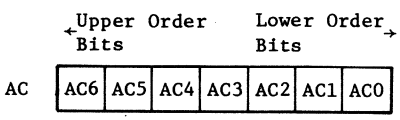
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB_0 ~ DB_6 when RS=0 and R/W=1, as shown in Table 2.

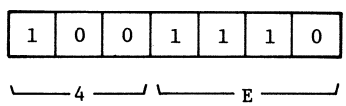
(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80×8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

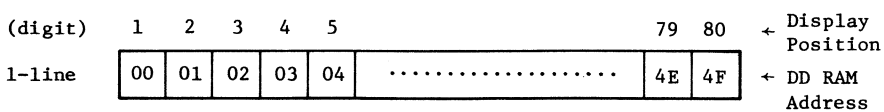
The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



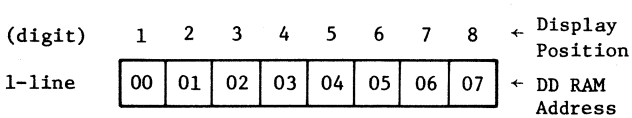
(Example) DD RAM address "4E"



1-line Display (N=0)



(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using 1 HD44780 are displayed as:



When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display)

01	02	03	04	05	06	07	08

(Right Shift Display)

4F	00	01	02	03	04	05	06

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address

HD44780 Display — HD44100H Display

When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display)

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

(Right Shift Display)

4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	...	73	74	75	76	77	78	79	80	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	----	48	49	4A	4B	4C	4D	4E	4F	← DD RAM Address

HD44780 Diaplay — HD44100H(1) Display — HD44100H (2)∿(8) Display — HD44100H(9) Display

2-line Display (N=1)

(digit)	1	2	3	4	5	.....	39	40	← Display Position
1-line	00	01	02	03	04	.....	26	27	← DD RAM Address
2-line	40	41	42	43	44	.....	66	67	

(a) When the number of display characters is less than 40 × 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

(b) 16 characters × 2 lines are displayed when an HD44780 and an HD44100H are used.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

└── HD44780 Display ──┘└── HD44100H Display ──┘

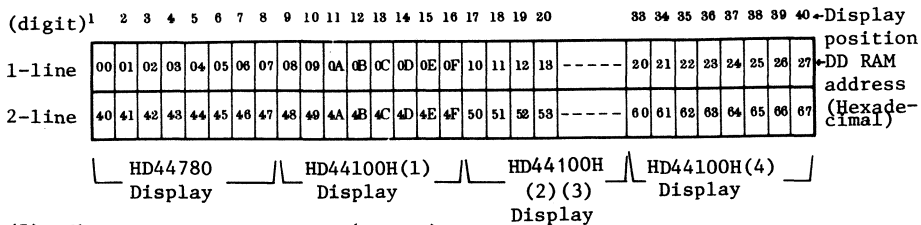
When display shift is performed, the DD RAM address moves as follows:

(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting 4 HD44780's externally.



(5) Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 × 7 dot character patterns and 32 types of 5 × 10 dot character patterns. Table 3 and 4 show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM.

(6) Character Generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 × 7 dots, 8 byptes of character patterns can be written and with 5 × 10 dots 4 types can be written. Write the character codes in the left columns of Tables 3 and 4 to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

As Table 5 shows, an area that is not used for display can be used as a general data RAM.

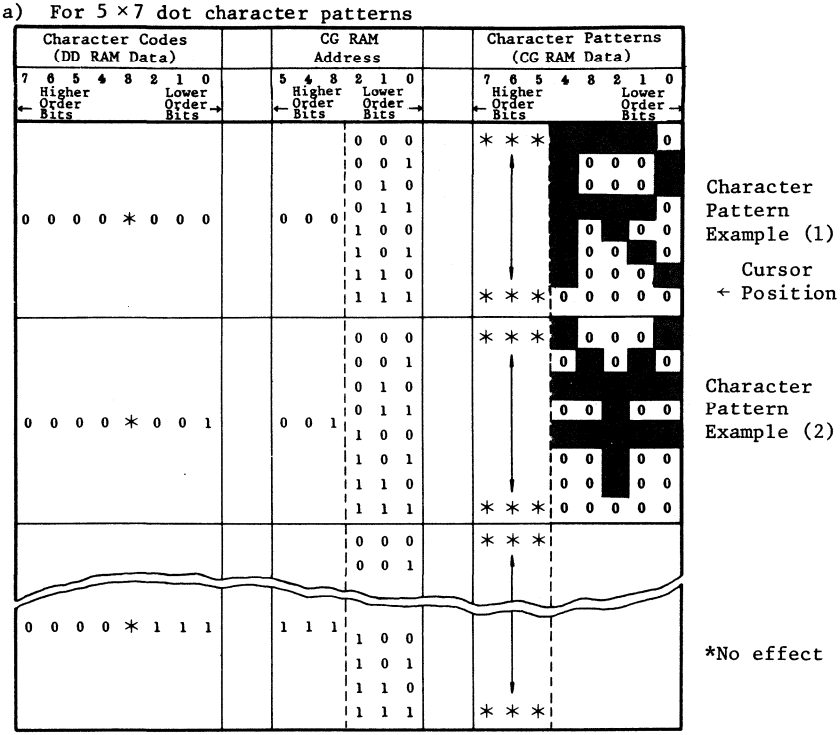
Table 3 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD44780A00)

Higher / Lower 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

* The user can specify any pattern for character-generator ROM.

Table 4 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

(a) For 5 × 7 dot character patterns



(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.

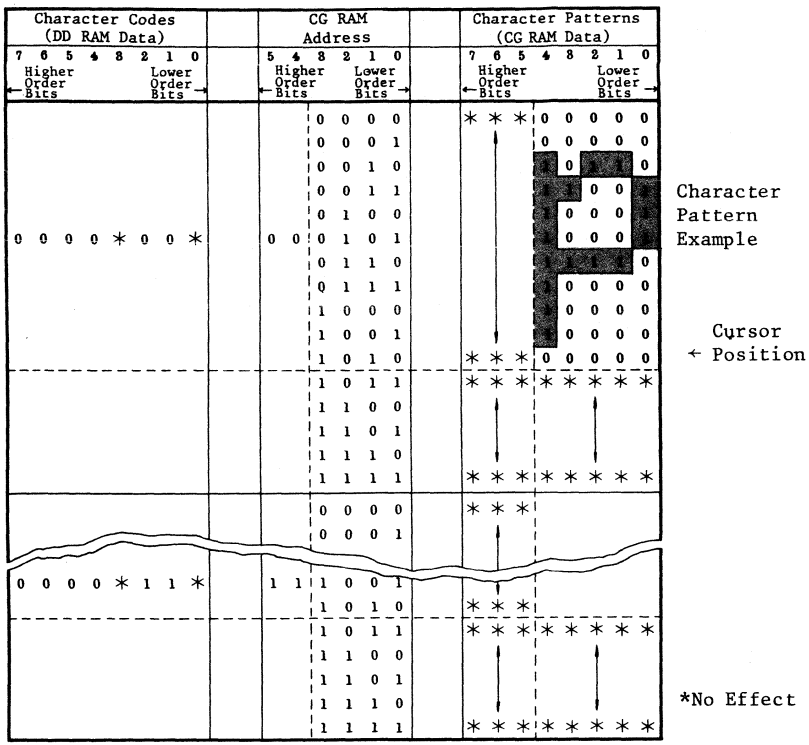
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Table 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit,the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(b) For 5 ×10 dot character patterns



(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.

Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(7) Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undersirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension.

Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

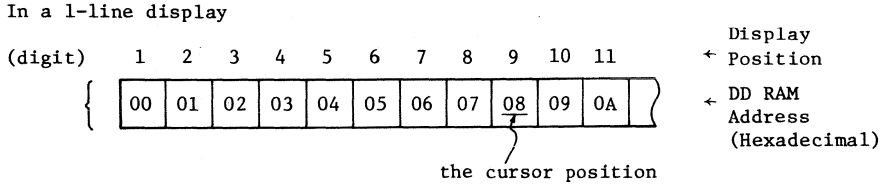
(9) Cursor/Blink Control Circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

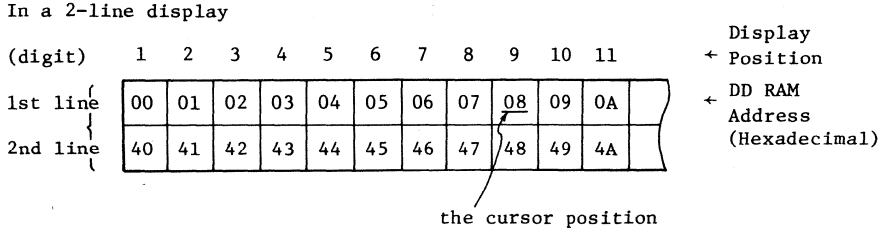
When the address counter is $(08)_{16}$, a cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.

The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

■ INTERFACING TO MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interace to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

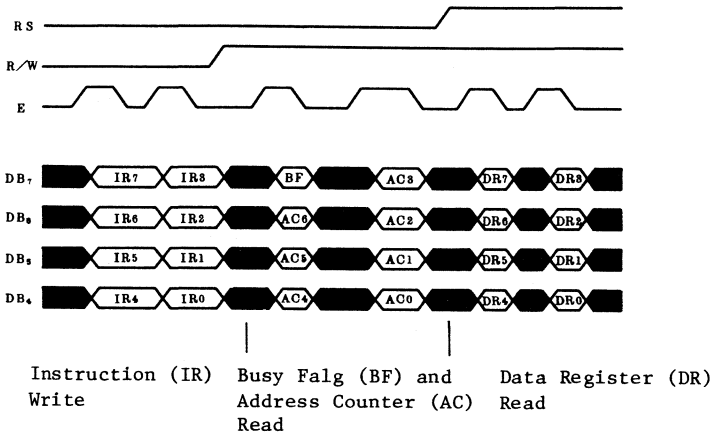


Fig. 4 4-bit Data Transfer Example

(2) When interface data is 8 bits long, data is transferred using the 8 data buses of DB_0 ~ DB_7.

■ RESET FUNCTION

● Initializing by Internal Reset Circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10 ms after V_{CC} rises to 4.5V.

(1) Display clear

(2) Function ser ..... DL=1 : 8 bit long interface data
N =0 : 1-line display
F =0 : 5 × 7 dot character font

(3) Display ON/OFF control ..... D =0 : Display OFF
C =0 : Cursor OFF
B =0 : Blink OFF

(4) Entry mode set ..... I/D=1: +1 (increment)
S =0 : No shift

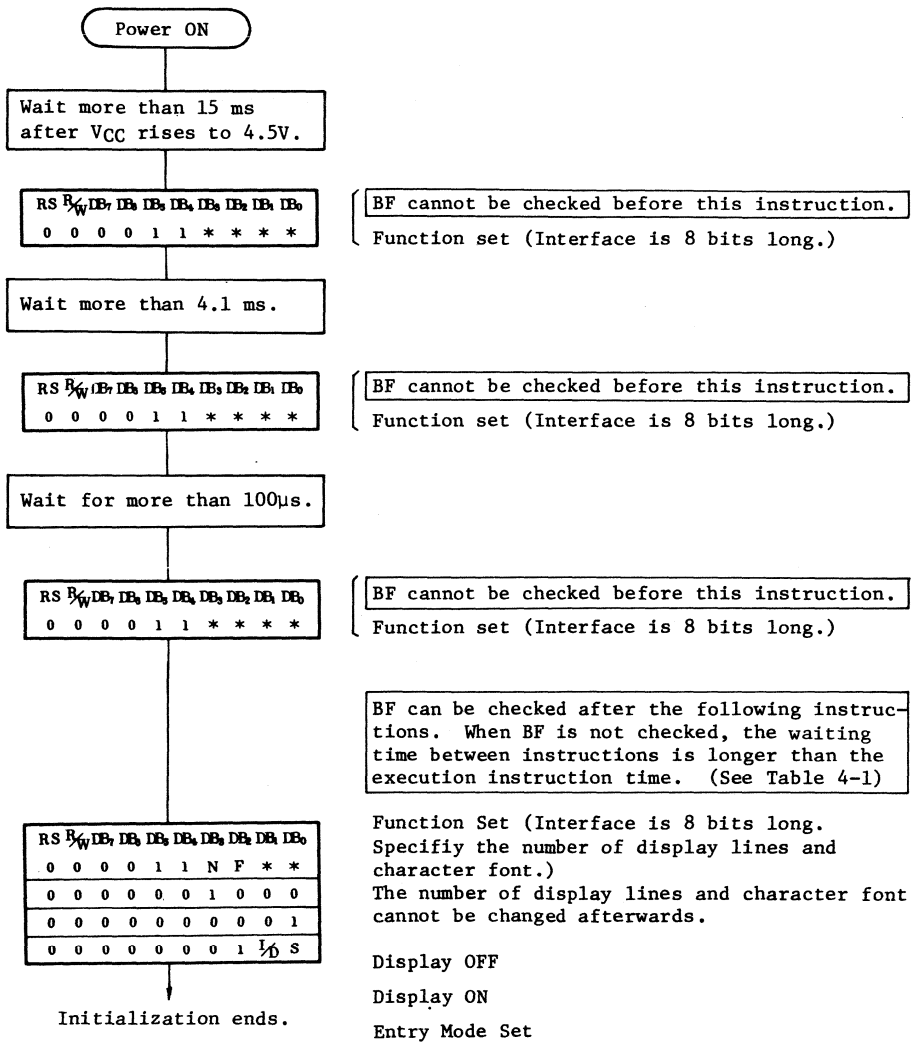
(Note) When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit with not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

● Initializing by Instruction

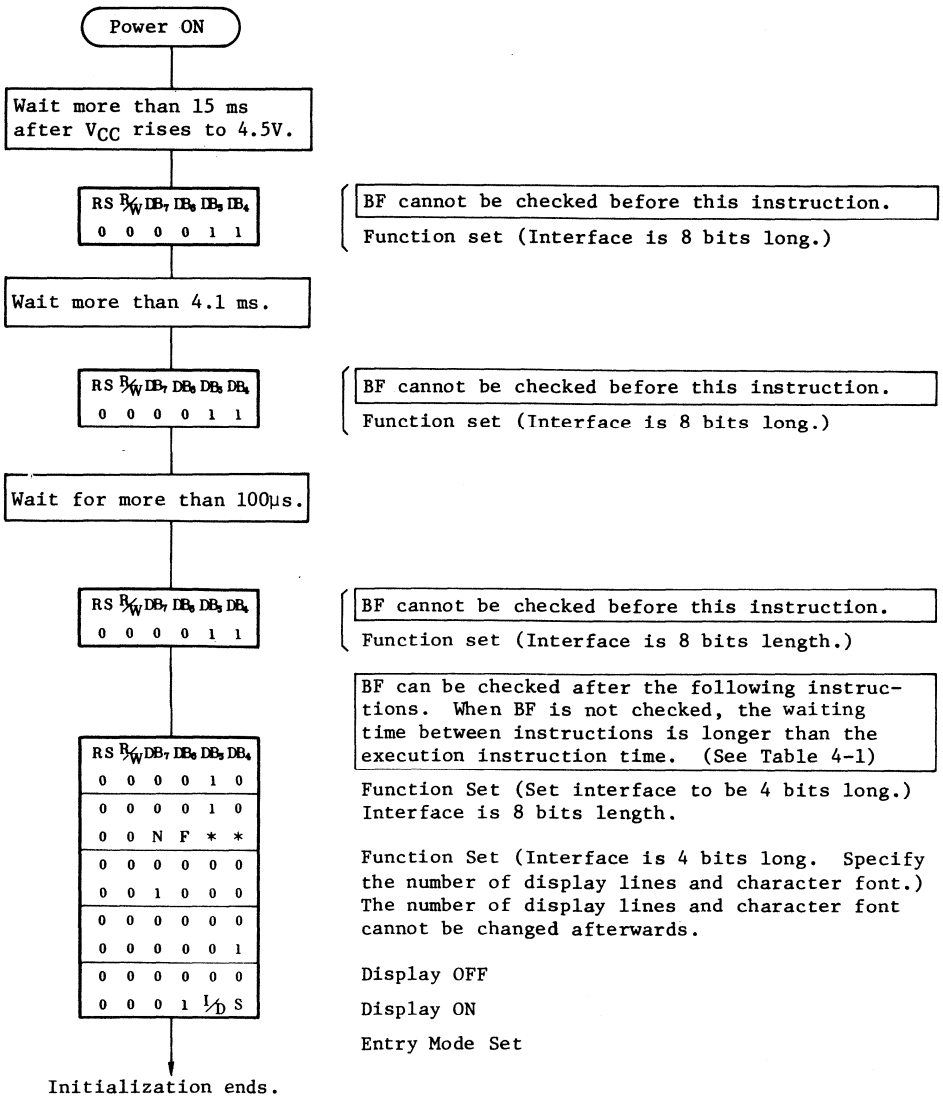
If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;



(2) When interface is 4 bits long;



■ INSTRUCTION

● Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.

(2) Give internal RAM addresses.

(3) Perform data transfer with internal RAM

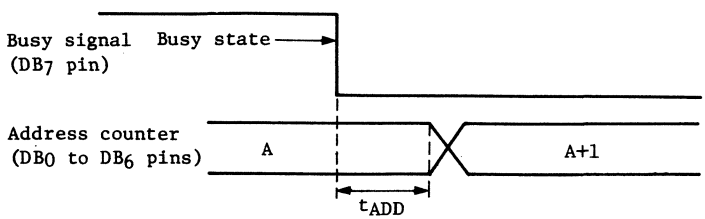
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by -1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see Table 7.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

(Note) 1. Make sure the HD44780 is not in the busy state (BF=0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 5 for a list of each instruction execution time.

2. After execution of a CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off. Suppose that the time elapses after the busy flag turns off until the address counter is updated is t_{ADD}.



t_{ADD} depends on the operation frequency.

t_{ADD}(sec) = $1.5/f_{cp}$ or f_{osc}

Table 5 Instructions

Instruction	Code										Description	Execution time (max) (when fcp or fosc is 250kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in adress counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40µs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40µs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40µs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0µs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40µs t_{ADD}=6ns (Note 2)
Read Data from CG or DD RAM	1	0	Read Data								Reads data from DD RAM or CG RAM.	40µs t_{ADD}=6ns (Note 2)
	I/D=1 : Increment I/D=0 : Decrement S =1 : Accompanies display shift. S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right. R/L=0 : Shifts to the left. DL =1 : 8 bits, DL=0 : 4 bits. N =1 : 2 lines, N=0 : 1 line F =1 : 5×10 dots, F=0 : 5×7 dots BF =1 : Internally operating BF =0 : Can accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM A_{CC} : CG RAM address A_{DD} : DD RAM address. Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fcp or fosc is 270kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* No Effect

Description of Details

(1) Clear Display

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal)(character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the dispaly (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return Home

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	*

* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry Mode Set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D=1) or decrements (I/D=0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S : Shifts the entire display either to the right or to the left when S is 1; to the left when I/D=1 and to the right when I/D=0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S=0.

(4) Display ON/OFF Control

	RS	R/W	DB_7						DB_6
Code	0	0	0	0	0	0	1	D	C	B

D : The display is ON when D=1 and OFF when D=0. When off due to D=0, display data remains in the DD RAM. It can be displayed immediately by setting D=1.

C : The cursor displays when C=1 and does not display when C=0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5 × 10 dot character font is selected.

B : The character indicated by the cursor blinks when B=1. The blink is displayed by switching between all blank dots and display characters at 409.6ms interval when fcp or fosc=250kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. $409.6 \times \frac{250}{270} = 379.2$ms when fcp=270kHz.)

5 × 7 dot character font 5 × 10 dot character font Alternating display

(a) Cursor Display Example (b) Blink Display Example

(5) Cursor or Display Shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* (Don't care)

DL : Sets interface data length. Data is sent or received in 8 bit lengths ($DB_7 \sim DB_0$) when DL=1 and in 4 bit lengths ($DB_7 \sim DB_4$) when DL=0.
When the 4 bit length is selected, data must be sent or received twice.

N : Sets number of display lines.

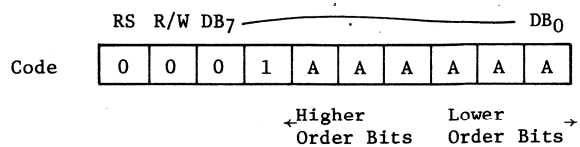
F : Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N F	No. of display lines	Character font	Duty factor	Remarks
0 0	1	5 ×7 dots	1/8	
0 1	1	5 ×10 dots	1/11	
1 *	2	5 ×7 dots	1/16	Cannot display 2 lines with 5 ×10 dot character font.

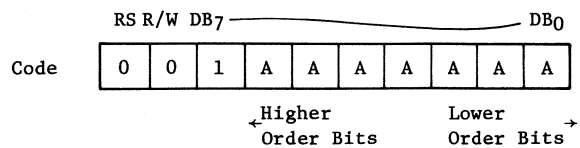
* (Don't care)

(7) Set CG RAM Address



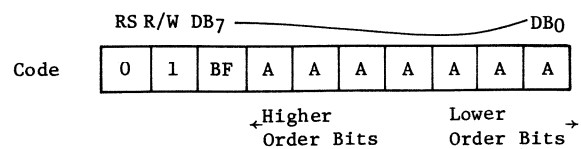
Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM Address



Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.
However, when N=0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal).
when N=1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read Busy Flag and Address



Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF=1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write Data to CG or DD RAM

	RS	R/W	DH_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read Data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift in struction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set

instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

■ HOW TO USE THE HD44780

● Interface to MPU

(1) Interface to 8-bit MPU

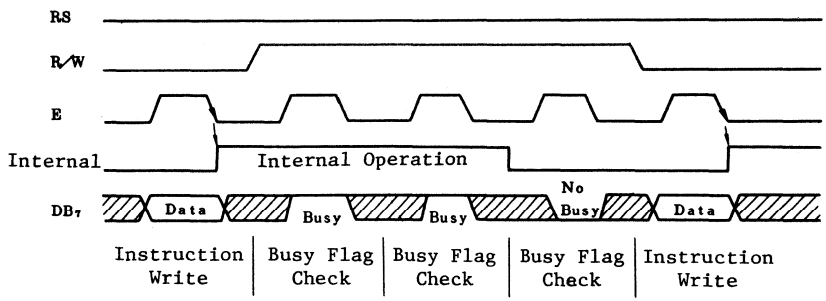
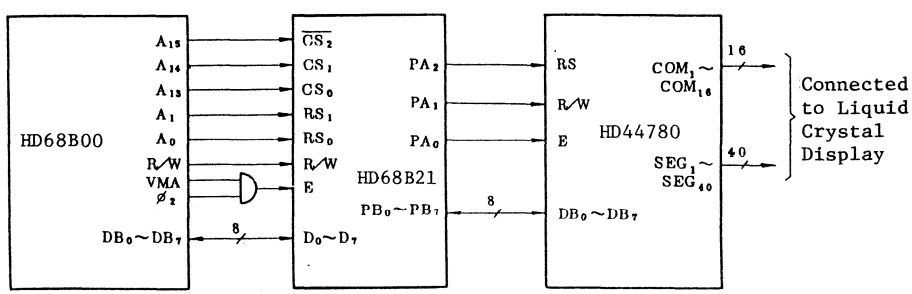


Fig. 5 Example of Busy Flag Check Timing Sequence

① When connecting to 8-bit MPU through PIA

Fig. 6-2 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

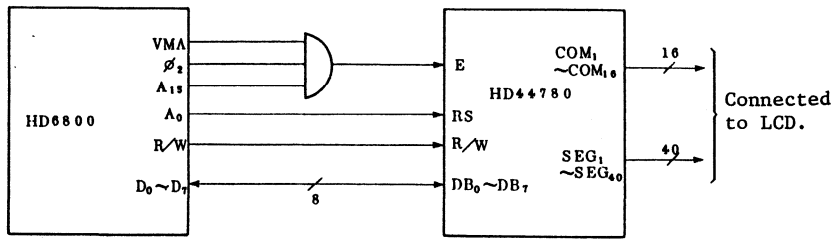
In the example, PB_0 to PB7 are connected to the data buses DB_0 to DB_7 and PA0 to PA2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.



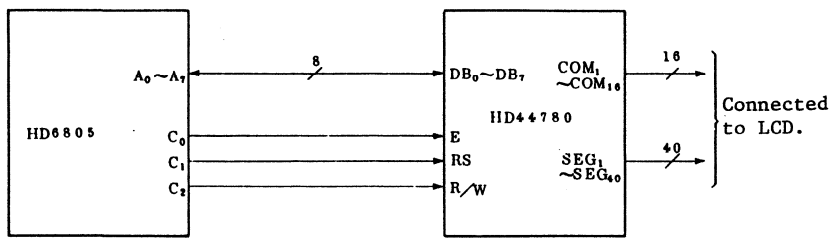
HD68B00: 8 bit CPU

Fig. 6 Example of Interface to HD68B00 Using PIA (HD68B21)

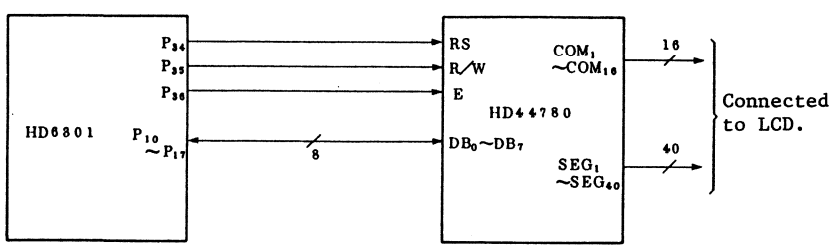
② Connecting directly to the 8-bit MPU bus line



③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301

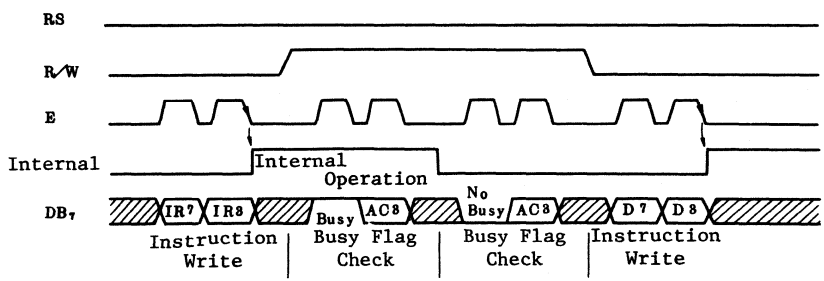


(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 7)

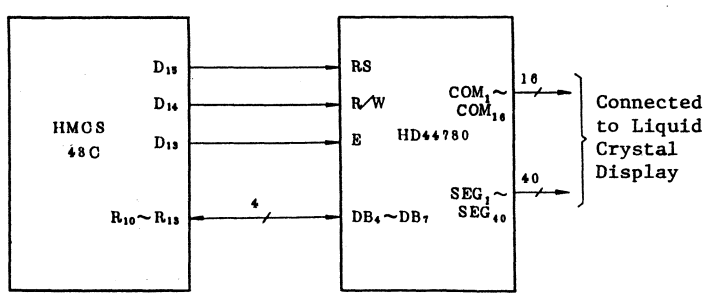
Fig. 8 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



(Note) IR7, IR3: Instruction 7th bit, 3rd bit
AC3 : Address Counter 3rd bit

Fig. 7 An Example of 4-bit Data Transfer Timing Sequence



HMCS43C: Hitachi 4-bit single-chip microcomputer

Fig. 8 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

(1) Character Font and Number of Lines

The HD44780 can perform 2 types of display, 5 ×7 dots and 5 ×10 dots as character font, with a cursor on each.

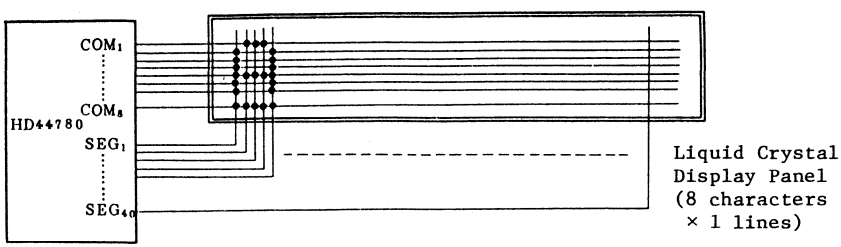
Up to 2 lines are displayed with 5 ×7 dots and 1 line with 5 ×10 dots. Therefore, three types of common signals are available:

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 ×7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 ×7 dots + Cursor	16	1/16

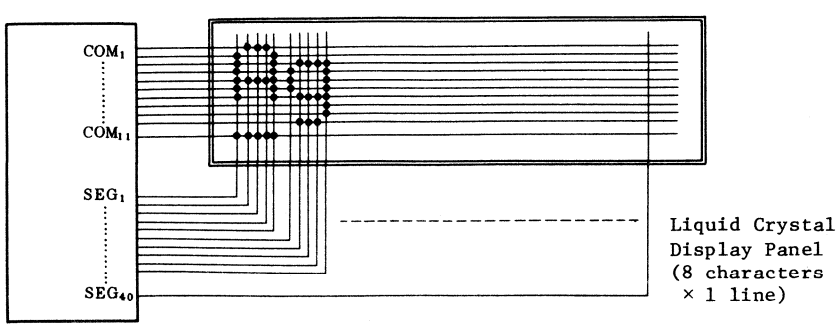
Number of lines and font types can be selected by program.
(See to Table 5 Instruction)

(2) Connection to HD44780 and Liquid Crystal Display

Fig. 9 (1) and (2) show connection examples.

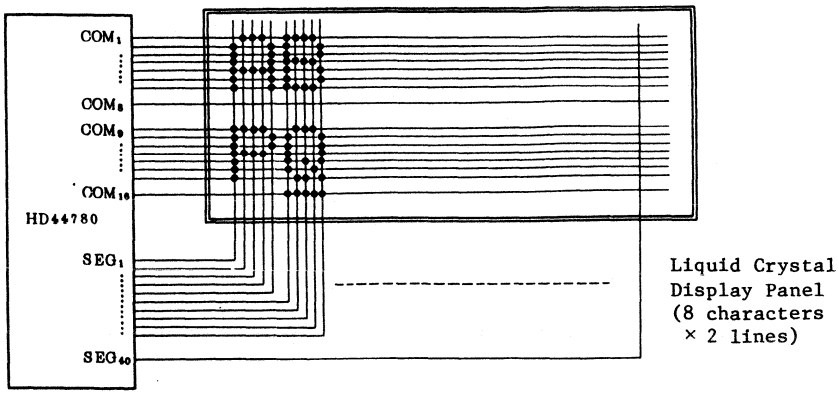


(a) Example of a 5 ×7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)



(b) Example of a 5 ×10 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

Fig. 9 (1) Liquid Crystal Display and Connections to HD44780

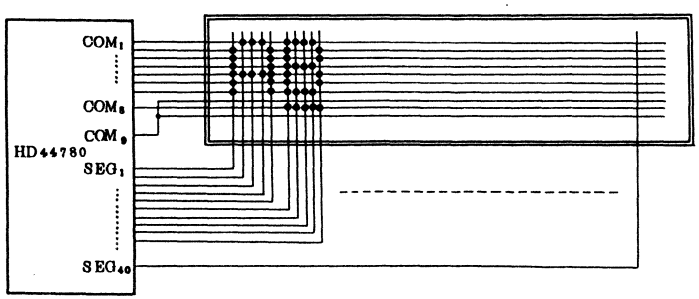


(c) Example of 5 × 7 dot, 8 character × 2 lines Display
(1/5 Bias, 1/16 Duty)

Fig. 9 (2) Liquid Crystal Display and Connection to HD44780

Since 5 signal lines at the SEG can display one digit, one HD44780 can display up to 8 digits for 1-line display and 16 digits for 2-line display.

In Fig. 9 examples (a) and (b), there are unused common signal terminals, non-selection waveforms which always output. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals.

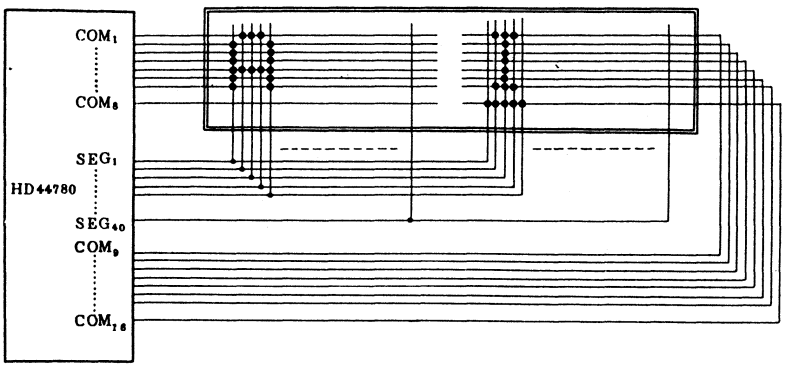


5 × 7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

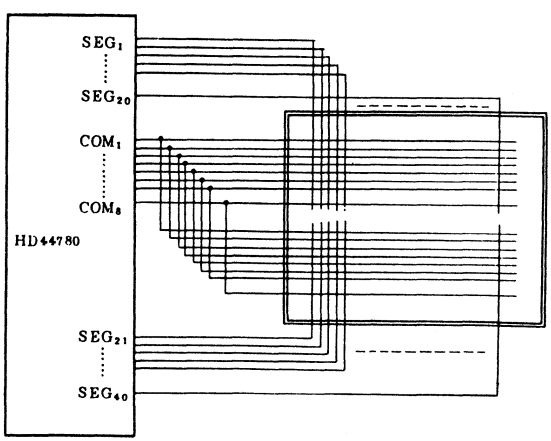
Fig. 10 Using COMg to Avoid Cross-talk on Unneeded Scanning Line

(3) Connection of Changed Matrix Layout

In the preceding examples, the number of lines was matched to the number of scanning lines. The following display types are possible by changing the matrix layout in the liquid crystal display panel.



(a) 5 ×7 dot, 16 character × 1 line Display
(1/5 Bias, 1/16 Duty)



(b) 5 ×7 dot, 4 character × 2 line Display
(1/4 Bias, 1/8 Duty)

Fig. 11 Changed Matrix Layout Displays

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters are dependent on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in Fig. 9.

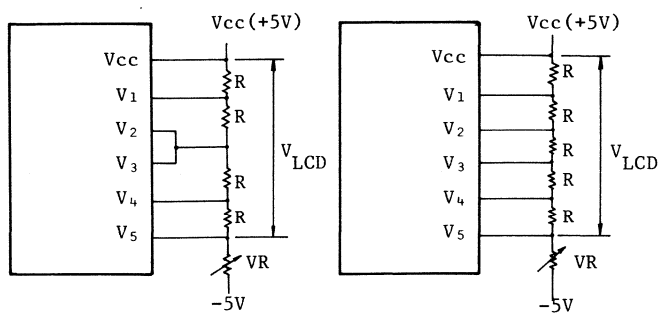
● Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 6 shows the relation.

Table 6 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor / Power Supply Bias	1/8, 1/11	1/16
	1/4	1/5
V_1	$V_{cc} - 1/4\,V_{LCD}$	$V_{cc} - 1/5\,V_{LCD}$
V_2	$V_{cc} - 1/2\,V_{LCD}$	$V_{cc} - 3/5\,V_{LCD}$
V_3	$V_{cc} - 1/2\,V_{LCD}$	$V_{cc} - 3/5\,V_{LCD}$
V_4	$V_{cc} - 3/4\,V_{LCD}$	$V_{cc} - 4/5\,V_{LCD}$
V_5	$V_{cc} - V_{LCD}$	$V_{cc} - V_{LCD}$

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Fig. 13.



(a) 1/4 Bias (1/8, 1/11 Duty)

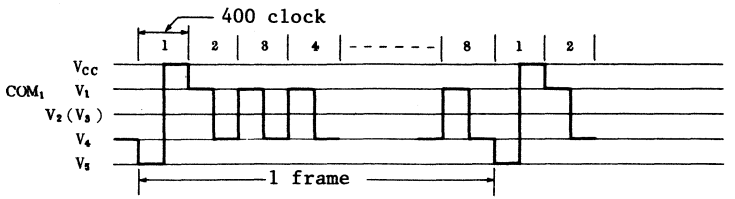
(b) 1/5 Bias (1/16 Duty)

Fig. 13 Drive Voltage Supply Example

- Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The following examples of liquid crystal display frame frequency apply only when oscillation frequency is 250kHz. (1 clock = 4μs)

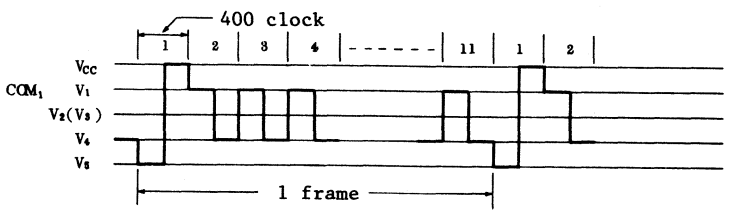
(1) 1/8 Duty



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

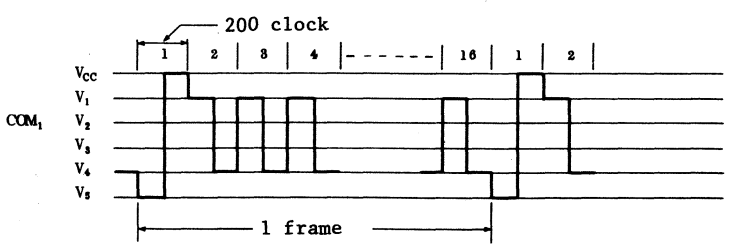
(2) 1/11 Duty



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

● Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting a liquid crystal display driver LSI HD44100H to the HD44780.

When connected to the HD44780, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD44780 directly since it supplies CL_1, CL_2, M and D signals and power for liquid crystal display drive. Fig. 14 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated.

Up to 9 units of the HD44100H can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 4 units for the 2-line display (duty factor 1/16). RAM size limits the HD44780 to a maximum of 80 character display digits. The connection method in Fig. 14 remains unchanged for both 1-line and 2-line display or both 5 ×7 and 5 ×10 dot character fonts.

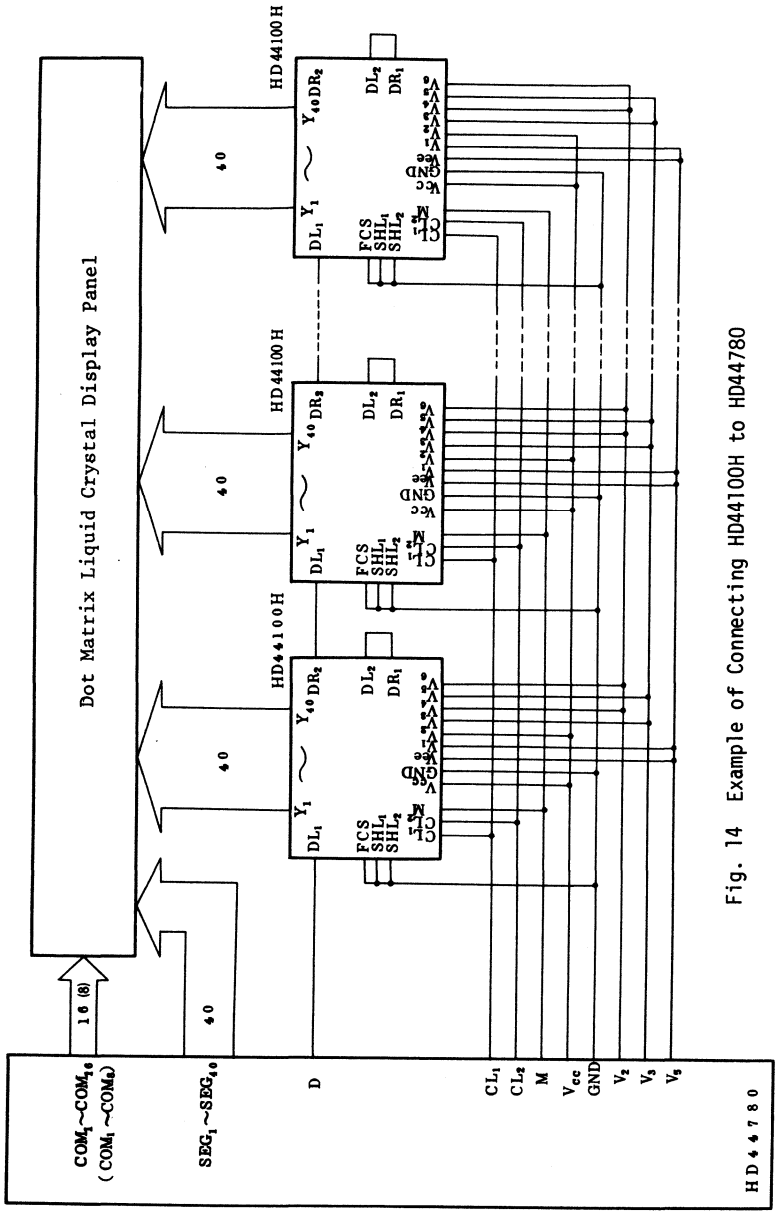


Fig. 14 Example of Connecting HD44100H to HD44780

● Instruction and Display Correspondence

(1) 8-bit operation, 8-digit × 1-line display (using internal reset)

Table 7 shows an example of 8-bit × 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

(2) 4-bit operation, 8-digit × 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. Table 8 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as a function (see Table 8).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

(3) 8-bit operation, 8-digit × 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See Table 9) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

(Note) When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD44780 must be initialized by instruction. (See "Initializing by Instruction")

Table 7 8-bit Operation, 8-digit 1-line Display Example(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	

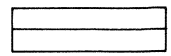
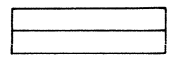
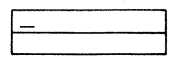
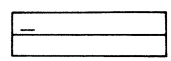
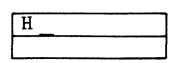
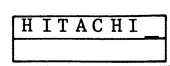
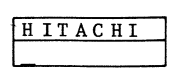
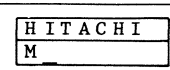
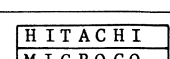
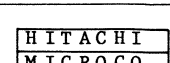
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

Table 8 4-bit Operation, 8-digit 1-line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 ⁓ DB4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5×7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 9 8 bit Operation, 8-digit × 2 line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 DB0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5×7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0		Writes "H". The DD RAM has has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1		Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0		Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data co CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1		Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1		Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1		Sets mode for display shift at the time of write.

13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

MODIFYING CHARACTER PATTERNS

(1) Character Pattern Development Procedure

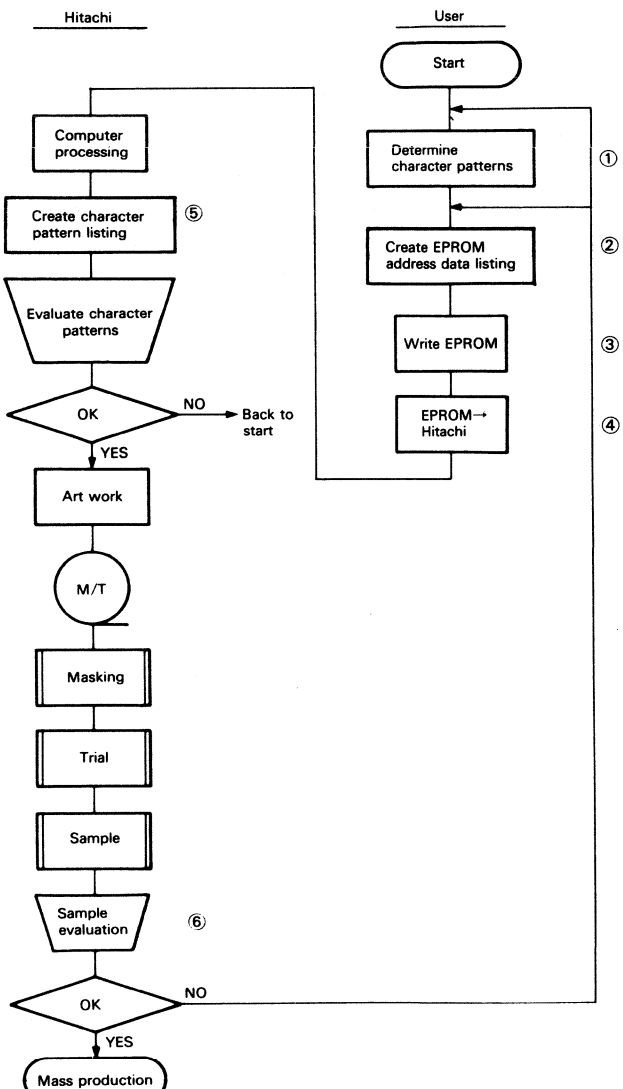


Fig. 15 Character Pattern Development Procedure

The numbers in the above figure correspond to the following operations:

(1) Determine the correspondence between character codes and character patterns.

(2) Create a listing indicating the correspondence between EPROM addresses and data.

(3) Program character patterns in the EPROM.

(4) Send the EPROM to Hitachi.

(5) Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

(6) If there is no problem in the character pattern listing, Hitachi creates LSI for trial and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, mass production of LSI is started.

2. Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II character generator ROM can generate 160 5 × 7-dot character patterns and 32 5 × 10-dot character patterns in total of 192 different character patterns.

2.1 5 × 7-dot Character Pattern

For a 5 × 7-dot character pattern, EPROM address data and character pattern correspond with each other as shown below. Table 10 Example of correspondence between EPROM address data and character pattern (5 × 7 dots).

Table 10 Example of Correspondence between EPROM Address Data and Character Pattern (5 x 7 dots)

EPROM address											Data				
															(LSB)
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
								0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
0	1	0	1	0	0	1	0	0	1	1	1	1	1	1	0
								1	0	0	1	0	0	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Fill line 8 (cursor position) with 0.

Character code — Line position

(1) EPROM addresses A_{10} to A_3 correspond to a character code.

(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.

(3) EPROM data O_4 to O_0 correspond to character pattern data.

(4) A lit display position (black) corresponds to "1".

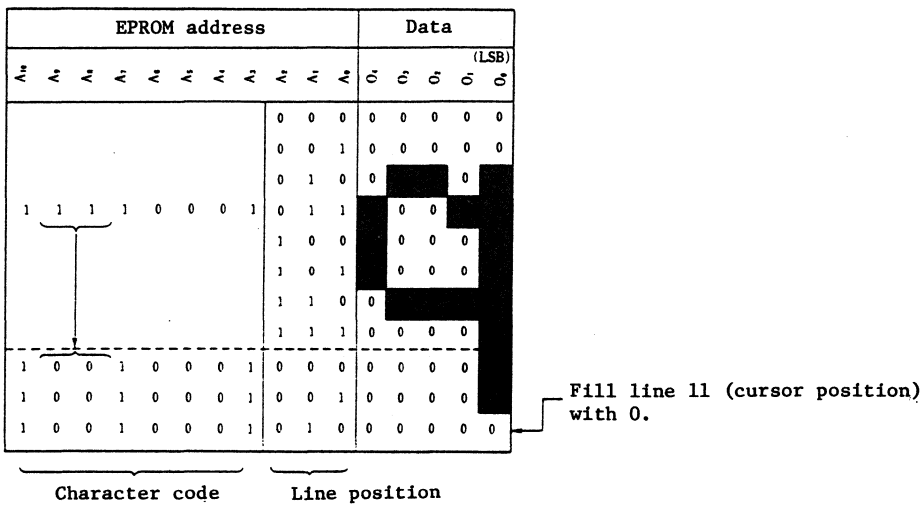
(5) Fill line 8 (cursor position) of character pattern with 0.

(6) EPROM data O_5 to O_7 are not used.

2.2 5 × 10-dot Character Pattern

For a 5 × 10-dot character pattern, EPROM address data and character pattern correspond with each other as shown below.

Table 11 Example of Correspondence between EPROM Address Data and Character Pattern (5 x 10 dots)



(1) EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern line 9 and later lines to 0.

(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.

(3) EPROM data O_4 to O_0 correspond to character pattern data.

(4) A lit display position (black) corresponds to "1".

(5) Fill line 11 (cursor position) of character pattern with 0.

(6) EPROM data O_5 to O_7 are not used.

2.3 Handling Unused Character Patterns

(1) EPROM data outside the character pattern area
It is ignored by the character generator ROM for display operation so that it can be 0 or 1.

(2) EPROM data in CG RAM area
It is ignored by the character generator ROM for display operation so that it can be 0 or 1.

(3) EPROM data used when the user does not use any LCD-II character pattern

It is handled in one of the two ways explained below.

Select one of the two ways according to the user application.

1) When unused character patterns are not programed

If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1 when the EPROM is erased.)

2) Program 0 for unused character patterns

Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (It is equivalent to space.)

HD66780 (LCD-IIA)

(Dot Matrix Liquid Crystal Display Controller and Driver)

Description

The LCD-IIA (HD66780)is a dot matrix liquid crystal display controller and driver LSI that displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microcontroller or microprocessor control. All the functions required for driving a dot matrix liquid crystal display are internally provided on one chip.

Designers can complete dot matrix liquid crystal display systems with fewer chips by using the LCD-IIA (HD66780). If a driver LSI (HD44100H or HD66100F) is connected to the HD66780, up to 80 characters can be displayed.

The LCD-IIA is produced by the CMOS process. Therefore, the combination of the LCD-IIA with a CMOS microcontroller or microprocessor can complete a portable battery-driven device with low power dissipation.

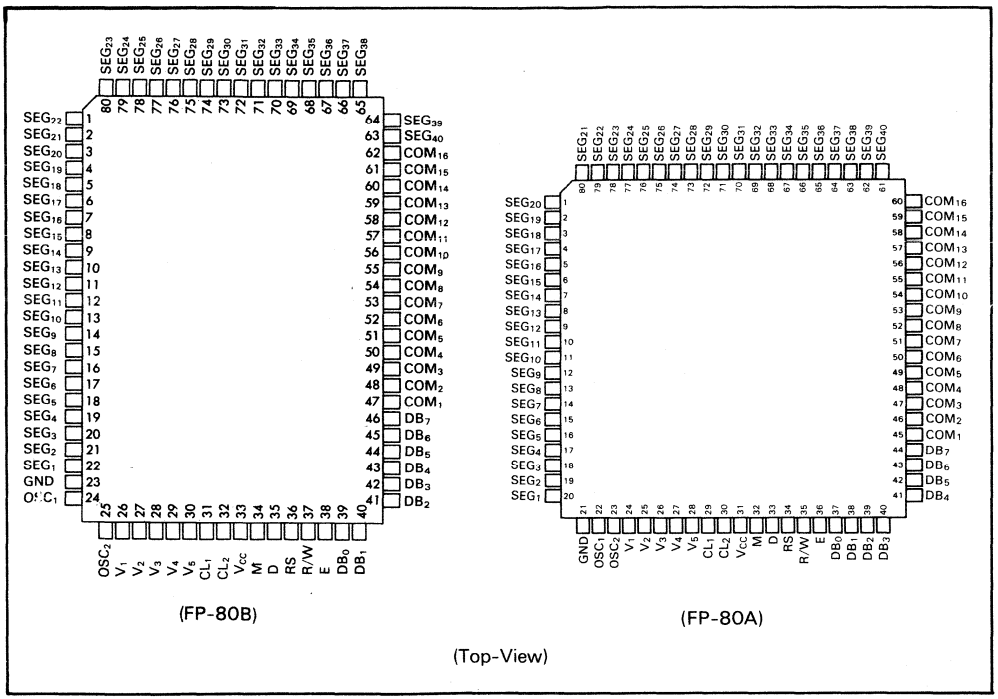
Features

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Can interface to 4-bit or 8-bit MPU
- Display data RAM : 80 × 8 bits (80 characters, max)
- Character generator ROM : 12000 bits ; Character font 5×10 dots : 240 characters
- Character generator RAM : 64 × 8 bits ; Character font 5×8 dots : 8 characters or character font 5 × 11 dots : 4 characters
- Both display data and character generator RAMs can be read from the MPU.
- Internal liquid crystal display driver
  −16 common signal drivers
  −40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H or HD66100F)
- Duty factor selection (selectable by program).
  −1/8 duty: 1 line of 5 × 7 dots + cursor
  −1/11 duty: 1 line of 5 × 10 dots + cursor
  −1/16 duty: 2 lines of 5 × 7 dots + cursor
- Maximum number of display characters as shown in table 1
- Wide range of instruction functions : Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Internal automatic reset circuit at power on (internal reset circuit)
- Internal oscillation circuit
  −External resistor or ceramic filter
  −External clock operation possible
- CMOS process
- Single +5V logic power supply (excluding power for liquid crystal display drive)
- Operation temperature range : -20°C to + 75°C (-40°C to +85°C device available upon request)
- 80-pin plastic flat package (FP-80, FP-80A)
- Low power consumption

Ordering Information

Type No.	Package
HD66780FS	80-pin plastic QFP (FP-80B)
HD66780FH	80-pin plastic QFP (FP-80A)

Pin Arrangement



Pin Description

Signal	No. of Lines	I/O	Connected to	Function
RS	1	Input	MPU	Selects register
R/W	1	Input	MPU	Selects read or write
E	1	Input	MPU	Starts data read or write
DB_7-DB_0	8	I/O	MPU	Bidirectional data bus
CL_1	1	Output	Driver LSI	Serial data latch clock
CL_2	1	Output	Driver LSI	Serial data shift clock
M	1	Output	Driver LSI	LCD waveform AC switch signal
D	1	Output	Driver LSI	Character pattern data
COM_1-COM_{16}	16	Output	LCD	Common signals
SEG_1-SEG_{40}	40	Output	LCD	Segment signals
V_1-V_5	5		Power supply	LCD drive voltages
V_{CC}, GND	2		Power supply	+5V and ground
OSC_1-OSC_2	2			System clock

Pin Function

RS (Register Select)

RS selects the register that the MPU is accessing. RS=0 selects the instruction register for MPU writes, and the busy flag and address counter for reads. RS=1 selects the data register for MPU reads and writes.

R/W (Read/Write)

R/W selects whether the MPU will read from (R/W=1) or write to (R/W=0) the LCD-IIA.

E (Enable)

The MPU sets the E input high to signal the start of the read/write operation.

DB_7–DB_0 (Data Bus)

The bidirectional, three-state data bus, DB_0–DB_7, transfers data between the MPU and the LCD-IIA. DB_7 can be used as the busy flag. The lower-order four lines, DB_0-DB_4, are not used in four-bit interface operation.

CL_1, CL_2 (Clock 1, Clock 2)

The CL_1 output signals the HD44100H or HD 66100F driver LSI to latch the serial data sent on line D. The CL_2 output signals it to shift the data.

M (Master AC Signal)

The HD44100H or HD66100F driver LSIs use the M output to convert the LCD drive waveform to AC.

D (Serial Data)

The LCD-IIA outputs serial character pattern data corresponding to the common signals to the HD44100H or HD66100F driver LSIs on D.

COM_1–COM_{16} (Common)

COM_1-COM_{16} are the LCD common lines. Common signals that are not used are deselected. At 1/8 duty factor COM_9-COM_{16} are not used, so they output non-selected waveforms. At 1/11 duty factor COM_{12}-COM_{16} are not used, so they output non-selected waveforms.

SEG_1–SEG_{40} (Segment)

SEG_1-SEG_{40} are the LCD segment lines.

V_1–V_5 (LCD Voltages)

The LCD-IIA requires the V_1-V_5 voltages to output LCD-driving waveforms.

V_{CC}, GND (Power Supply, Ground)

V_{CC} is the LCD-IIA's logic power supply. GND is the power supply ground.

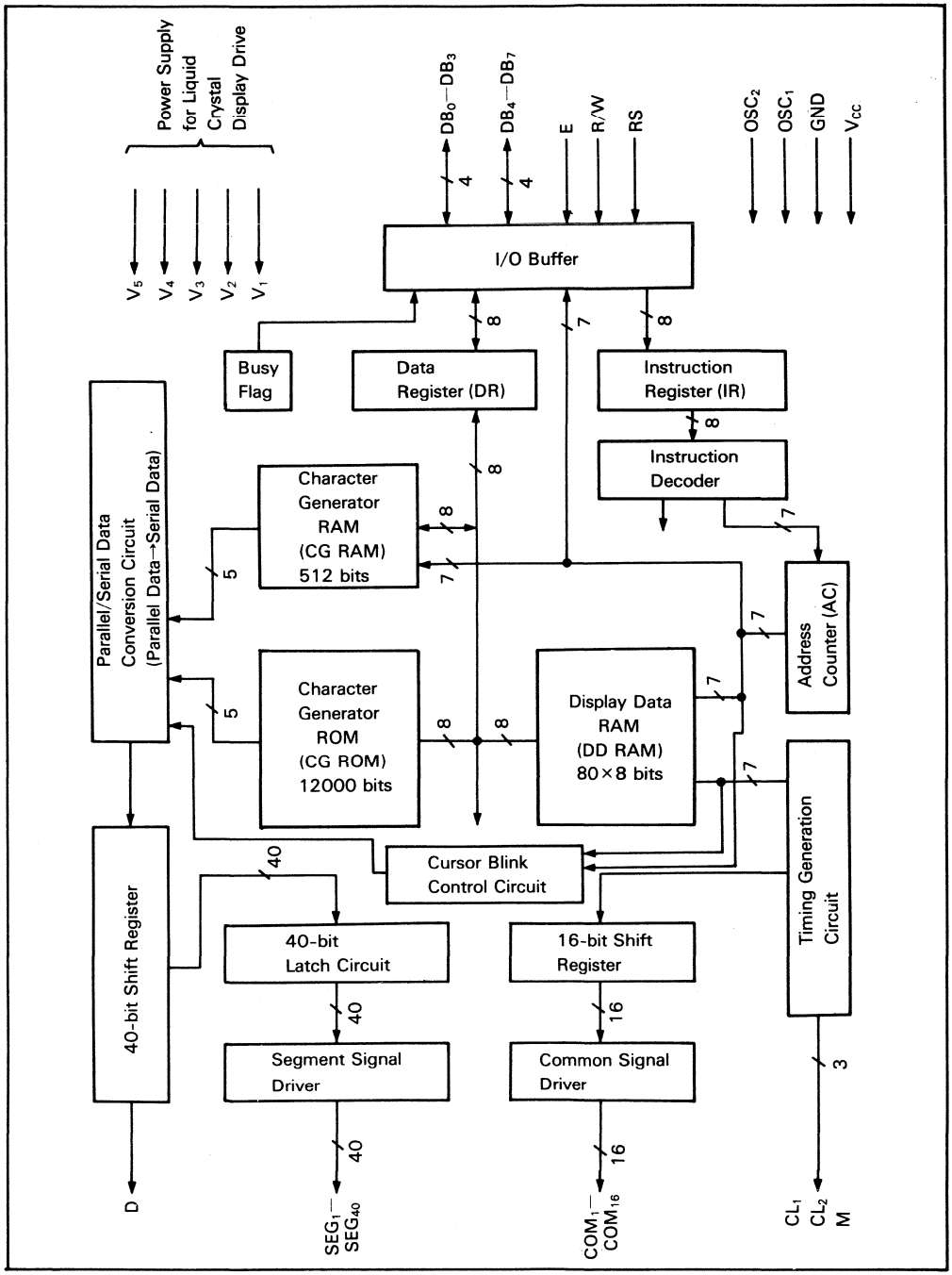
OSC_1, OSC_2 (Oscillator 1, Oscillator 2)

OSC_1 and OSC_2 are the connections for the LCD-IIA system clock. The LCD-IIA can use its internal oscillator if OSC_1 and OSC_2 are connected to a resistor or ceramic filter. An external clock can be input to OSC_1.

Table 1. Number of Display Characters

No. of Display Lines	Duty factor	Extension	HD44100H	HD66100F	No. of Display Characters
1-line display	1/8, 1/11 duty	Not provided	–	–	8 characters×1 line
		Proveded	9 pcs. (8 characters/pc.)	5 pcs. (16 characters/pc.)	80 characters × 1 line
2-line display	1/16 duty	Not provided	–	–	8 characters × 2 lines
		Provided	4 pcs.(8 characters × 2 lines/pc.)	2 pcs.(16 characters × 2 lines/pc.)	40 characters × 2 lines

HD66780 Block Diagram



Block Function

Registers

The HD66780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM internally. The MPU also uses the DR for data storage when reading data from the DD RAM or the CG RAM. When the MPU writes address information into the IR, the LCD-IIA sends data to the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, the LCD-IIA sends data in the DD RAM or CG RAM at the next address to the DR for the next read from the MPU. Register selector (RS) signals select these two registers (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66780 is in the internal operation mode, and instructions will not be accepted. As table 2 shows, the busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after confirming that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD and CG RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.
After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by 1
(or decremented by 1). AC contents are output to DB_0-DB_6 when RS=0 and R/W=1, as shown in table 2.

Display Data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown in figure 1.
The DD RAM adress (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.

When there are fewer then 80 display characters, the display begins at the head positon. For example, 8 characters using an HD66780 are displayed as shown in figure 2.

When the display shift operation is performed, the DD RAM address moves as shown in figure 3.

A 16-character display using an HD66780 and an HD44100H is shown in figure 4.

The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD66780 and two or more HD44100Hs can be considered an extension of figure 4.

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be

Table 2. Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc)
0	1	Read busy flag (DB_7) and address counter (DB_0-DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

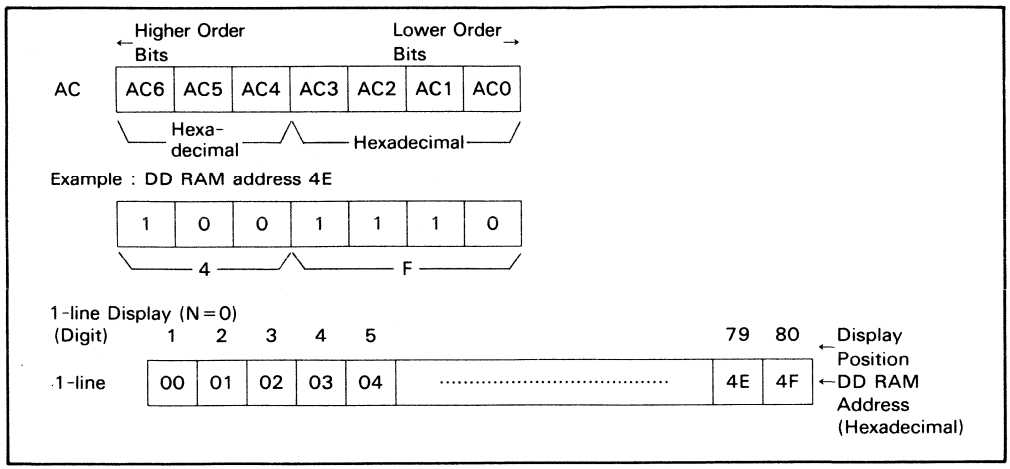


Figure 1. DD RAM Address

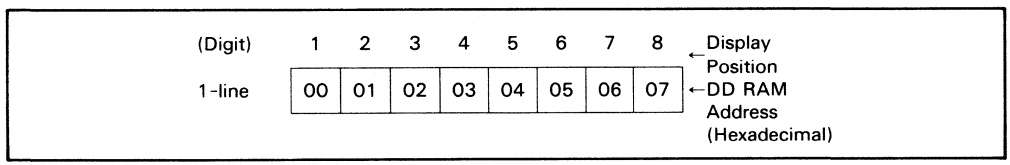


Figure 2. Eight-Character Display Example

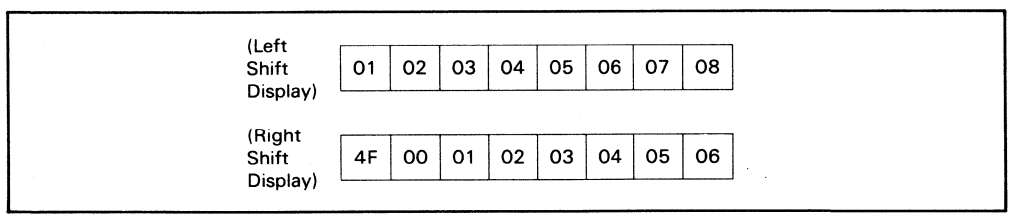


Figure 3. Display shift

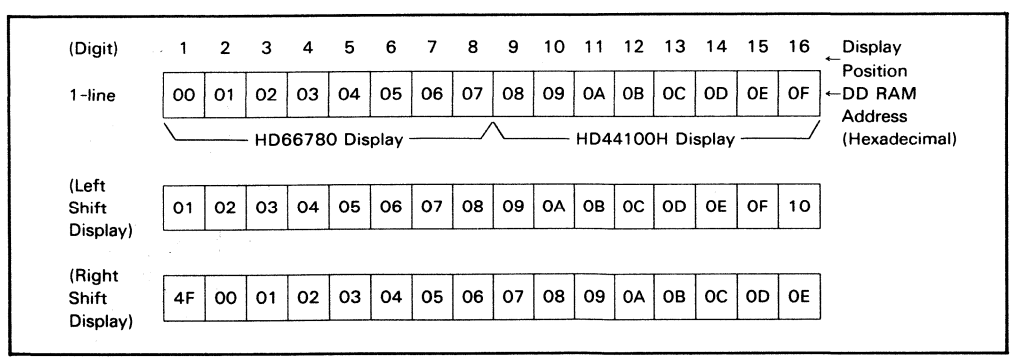


Figure 4. Sixteen-Character Display Example

displayed by externally connecting 9 HD44100Hs.
The same holds when HD66100Fs are used as display drivers. Consisting of 80 outputs, one HD66100F can display 16 digits (figure 5).

When the number of display characters is fewer than 40×2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD66780 is used, 8 characters × 2 lines are displayed as shown in figure 6.

When display shift is performed, the DD RAM address moves as shown in figure 7.

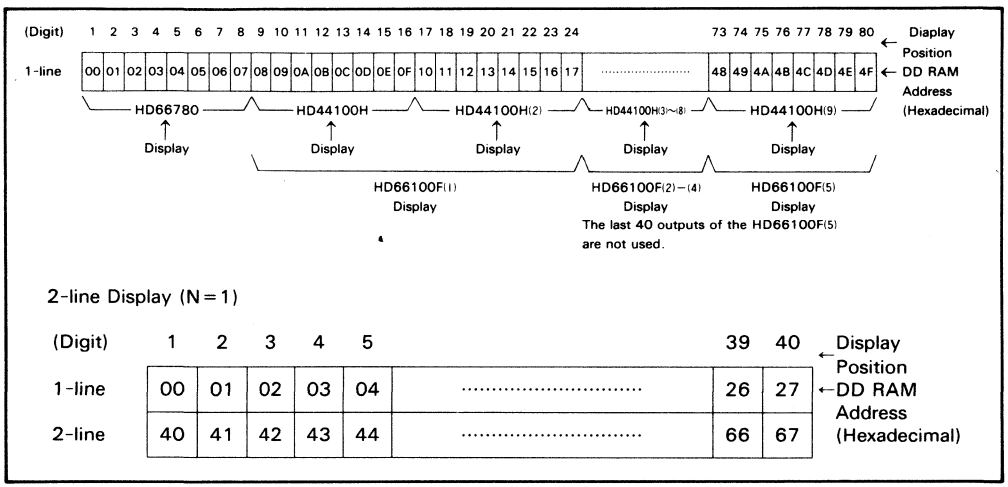


Figure 5. Extended Display

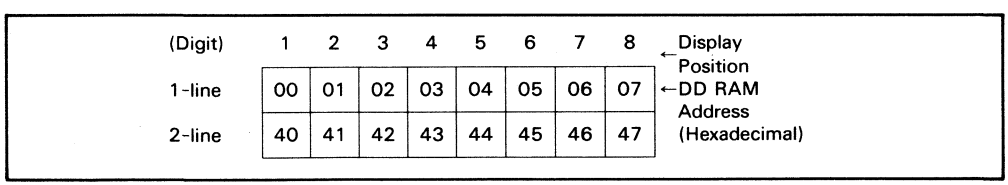


Figure 6. Two-Line by Eight-Chasrcter Display Example

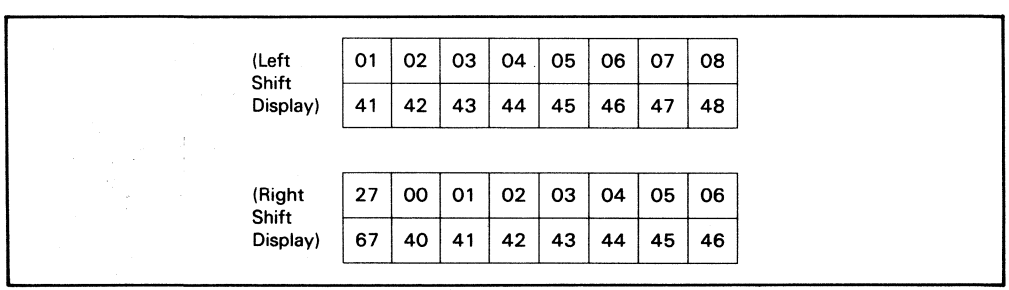


Figure 7. Two-Line Display Shift

16 characters × 2 lines are displayed as in figure 8 when an HD66780 and an HD44100H are used.

The relation between diaplay position and DD RAM address when the number of display digits is increased by using one HD66780 and two or more HD44100Hs, can be considered an extension of figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits × 2 lines can be displayed by connecting 4 HD66780s (or 2 HD66100Fs) externally.

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8 -bit character codes. A CG ROM has 240 types of 5 × 10 dot character patterns built-in. (Note; In a 5 × 7 dot + cursor display, only the upper part, that is, 5 × 7 dots of 5 × 10 dots, is displayed.)

Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD66780A00. User-defined character patterns are also available by mask -programming ROM.

Character Generator RAM (CG RAM)

With the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots 4 patterns can be written.

Write the character codes in the left columns of table 3 to display character patterns stored in CG RAM.

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	(Hexadecimal)
	HD66780 Display								HD44100H Display								
(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	
(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

Figure 8. Two-Line by Sixteen-Charater Display Example

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	.....	33	34	35	36	37	38	39	40	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	.....	20	21	22	23	24	25	26	27	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	.....	60	61	62	63	64	65	66	67	(Hexadecimal)
	HD667780 Display								HD44100H(1) Display												HD44100H(2)(3) Display								HD44100H(4) Display	
									HD66100F(1) Display																				HD66100F(2) Display	

Figure 9. Two-Line Extended Display Example

Table 3. Correspondence between Character Codes and Character Pattern (Hitachi Standard HD66780A00)

Lower 4Bits \ Higher 4Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
××××0000	CG* RAM (1)															
××××0001	(2)															
××××0010	(3)															
××××0011	(4)															
××××0100	(5)															
××××0101	(6)															
××××0110	(7)															
××××0111	(8)															
××××1000	(1)															
××××1001	(2)															
××××1010	(3)															
××××1011	(4)															
××××1100	(5)															
××××1101	(6)															
××××1110	(7)															
××××1111	(8)															

Note: * The user can specify any pattern for character-generator ROM.

Table 4 shows the relation between CG RAM addresses and data and display patterns.

As table 4 shows, an area that is not used for display can be used as general data RAM.

Table 4. Relation between CG RAM Address and Character Codes (DD RAM) and Character Patterns (CG RAM Data) (Cont)

For 5 × 7-dot character patterns

Character Codes (DD RAM Data)	CG RAM Address	Character Patterns (CG RAM Data)
7 6 5 4 3 2 1 0 Higher ←Order Bits Lower Order → Bits	5 4 3 2 1 0 Higher ←Order Bits Lower Order → Bits	7 6 5 4 3 2 1 0 Higher ←Order Bits Lower Order → Bits
0 0 0 0 * 0 0 0	0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * 0 0 0 0 0
0 0 0 0 * 0 0 1	0 0 1 0 0 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * 0 0 0 0 0
0 0 0 0 * 1 1 1	1 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * * * *

Character Pattern Example (1)

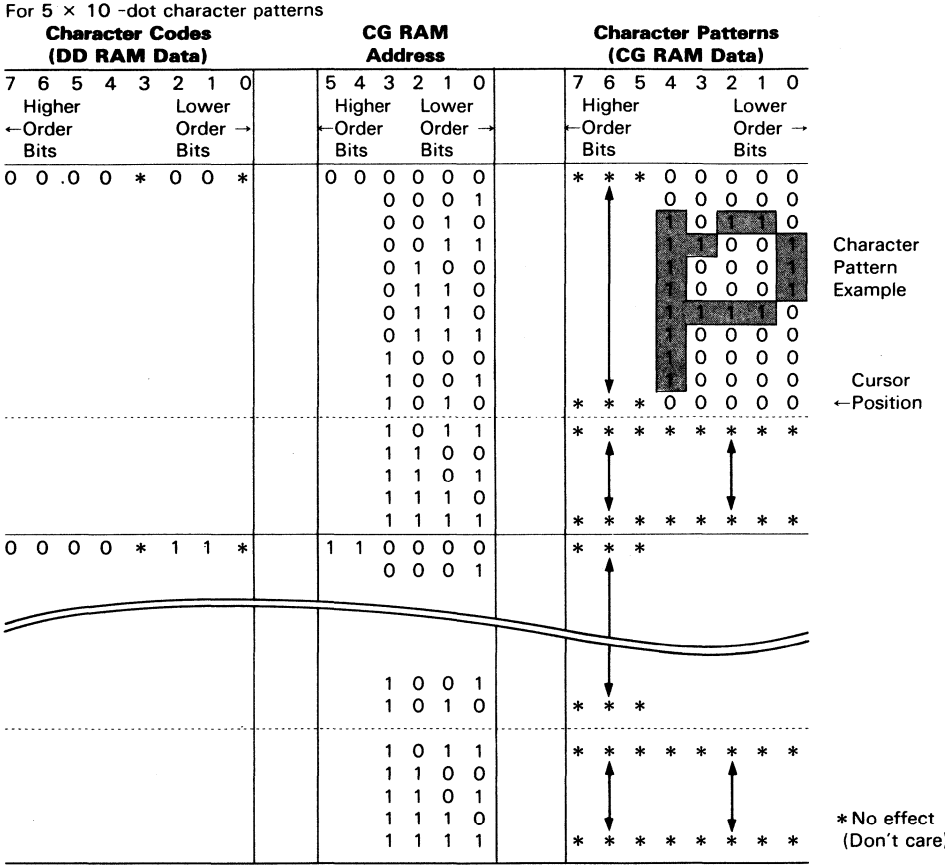
Cursor ←Position

Character Pattern Example (2)

*No effect (Don't Care)

Notes: 1. Character code bits 0-2 correspond to CG RAM address bits 3-5 (3 bits: 8 types).
2. CG RAM address bits 0-2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor.
Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor existence.
3. Character pattern row positions correspond to CG RAM data bits 0-4, as shown in the figure (bit 4 being at the left end).
Since CG RAM data bits 5-7 are not used for display, they can be used for the general data RAM.
4. As shown in table 3 and 4, CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 3 is ineffective, the R display in the character pattern example, is selected by character code 00 (hexadecimal) or 08 (hexadecimal).
5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

For 5 × 10 -dot character patterns



Notes: 1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 patterns).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is performed by logical OR with cursor.
Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor existence. Since the 12nd-16th lines are not used for display, they can be used for the general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 are ineffective, P display in the character pattern example is selected by character code 00, 01, 08 and 09 (hexadecimal).
5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

Timing generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so that they may not interfere with each other. Therefore, when writing data to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected drivers (HD44100H or HD66100F).

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms. The other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data can be sent to HD44100H or HD66100Fs, externally connected in cascade, to diaplay an extended number of characters.

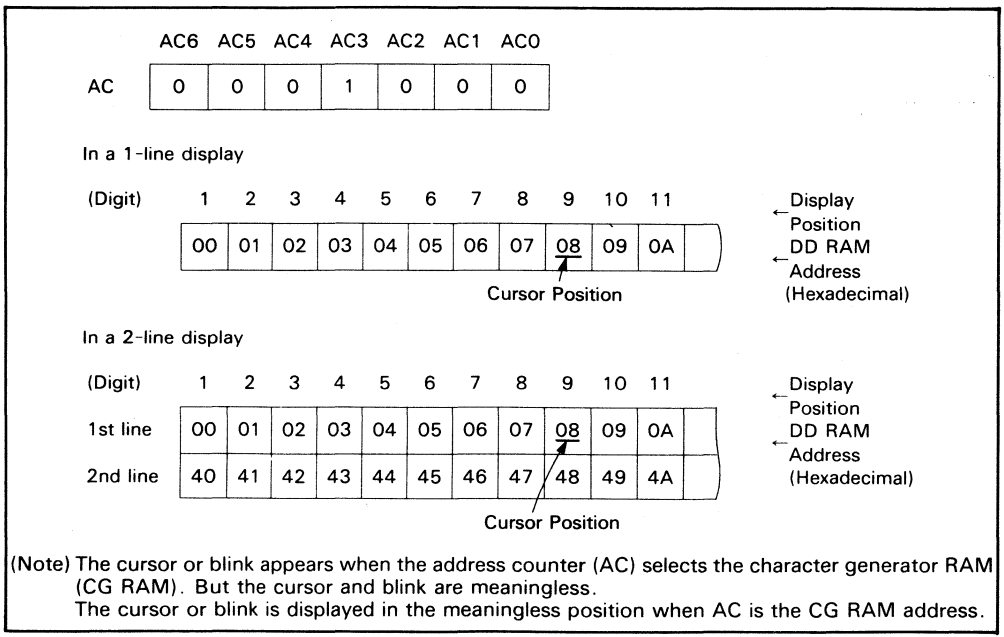
The LCD-IIA always starts sending serial data at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD66780 drives the head of the display. The rest of the display, corresponding to later addresses, are added with each additional HD44100H or HD66100F.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or blinking. The cursor or blinking appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, a cursor position is as shown in figure 10.



(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

Figure 10. Cursor or Blink

MPU Interface

The HD66780 can send data in either 2 4-bit operations or 1 8-bit operation so it can interface to both 4-and 8-bit MPU's.

When interface data is 4 bits long, data is transferred using only 4 bus lines: DB_4–DB_7. DB_0–DB_3 are not used. Data transfer between the HD66780 and the MPU completes when 4 -bit data is transferred twice.

Data of the higher order 4 bits (contents of DB_4 –DB_7 when interface data is 8 bits long) is transfer-red first, then the lower order 4 bits (contents of DB_0–DB_3 when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bits data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data (figure 11).

When interface is 8 bits long, data is transferred using the 8 data bus lines DB_0–DB_7.

Reset Function

Initializing by Internal Reset Circuit

The HD66780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed at initialization. The busy flag (BF) is kept in busy state until initialization ends (BF=1). The busy state lasts 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set
   a. DL = 1: 8-bit long interface data
   b. N = 0: 1-line display
   c. F = 0: 5×7-dot character font
3. Display on/off control
   a. D = 0: Display off
   b. C = 0: Cursor off
   c. B = 0: Blink off
4. Entry mode set
   a. I/D = 1: + 1(increment)
   b. S = 0: No shift

Note: When conditions in power supply conditions using internal reset circuit in the electircal characteristics are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to initializing by instruction.

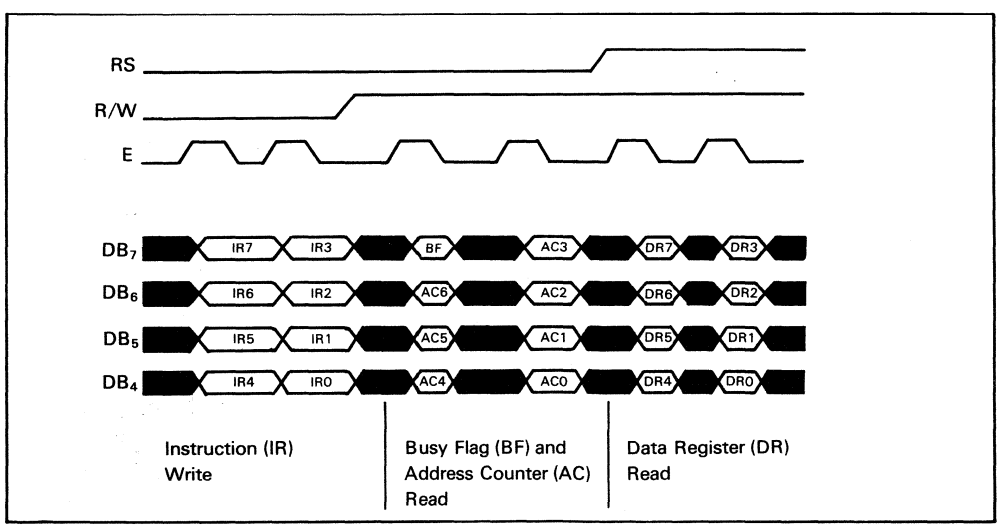


Figure 11. 4-Bits Data Transfer Example

Instructions

Only two HD66780 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD66780 internal operation to various types of MPU's which operate at different speeds or to allow interface to peripheral control IC's. HD66780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W), and data bus signals (DB_0–DB_7), and are here called instructions. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate HD66780 functions such as display format, data length, etc
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of HD66780 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can be performed concurrently with display data write, enabling the disigner to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 7.

During internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is on 0 before sending an instruction from the MPU.

Note: Make sure the HD66780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD66780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction execution time. See table 5 for a list of each instruction's execution time.

Table 5. Inteructions

Instruction	Code RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (Max) (fcp or fosc 250 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read	40 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C), and blink of cursor position character (B)	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts diaplay without changing DD RAM contents	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F)	40 μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	ADD							Set DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents	0 μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	46 μs
Read Data from CG or DD RAM	1	0	Read Data								Reads data from DD RAM or CG RAM	46 μs

Notes: 1

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
S = 1: Display shift
S/C = 0: Cursor move

BF = 1: Internally operating
BF = 0: Can accept instruction
DD RAM: Display data RAMA
CG RAM: Character generator RAM

A_{CG}: CG RAM address

R/L = 1: Shift to the right
R/L = 0: Shifts to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
F = 1: 5×10 dots, F = 0: 5×7 dots

A_{DD} :DD RAM address
Corresponds to cursor address
AC : Address counter used for both DD and CG RAM

2. * No effect (Don't care)
3. Execution time changes when freguency changes.
   Example: When fcp or fosc is 270 kHz:

$$40\ \mu s \times \frac{250}{270} = 37\ \mu s$$

Clear Display

Clear display (figure 12) writes space code 20 (hexadecimal)(character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it is shifted. In other words, the display disappears and the cursor or blink goes to the left edge of the display (the first line if 2 lines are displayed). Sets I/D = 1 (increment mode) of entry mode. S of entry mode does not change.

Return Home

Return home (figure 13) sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left of the display (the first line if 2 lines are displayed).

Entry Mode Set

I/D: I/D (figure 14) increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM. When writing into or reading out of the CG RAM does not shift. When S = 0, the display does not shift.

Display On/Off Control

D: The display is on when D = 1 and off when D = 0 (figure 15). When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc does not

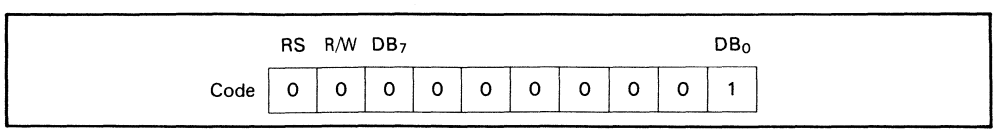


Figure 12. Clear Display Instruction

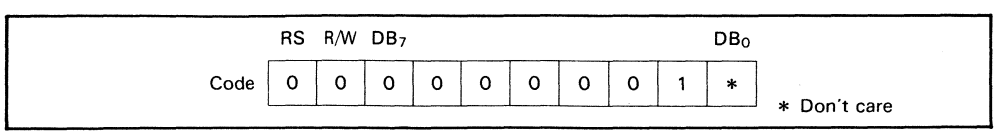


Figure 13. Return Home Instruction

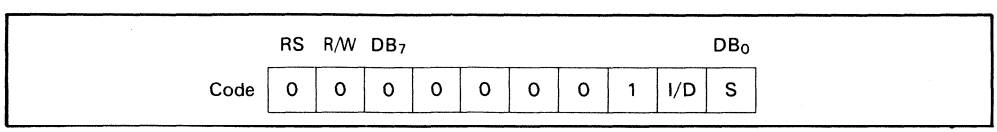


Figure 14. Entry Mode Set Instruction

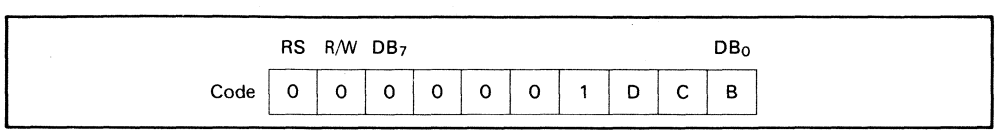


Figure 15. Display On/Off Control Instruction

change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7-dot is selected and 5 dots in the 11th line when the 5× 10-dot character font is selected (figure 16).

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms intervals when fcp or fosc = 250 kHz (figure 15). The cursor and the blink can be set to display simultaneously. (The blink time changes according to the reciprocal of fcp or fosc. For example, 409.6 × $\frac{250}{270}$ = 379.2 ms when fcp = 270 kHz.)

Cursor or Display Shift

Cursor or display shift (figure 17) shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In a 2 -line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

Table 6 shows how S/C and R/L control shifting.
Address counter (AC) contents do not change if the only action performed is shift display.

Function Set

DL: DL (figure 18) sets interface data length. Data is sent or received in 8-bit length (DB_7-DB_0) when DL = 1 and in 4-bit lengths (DB_7-DB_4) when DL = 0.

Table 6. Cursor or Display Shift Control

S/C	R/L	Function
0	0	Shifts the cursor position to the left (AC is decremented by one)
0	1	Shifts the cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift
1	1	Shifts the entire display to the right. The cursor follows the display shift

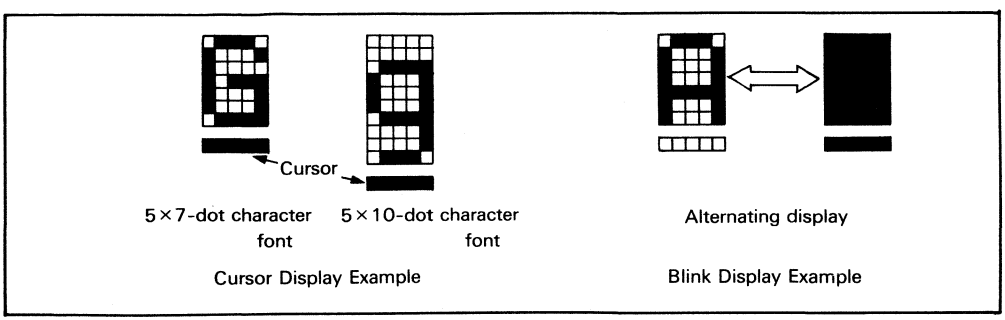


Figure 16. Cursor and Blink Display

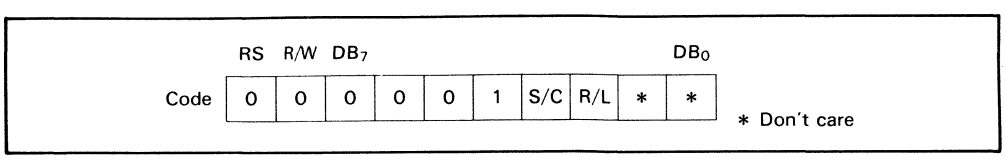


Figure 17. Corsor or Display Shift Instruction

When the 4-bit length is selected, data must be sent or received twice.

N: N sets number of display lines.
F: F sets character font. See table 7.

Note: Perform the function set at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address (figure 19) sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

Set DD RAM Address

Set DD RAM address (figure 20) sets the DD RAM address into the address counter in binary (AAAAAAA). Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is 00-4F (hexadecimal), when N = 1 (2-line display), AAAAAAA is 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

Read Busy Flag and Address

Read busy flag and address (figure 21) reads the busy flag (BF) that indicates the system is now internally operating on a previously received instruction. BF = 1 indicates that internal operation is in progress. The next

Table 7. Function Set N and F

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5×7 dots	1/8	
0	1	1	5×10 dots	1/11	
1	*	2	5×7 dots	1/16	Cannot display 2 lines with 5×10-dot character font.

Note: * Don't care

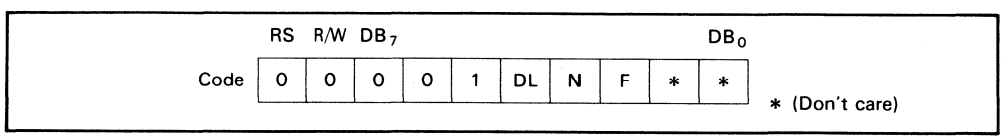


Figure 18. Function Set Instruction

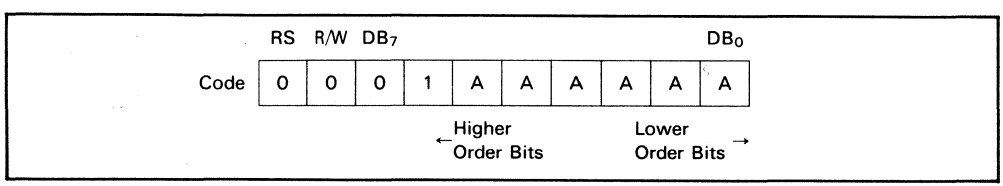


Figure 19. Set CG RAM Address Instruction

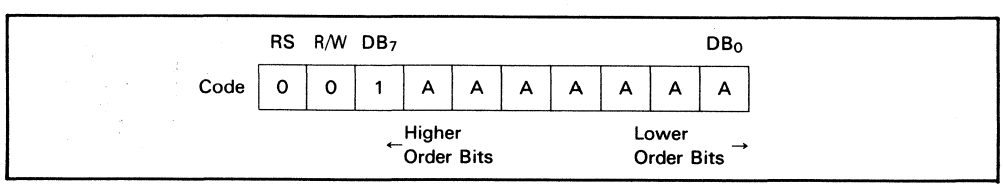


Figure 20. Set DD RAM Address Instruction

instruction will not be accepted until BF is set to 0. Check the BF status before the next write operation (figure 22).

At the same time, the value of the address counter expressed in binary (AAAAAAA) is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in set CG RAM address and set DD RAM address.

Write Data to CG or DD RAM

Write data to CG or DD RAM (figure 23) writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After writing the LCD-IIA automatically increments or decrements the address by 1, according to entry mode.

Read Data from CG or DD RAM

Read data from CG or DD RAM (figure 24) reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you do not the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift instruction (when reading out of DD RAM). The cursor shift instruction operation is the

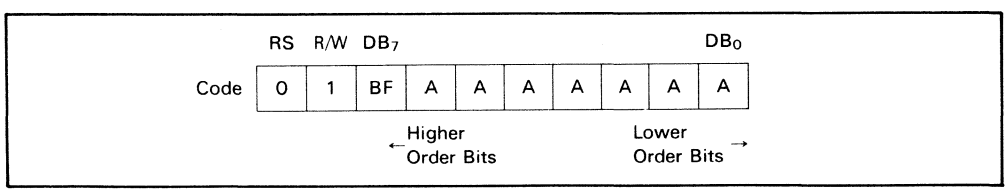


Figure 21. Read Busy Flag and Address Instruction

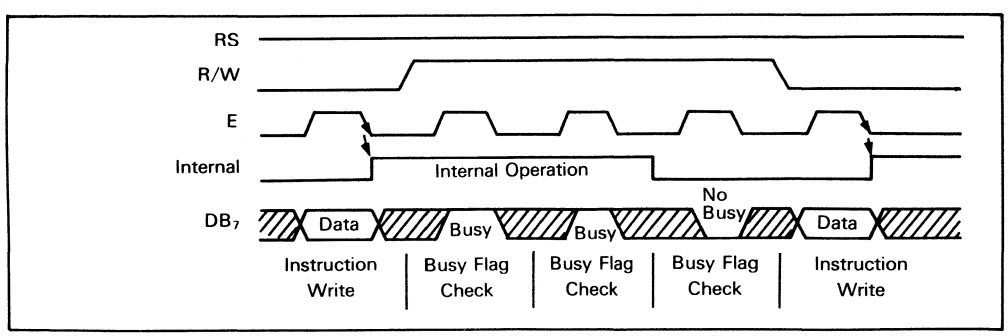


Figure 22. Example of Busy Flag Check Timing Sequence

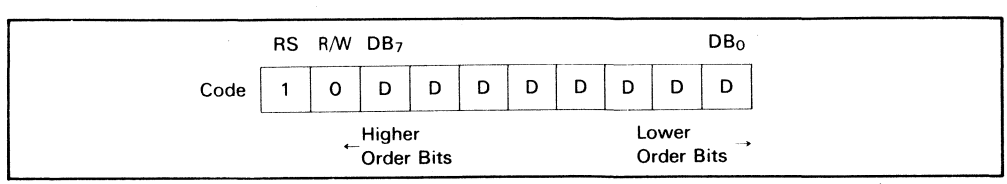


Figure 23. Write Data to CG or DD RAM Instruction

same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display is not shifted no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out, execute the read instruction from the second time the read instruction is serial.

How to Use the HD66780

Interface to 8-Bit MPU

When Connecting to 8-Bit MPU Through PIA: Figure 25 is an example of using a PIA or I/O port (for a microcontroller) as an interface device. Input and output of the device is TTL compatible.
In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/$\overline{W}$ and RS respectively.

Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

Connecting Directly to the 8-Bit MPU Bus: Figure 26 shows the LCD-IIA connected directly to an HD6800.

Example of Interfacing to the HD6805: Figure 27 shows the LCD-IIA connected directly to an HD6805.

Example of Interfacing to the HD6301: Figure 28 shows the LCD-IIA connected directly to an HD6301.

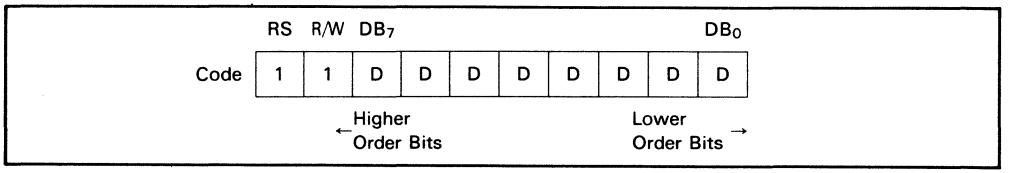


Figure 24. Read Data from CG or DD RAM Instruction

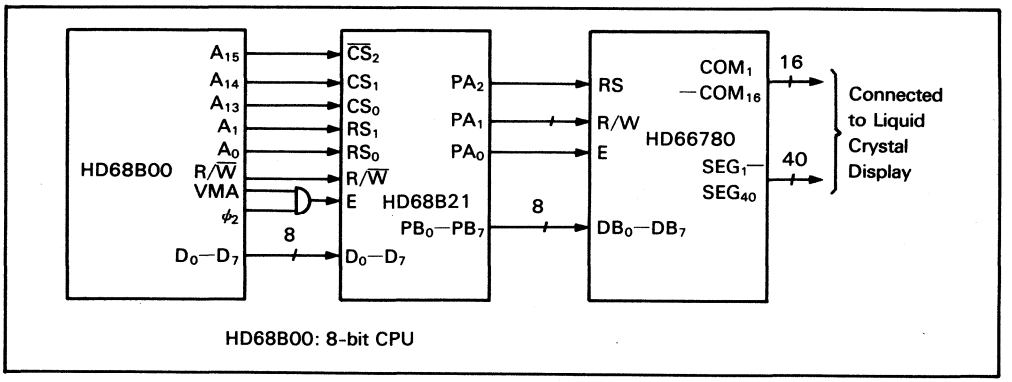


Figure 25. Example of Interface to HD68B00 using PIA (HD68B21)

Interface to 4-Bit MPU

The HD66780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit length, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (designating the interface data length as 4 bits). In the latter case, the timing sequence becomes somewhat complex. (see figure 29)

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

Figure 30 shows an example of an interface to the 400 series.

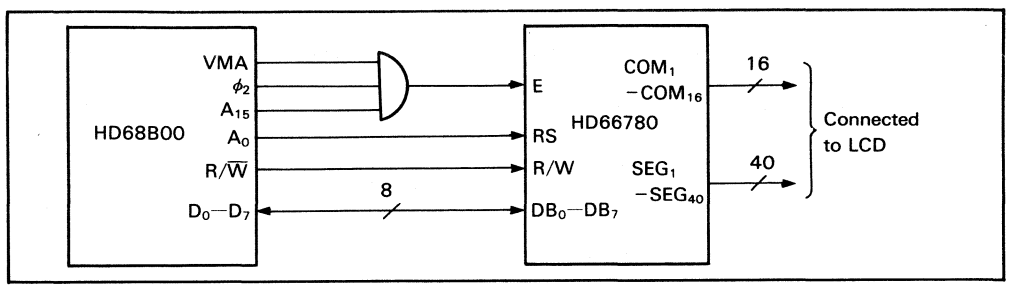


Figure 26. Direct Connection to HD68B00

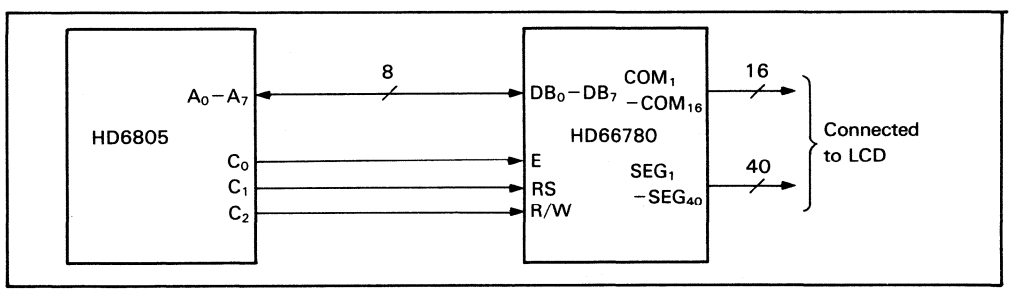


Figure 27. Direct Connection to HD6805

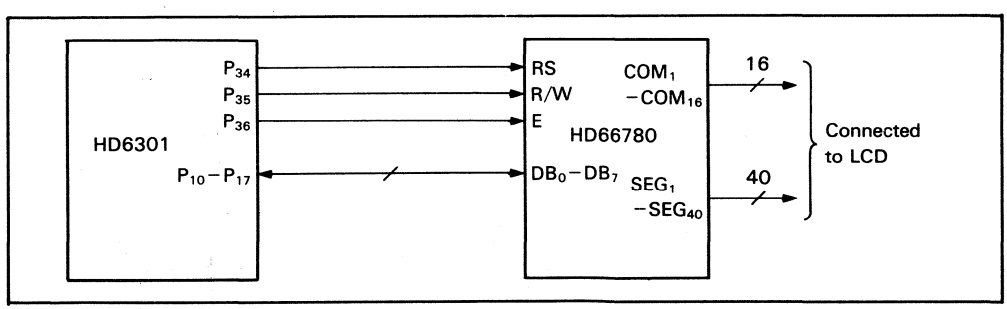


Figure 28. Direct Connection to HD6301

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66780 can perform 2 types of display, using 5 × 7 dots or 5 × 10 dots for the character font, with a cursor on each.

Up to 2 lines can be displayed with 5 × 7 dots and 1 line with 5 × 10 dots.

Therefore, three types of common signals are available (table 8).

Number of lines and font types can be selected by program (see table 5).

Connection to HD66780 and Liquid Crystal Display: Figure 31 shows connection examples. Since 5 SEG signal lines can display one digit, one HD66780 can display up to 8 digits

Table 8. Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 × 7 dots + Cursor	16	1/16

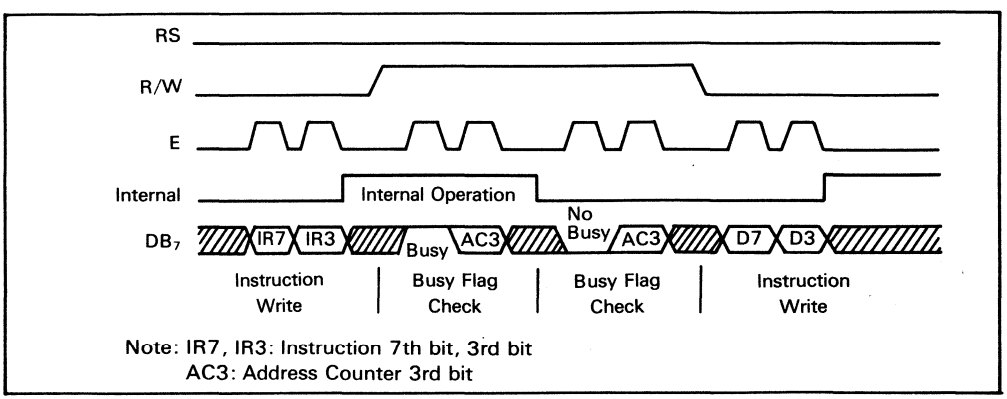


Figure 29. An Example of 4-Bit Data Transfer Timing Sequence

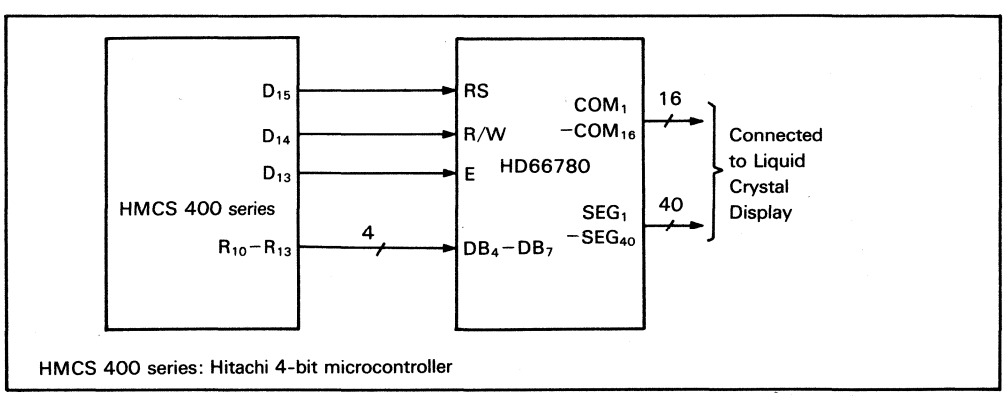


Figure 30. Example of Interface to the 400 Series

for a 1-line display and 16 digits for a 2-line display.
In figure 31 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals (figure 32).

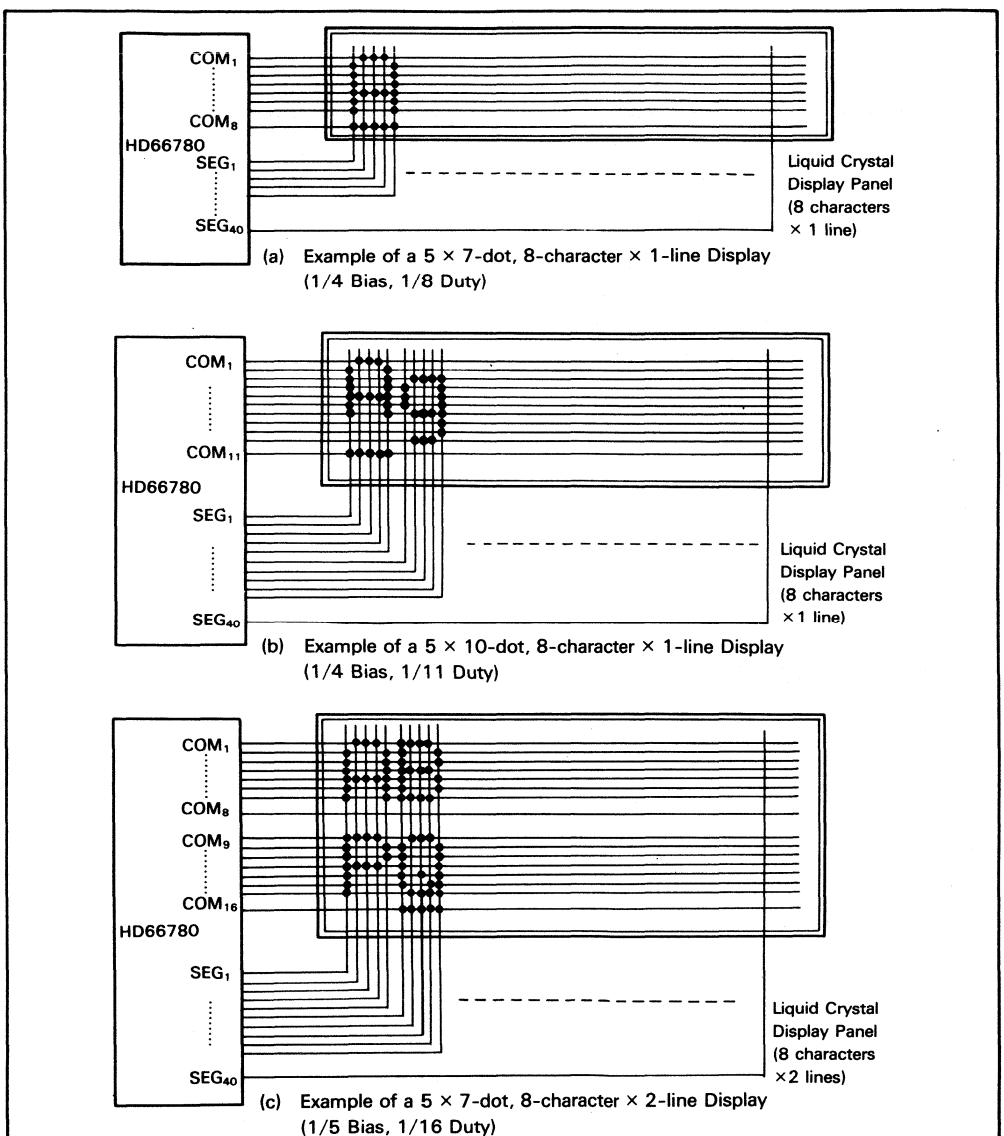


Figure 31. Liquid Crystal Display and Connections to HD66780

Connection for Changed Matrix Layout: In the preceding examples, the number of lines was matched to the number of scanning lines. The display types in figure 33 are possible by changing the matrix layout in the liquid crystal display panel.

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) address for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in figure 31.

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD66780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factors. Table 9 shows the relation.

V_{LCD} gives the peak values for lipuid crystal display drive waveforms. Resistance dividing provides each voltage as shown in figure 34.

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

Figure 35 shows examples of liquid crystal display frame frequency when the oscillation frequency is 250 kHz. (1 clock = 4 μs)

Connection with Driver LSI HD44100H or HD66100F

You can increase the number of display characters by externally connecting liquid crystal display driver LSI's HD44100H or HD66100F to the HD66780.

When connected to the HD66780, the HD44100H or HD66100F is used as a segment signal driver. The HD44100H and the HD66100F can be connected to the HD66780 directly since they supply CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figures 36 and 37 show connection examples.

Note: Connection of voltage supply terminals V_1 through V_6 for the liquid crystal display drive is complicated.

Table 9. Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor	Bias	Power Supply V_1	V_2	V_3	V_4	V_5
1/8,1/11	1/4	V_{CC} - (1/4)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (3/4)V_{LCD}	V_{CC} - V_{LCD}
1/16	1/5	V_{CC} - (1/5)V_{LCD}	V_{CC} - (2/5)V_{LCD}	V_{CC} - (3/5)V_{LCD}	V_{CC} - (4/5)V_{LCD}	V_{CC} - V_{LCD}

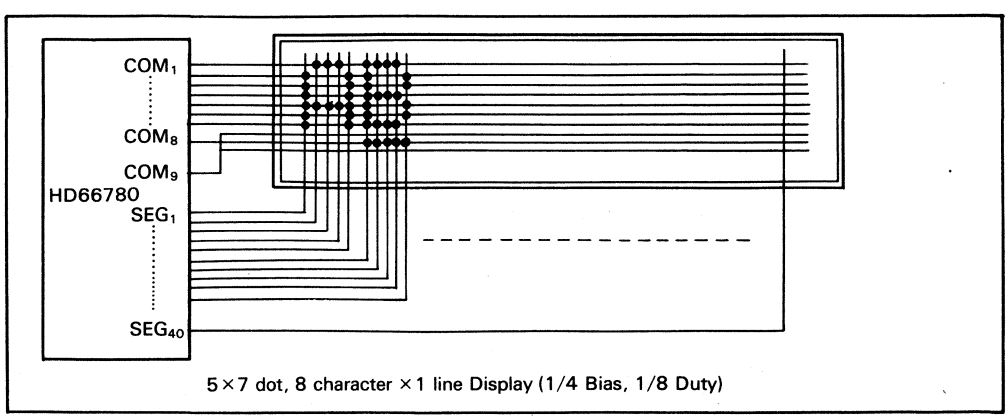


Figure 32. Using COM_9 to Avoid Cross-Talk on Unneeded Scanning Line

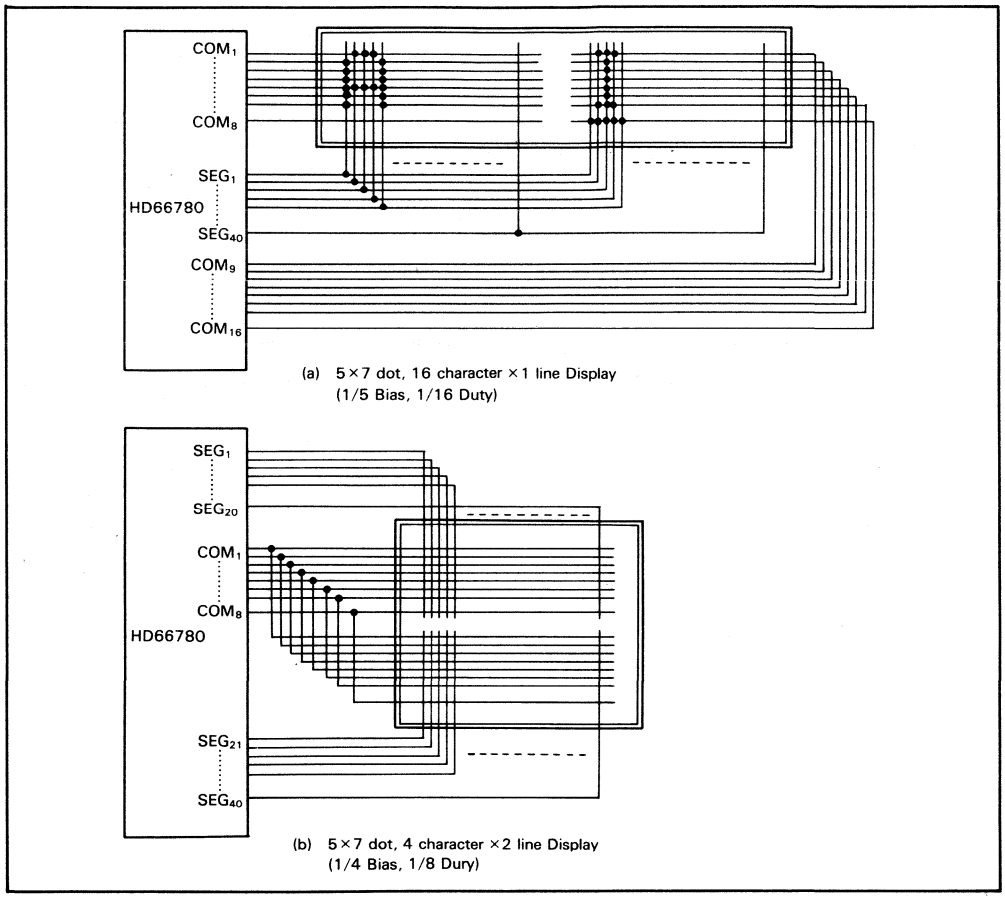


Figure 33. Changed Matrix Layout Displays

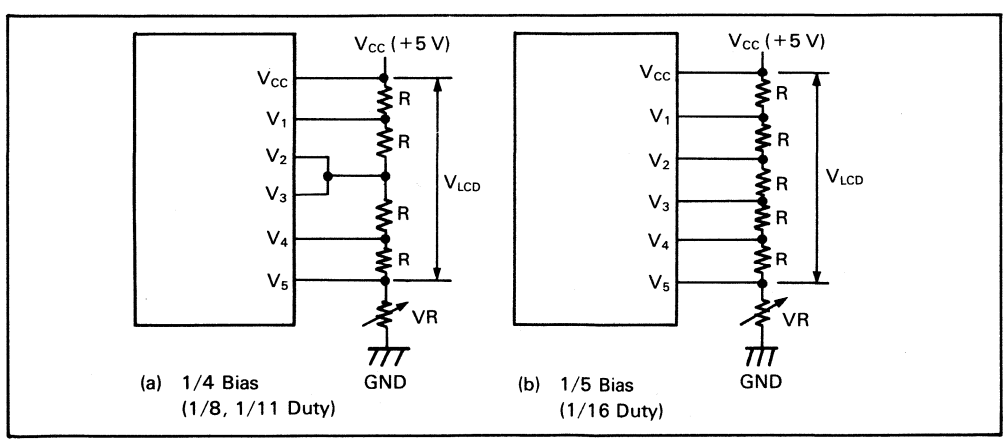
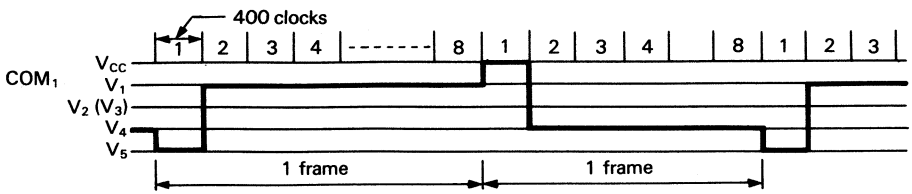


Figure 34. Drive Voltage Supply Example

Up to 9 HD44100Hs can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to 4 for a 2-line display (duty factor 1/16). (For the HD66100F, 5 and 2 units respectively.) RAM size limits the HD66780 to a maximum of 80 character diaplay digits. The connection method in figures 36 and 37 remains unchanged for both 1-line and 2-line display and both 5 × 7-and 5 × 10-dot character fonts.

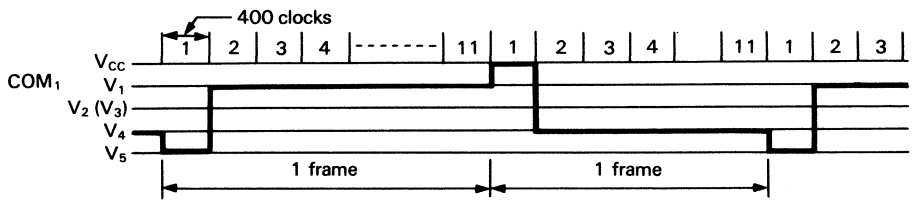
(1) 1/8 Duty



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

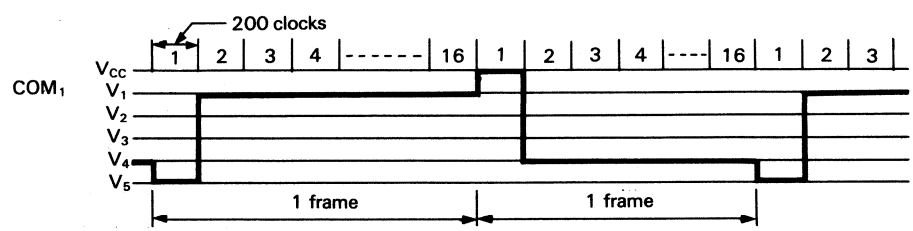
(2) 1/11 Duty



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

Figure 35. Liquid Crystal Display Waveforms (at f_{OSC} = 250kHz)

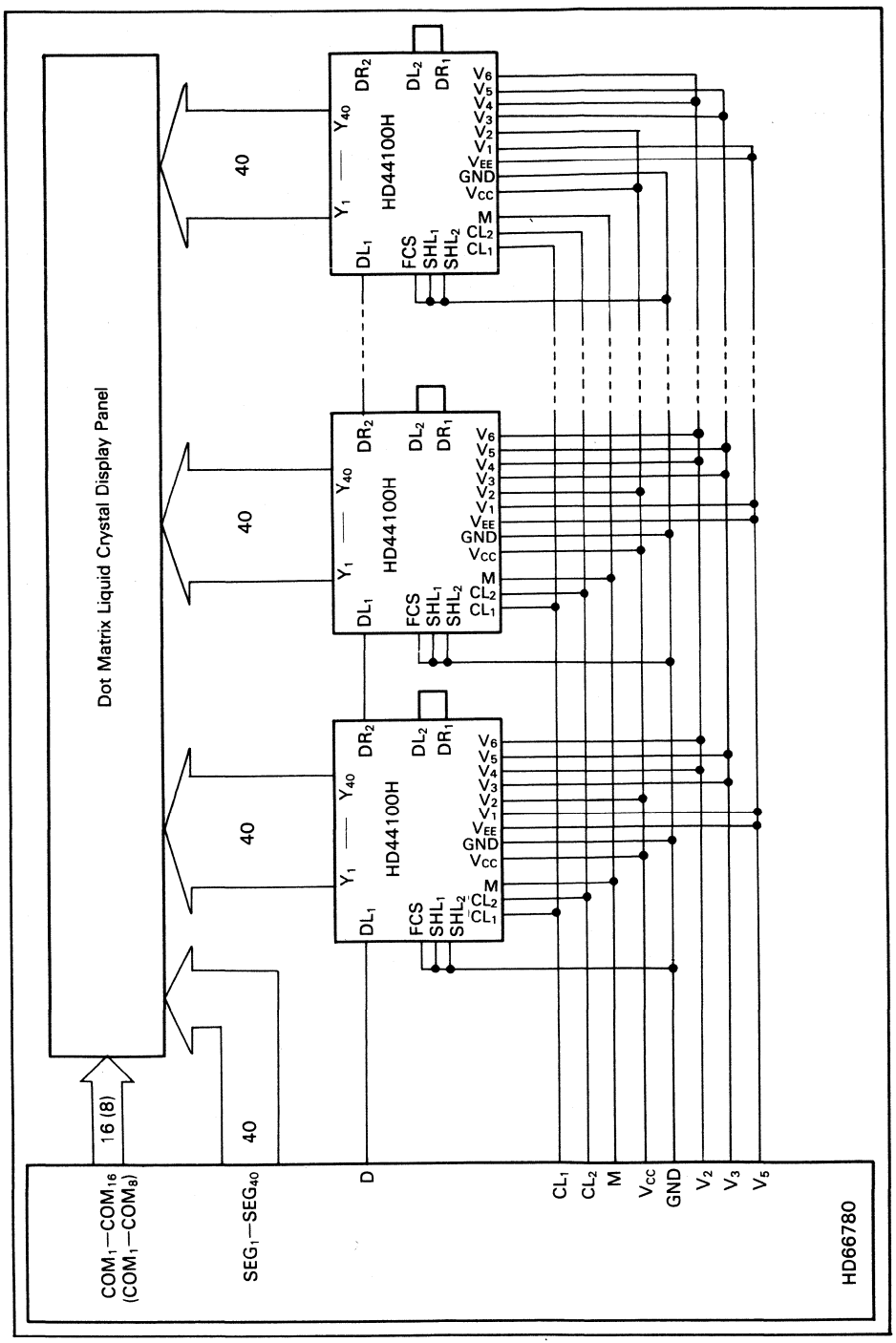


Figure 36. Example of Connecting HD44100H to HD66780

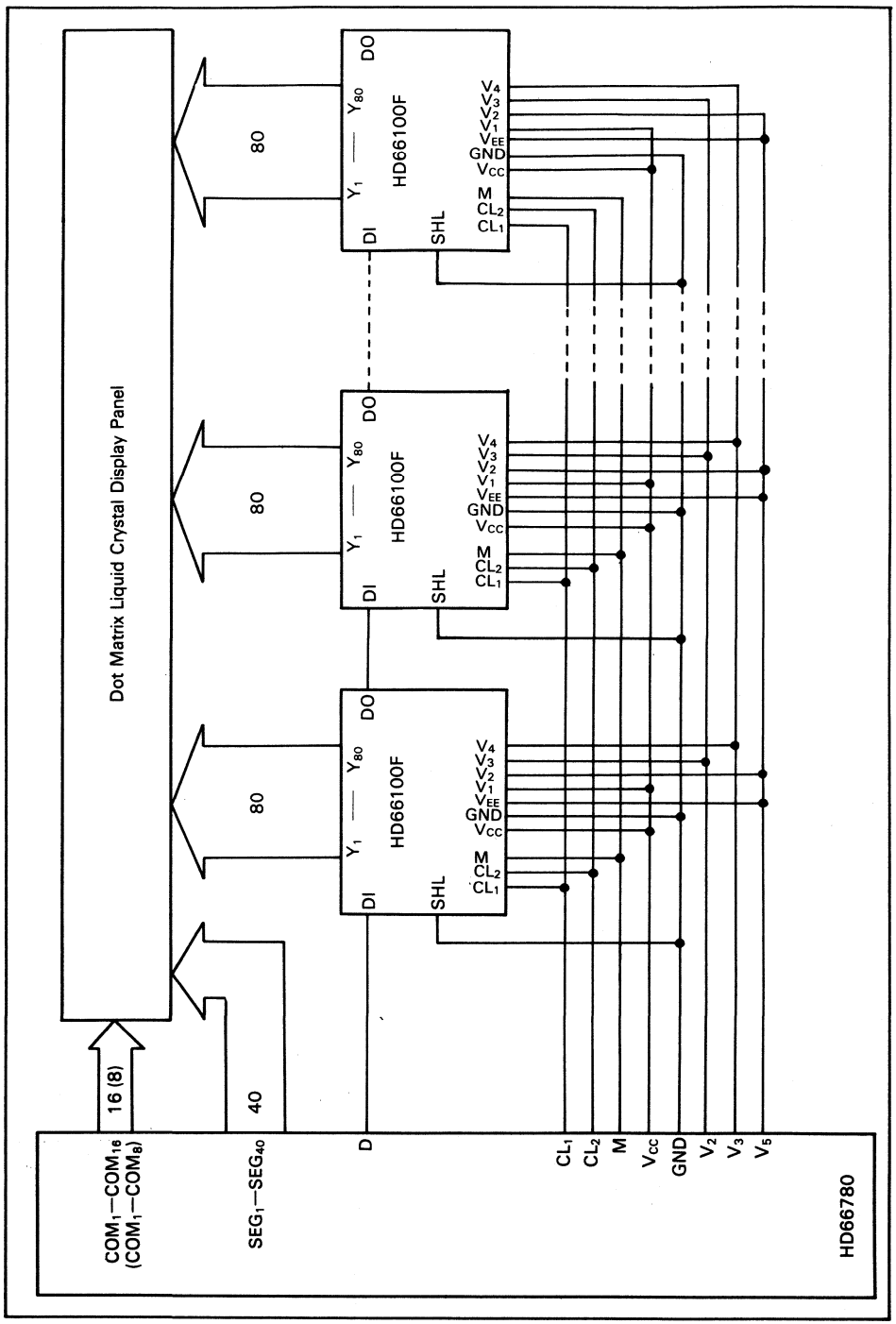


Figure 37. Example of Connecting HD66100F to HD66780

Instruction and Display Correspondence
8-bit Operation, 8-digit × 1-line Display (Using Internal Reset): Table 10 shows an example of an 8-bit × 1-line display in 8-bit operation. The HD66780 functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

4-bit Operation, 8-digit × 1-line Display (Using Internal Reset): The program must set functions prior to 4-bit operation. Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the LCD-IIA attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB_0-DB_3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed to set the functions (see table 11 step 3).

Thus, DB_4-DB_7 of the function set is written twice.

8-bit Operation, 8-digit × 2-line Display: For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set after the eighth character is completed (see table 12). Note that the first and second lines of the display are shifted.

In the example, the display is shifted when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD66780 must be initialized by instruction. (See "Initializing by Instruction")

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the LCD-IIA must be initialized by instruction.
When interface is 8 bits long, use the initialization procedure in figure 38.

When interface is 4 bits long, use the initialization proceduer in figure 39.

Table 10. 8-bit Operation, 8-character × 1-line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bits operation and selects 1-line display and one of the three character fonts. (Number of display lines and character font cannot be changed hereafter.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is on space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI	Writes space.
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO	Shifts only the cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (address 0).

Table 11. 4-bit Operation, 8-character × 1-line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets to 4-bit operation and selects 1-line display and one of the three character fonts. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character font cannot be changed hereafter.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.

Hereafter, control is the same as 8-bit operation.

Table 12. 8-bit Operation, 8-character × 2-line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 · · · DB0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and one of the three character fonts.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor may be positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the left. The first and second lines' shift is operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).

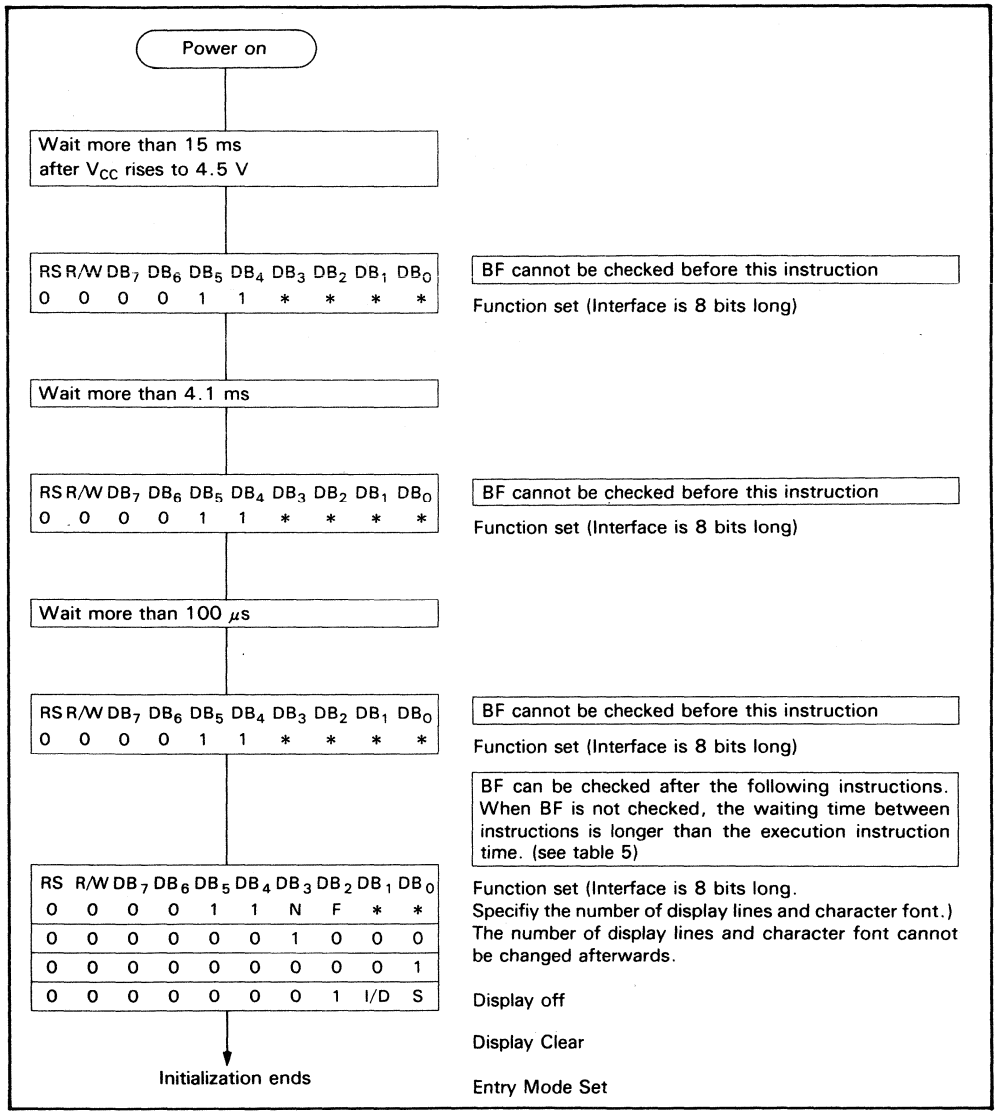


Figure 38. Initialization by Instruction, Eight-Bit Interface

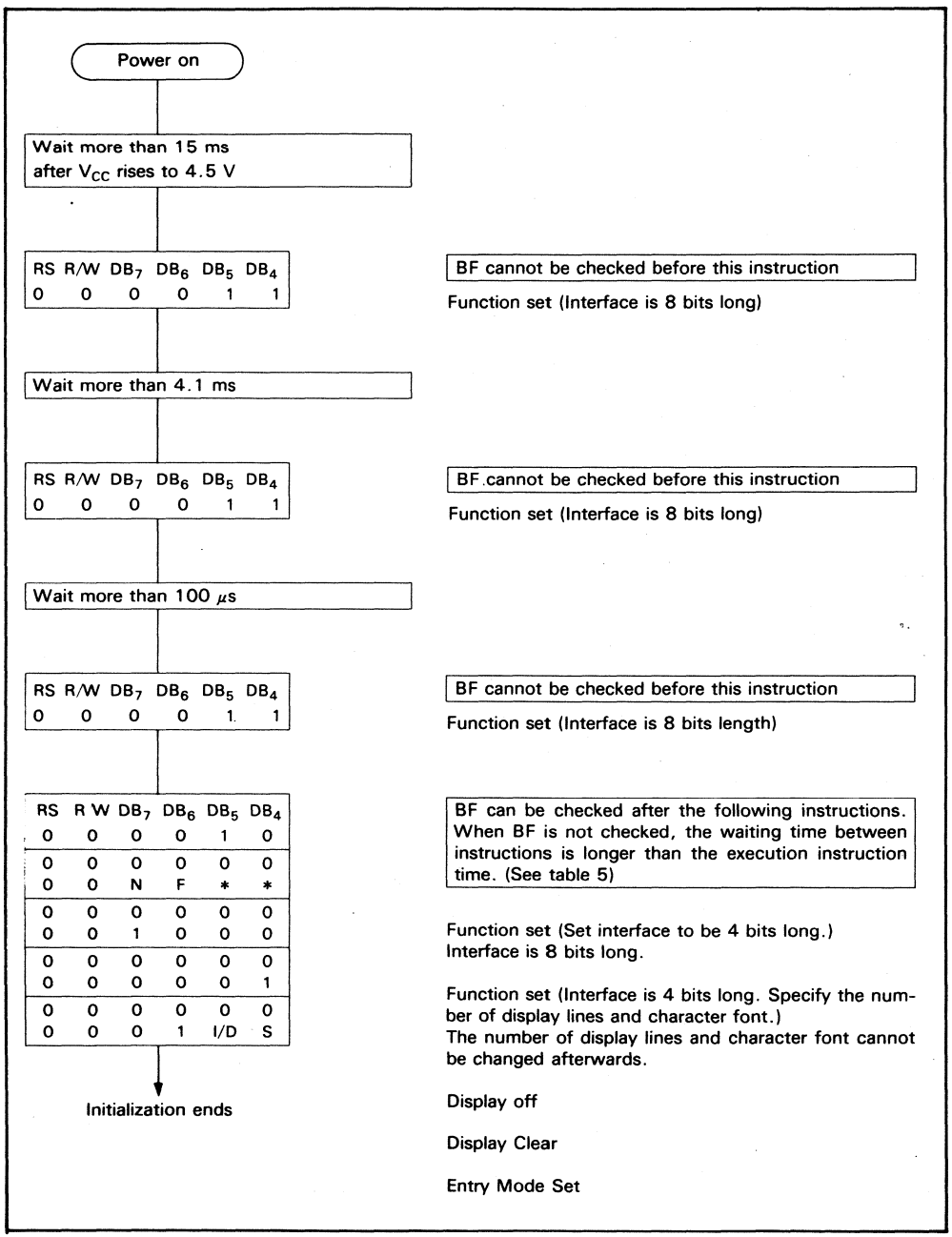


Figure 39. Initialization by Instruction, Four-Bit Interface

LCD-II and LCD-IIA

Table 13 shows the differences between the LCD-II and LCA-IIA.

There are two types of multiplex waveforms for LCD driving; A and B. A type, shown in figure 40, is used for alternation in 1 frame, and B type, shown in figure 41, for alternation in 2 frames. B type has better display quality in high multiplex drive.

Table 13. Functions Comparison between LCD-II and LCD-IIA

Item		LCD-II (HD44780)	LCD-IIA (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	Same as LCD-II	
*Character generator ROM (Kinds of characters)		7200 bits 192 characters 5×7 ;160 characters 5×10; 32 characters	12000 bits 240 characters 5×10;240 characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	Same as LCD-II	
LCD driving terminals (Maximum number of display characters/ unit)		16 COM's 40 SEG's (16 characters)	Same as LCD-II	
Character font (with a cursor)		5×8 dots 5×11 dots	Same as LCD-II	
Multiplexing duty ratio		1/8, 1/11, 1/16		
*LCD driving voltage	1/4 bias	3.0 to 11 (v)	3.0 to V_{CC} (V)	V_{CC} to V_5 (V)
	1/5 bias	4.6 to 11 (v)	3.0 to V_{CC} (v)	
*LCD driving waveform		A waveform	B waveform	See figures 40,41
*Bus timing		1, 1.5 MHz	2 MHz	
Instruction codes		11 instructions	Same as LCD-II	
Power-on reset circuit		Yes	Same as LCD-II	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	Same as LCD-II	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A	Same as LCD-II	
Pin arrangement		Refer to p.1	Same as LCD-II	

Note: * indicates the modified items on LCD-IIA.

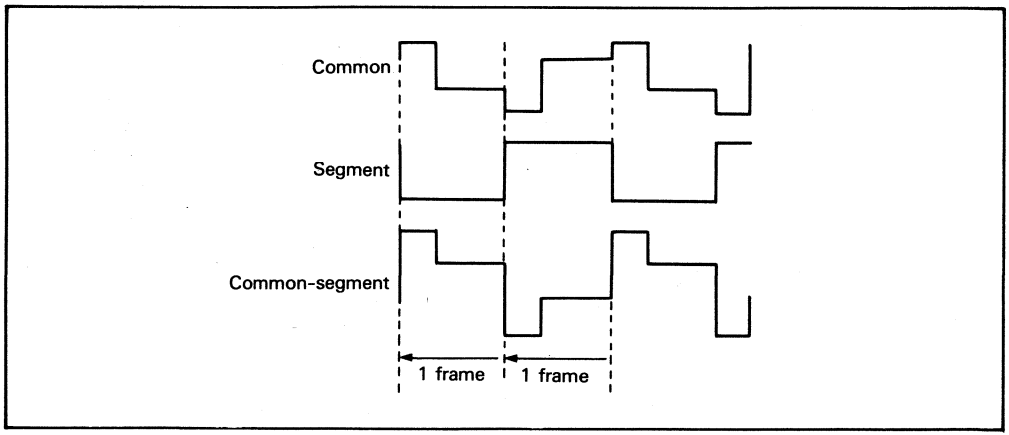


Figure 40. A-Type Waveforms (1/3 Duty, 1/3 Bias)

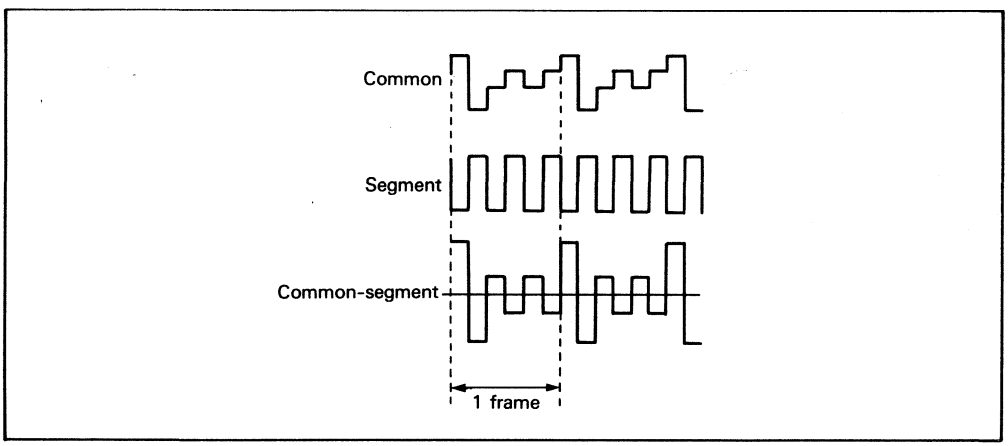


Figure 41. B-Type Waveforms (1/3 Duty, 1/3 Bias)

1. Character Pattern Development Procedure

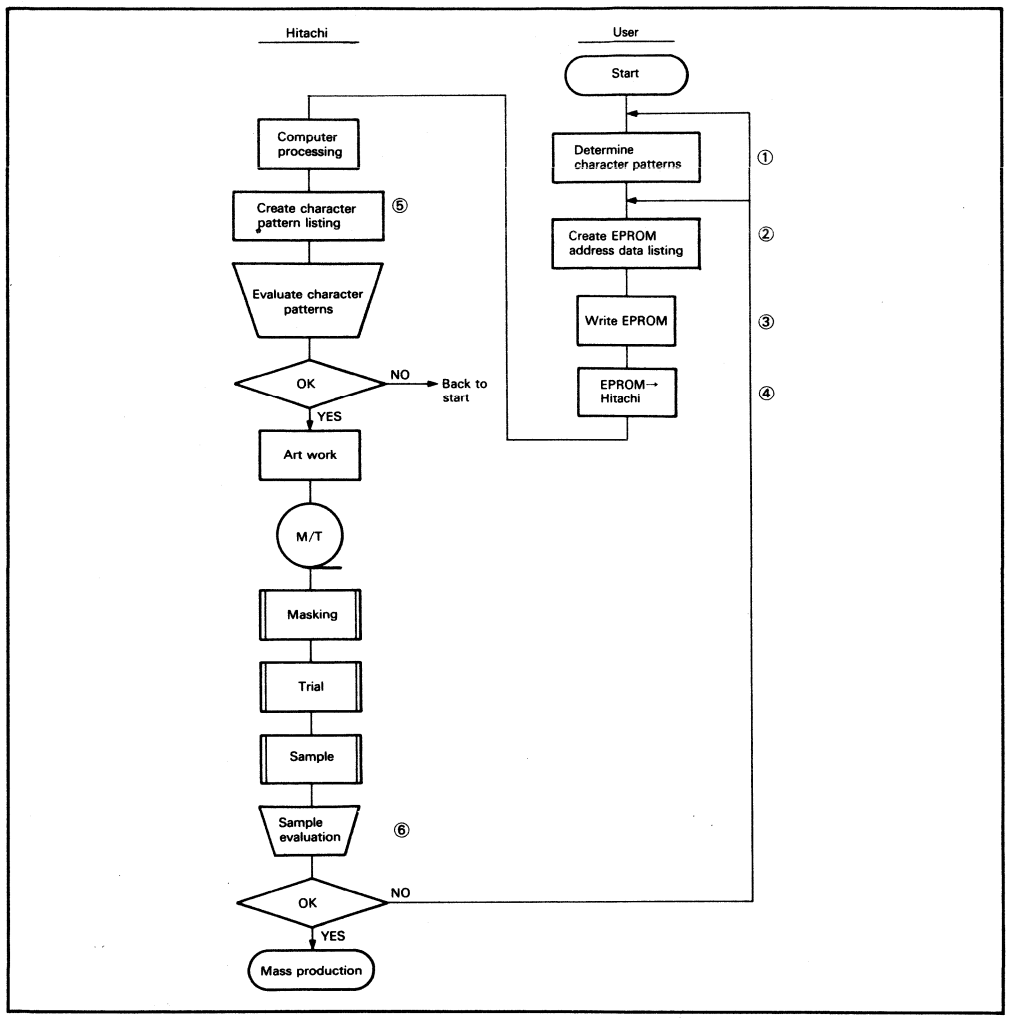


Figure 42. Character pattern development procedure

The numbers in the above figure correspond to the following operations:

(1) Determine the correspondence between character codes and character patterns.
(2) Create a listing indicating the correspondence between EPROM addresses and data.
(3) Program character patterns in the EPROM.
(4) Send the EPROM to Hitachi.
(5) Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.
(6) If there is no problem in the character pattern listing, Hitachi creates LSI for trial and sends samples to the user.The user evaluates the samples. When it is confirmed that character patterns are correctly written, mass production of LSI is started.

- Character pattern program method

The relationship between the EPROM address and character pattern is as follows.

In order to evaluate ROM patterns, we recommend to use our LCD controller HD61830. We also supply LCD control board (CB1026R).

EPROM ADDRESS												DATA							
												(LSB)							
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
								0	0	0	0	0	0	0	0	0			
								0	0	0	1	0	0	0	0	0			
								0	0	1	0	0	■	■	0	■			
								0	0	1	1	■	0	0	■	■			
								0	1	0	0	■	0	0	0	■			
1	1	1	1	0	0	0	1	0	1	0	1	■	0	0	0	■			
								0	1	1	0	0	■	■	■	■			
								0	1	1	1	0	0	0	0	■			
								1	0	0	0	0	0	0	0	■			
								1	0	0	1	0	0	0	0	■			
								1	0	1	0	0	0	0	0	0			
								1	0	1	1								
								1	1	0	0								
								1	1	0	1								
								1	1	1	0								
								1	1	1	1								

Character code — Line code

Note:
1. EPROM DATA O_5-O_7 are invalid
2. DATA "0" must be programed at 11 th line (cursor position).
3. DATA at 12-16 th line are invalid
4. DATA at O_0 locate at the left side of screen. (The relation between the bit No, and position is reversed, comparing with HD44780).

- **Handling unused character patterns**

(1) EPROM data outside the character pattern area
It is ignored by the character generator ROM for display operation so that it can be 0 or 1.
(2) EPROM data in CG RAM area
It is ignored by the character generator ROM for display operation so that it can be 0 or 1.
(3) EPROM data used when the user does not use any LCD-II character pattern
It is handled in one of the two ways explained below. Select one of two ways according to the user application.

1) When unused character patterns are not programed
If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1 when the EPROM is erased.)
2) Program 0 for unused character patterns
Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (It is equivalent to space.)

Absolute Maximum Ratings

Item	Pating	Reting	Unit
Power Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	Tstg	-55 to +125	°C

Notes: 1. If LSI's are used above the absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to V1 to V5. The relation: $V_{CC} \geqq V1 \geqq V3 \geqq V4 \geqq V5 \geqq GND$ must be maintained.
(high to low)

Electrical Characteristics

DC Electrical Characteristics (Vcc = 5V±10% Ta = -20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.0	–	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	–	–	0.8	V		(2)
Input High Voltage (2)	V_{IH2}	V_{CC} - 1.0	–	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	–	–	1.0	V		(12)
Output High Voltage (1)(TTL)	V_{OH1}	2.4	–	–	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1)(TTL)	V_{OL1}	–	–	0.4	V	I_{OL} = 1.6 mA	(3)
Output High Voltage (2)(CMOS)	V_{OH2}	0.9V_{CC}	–	–	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2)(CMOS)	V_{OL2}	–	–	0.1V_{CC}	V	I_{OL} = 0.04 mA	(4)
Driver On Resistance (COM)	R_{COM}	–	–	20	kΩ	±Id = 0.05 mA to each COM Pin	(10)
Driver On Resistance (SEG)	R_{SEG}	–	–	30	kΩ	±Id = 0.05 mA to each SEG Pin	(10)
Input Leakage Current	I_{IL}	-1	–	1	μA	V_{in} = 0 to V_{CC}	(5)
Pull up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	–	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	–	0.35	0.6	mA	Rf oscillation, External clock operation V_{CC} = 5 V, f_{OSC} = fcp = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	–	–	0.2	μs		(7)
External Clock Fall Time	t_{fcp}	–	–	0.2	μs		(7)
Internal Clock Operation (Rf Oscillation)							
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 82 kΩ±2%	(8)
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	3.0	–	V_{CC}	V	V_{CC} - V_5 1/5 bias	(13)
	V_{LCD2}	3.0	–	V_{CC}	V	1/4 bias	(13)

Notes:
1. Figure 42 shows the I/O pin configurations except for liquid crystal display output.
2. Input pins and I/O pins. Excludes OSC_1 pin.
3. I/O pins.
4. Output pins.
5. Current flowing through pull-up MOS's and output drive MOS's is excluded.
6. Input/output current is excluded. When input is at an intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.
7. External clock operation as shown in figure43.
8. Internal oscillator operation using oscillation resistor Rf (figure 44).
9. Internal oscillator operation using a ceramic filter (figure 45)
10. R_{COM} applies to the resistance between power supply pin (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).
    R_{SEG} applies to the resistance between power supply pin (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{40}).

11. Relation between operation frequency and current consumption is shown in figure 46. (V_{CC} = 5 V)
12. Applied to OSC_1 pin.
13. When each COM and SEG output voltage is within ±0.15 V of LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

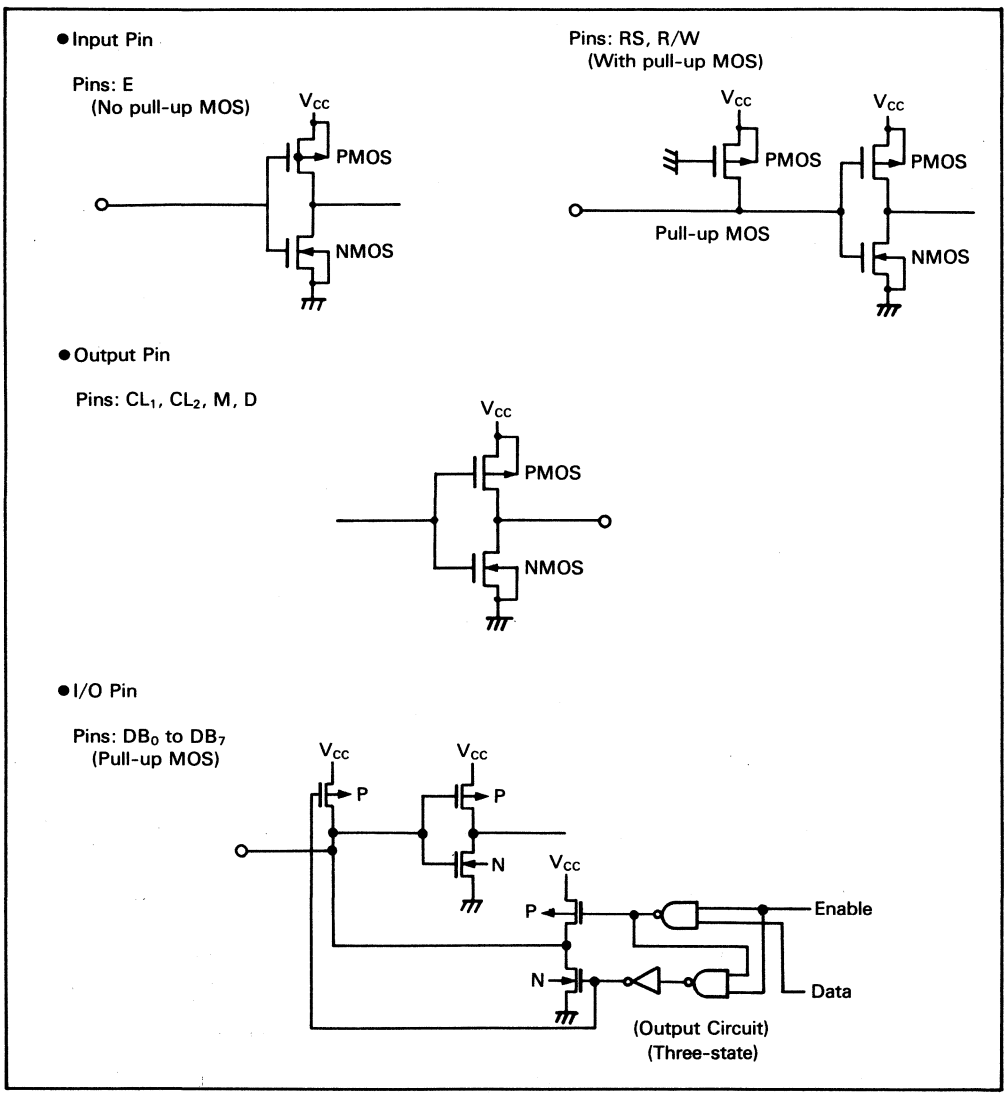


Figure 43. Pin Configuration

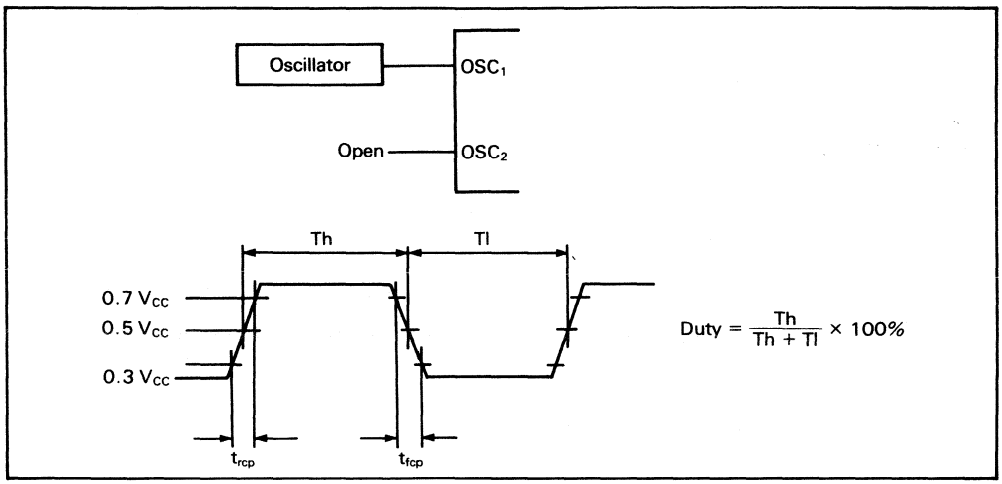
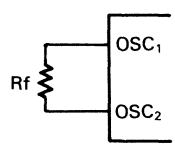
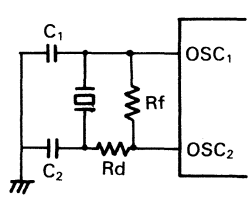


Figure 44. External Clock



Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length to these pin should be minimized.

Figure 45. Internal Oscillator, Resistor



Ceramic filter: CSB250A (Murata)
Rf: 1 MΩ ±10%
C_1: 680 pF ±10%
C_2: 680 pF ±10%
Rd: 3.3 kΩ ±5%

Note: This circuit is a standard one and we do not insure the oscillation frequency characteristics. Study the actual circuit ratings in using this circuit.

Figure 46. Internal Oscillator, Ceramic Filter

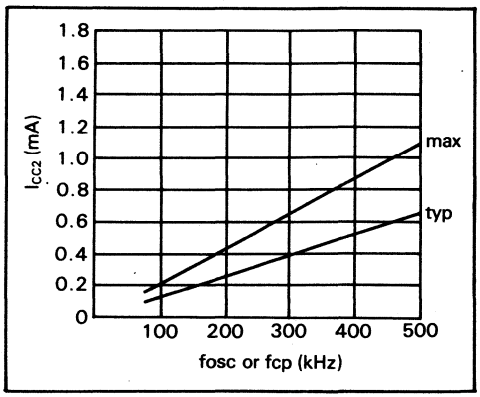
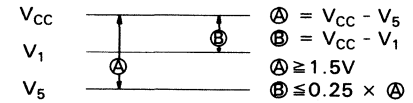


Figure 47. Frequency vs Current



Ⓐ = V_{CC} - V_5
Ⓑ = V_{CC} - V_1
Ⓐ ≧ 1.5V
Ⓑ ≦ 0.25 × Ⓐ

Note: The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level (figure 47). The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

Figure 48. V_1, V_5 Voltages

Bus Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Write Operation (Writing Data from MPU to HD66780)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 51
Enable Pulse Width (High level)	PW_{EH}	220	–	ns	Fig. 51
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 51
Address Set-up Time (RS, R/W−E)	t_{AS}	50	–	ns	Fig. 51
Address Hold Time	t_{AH}	10	–	ns	Fig. 51
Data Set-up Time	t_{DSW}	60	–	ns	Fig. 51
Data Hold Time	t_H	10	–	ns	Fig. 51

Read Operation (Reading Data from HD66780 to MPU)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 52
Enable Pulse Width (High level)	PW_{EH}	220	–	ns	Fig. 52
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 52
Address Set-up Time (RS, R/W −E)	t_{AS}	50	–	ns	Fig. 52
Address Hold Time	t_{AH}	10	–	ns	Fig. 52
Data Delay Time	t_{DDR}	–	150	ns	Fig. 52
Data Hold Time	t_{DHR}	20	100	ns	Fig. 52

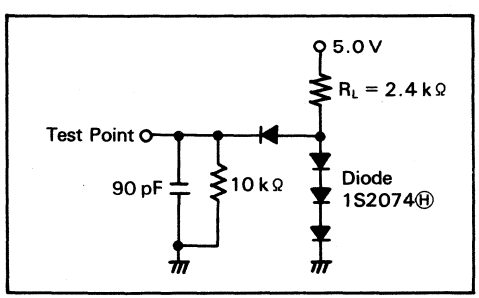


Figure 49. Load Circuit (DB_0−DB_7)

Interface Signal with HD44100H or HD66100F Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Item		Symbol	Min	Max	Unit	Test Condition
Clock Pulse Width	(High level)	t_{CWH}	800	–	ns	Fig. 53
Clock Pulse Width	(Low level)	t_{CWL}	800	–	ns	Fig. 53
Clock Set-up Time		t_{CSU}	500	–	ns	Fig. 53
Data Set-up Time		t_{SU}	300	–	ns	Fig. 53
Data Hold Time		t_{DH}	300	–	ns	Fig. 53
M Delay Time		t_{DM}	-1000	1000	ns	Fig. 53
Clock Rise/Fall Time		t_{ct}	–	100	ns	Fig. 53

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Max	Unit	Test Condition
Power Supply Rise Time	t_{rCC}	0.1	10	ms	–
Power Supply Off Time	t_{OFF}	1	–	ms	–

Note: The internal reset circuit will not operate normally unless the preceding conditions are met. In that case, initialize by instruction. (Refer to Initializing by Instruction)

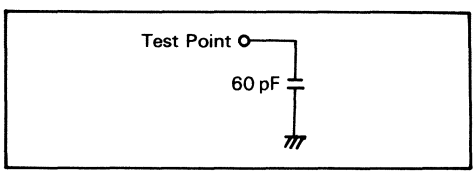


Figure 50. Interface Signal Load Circuit

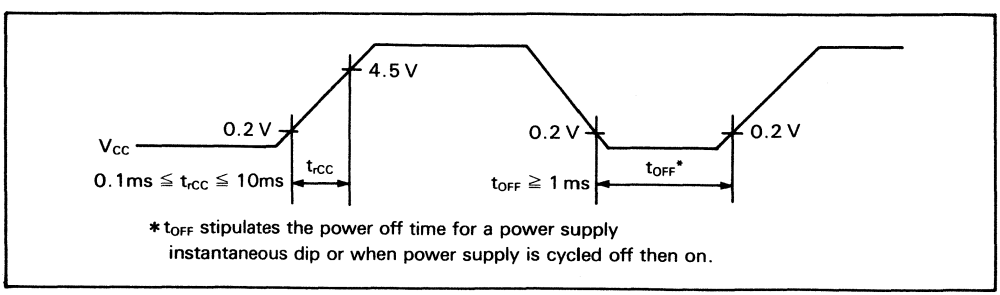


Figure 51. Power Supply Timing

Timing Characteristics

Write Operation

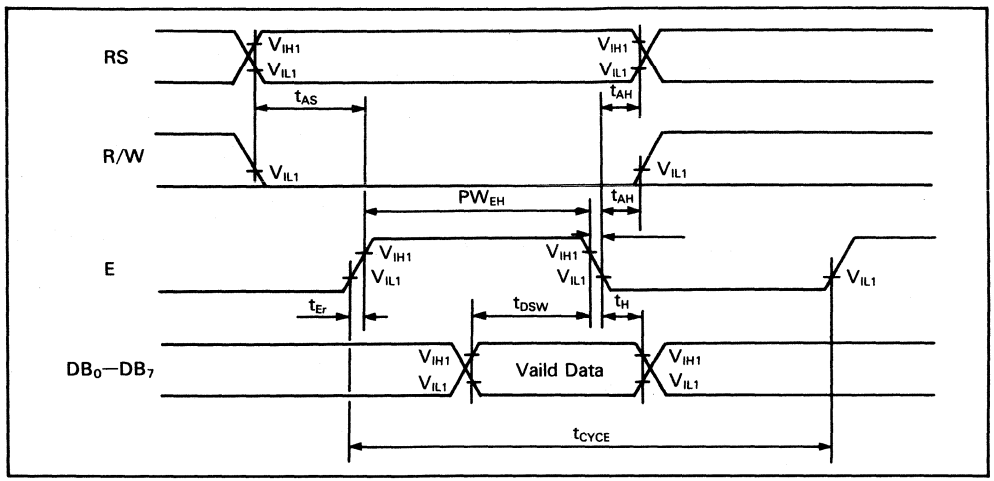


Figure 52. Bus Write Operation Sequence (Writing Data from MPU to HD66780)

Read Operation

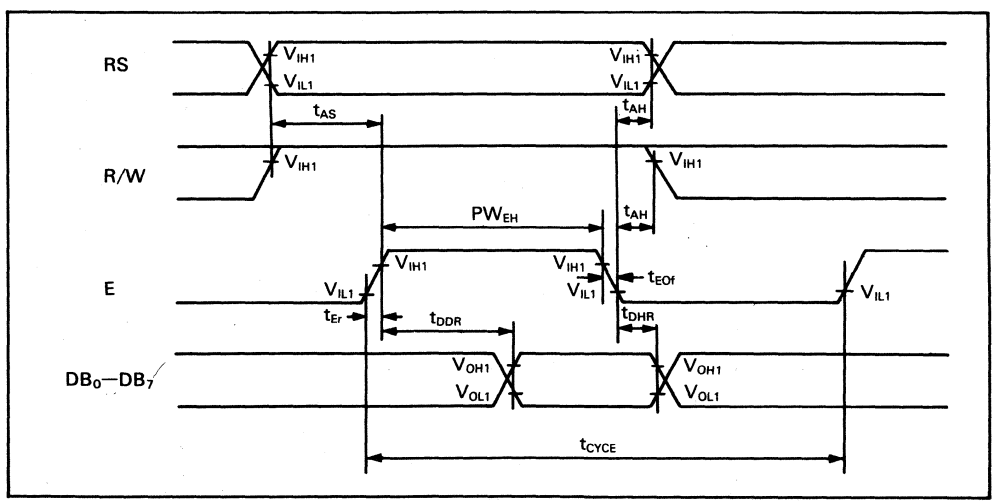


Figure 53. Bus Read Operation Sequence (Reading Data from HD66780 to MPU)

Interface signal with driver LSI HD44100H or HD66100F

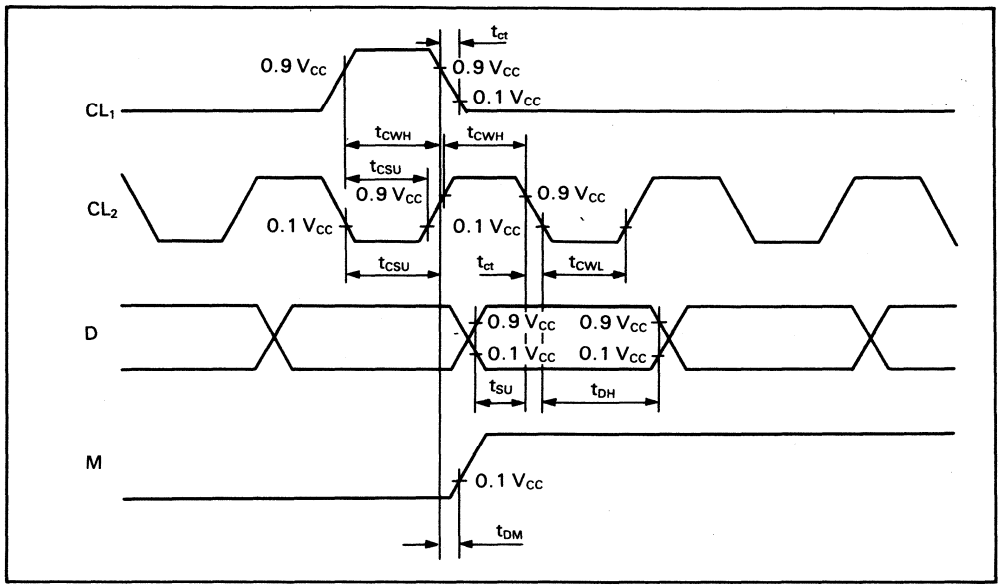


Figure 54. Sending Data to Driver LSI HD44100H or HD66100F

HD44102CH

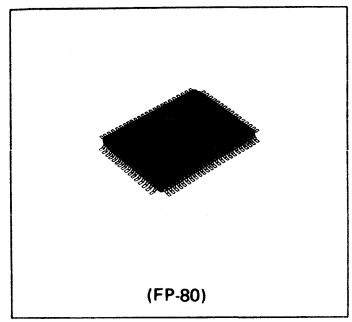
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

The HD44102CH is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit microcomputer in the internal display RAM and generating dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display

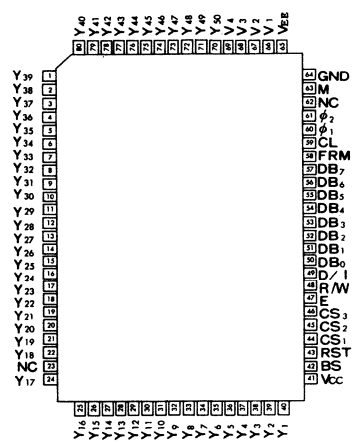
The HD44102CH is produced in the CMOS process. Therefore, the combination with a CMOS microcomputer can accomplish a portable battery drive equipment utilizing the liquid crystal display's lower power dissipation.

The combination of HD44102CH with the row (common) driver HD44103CH facilitates dot matrix liquid crystal graphic display system configuration.



(FP-80)

■PIN ARRANGEMENT

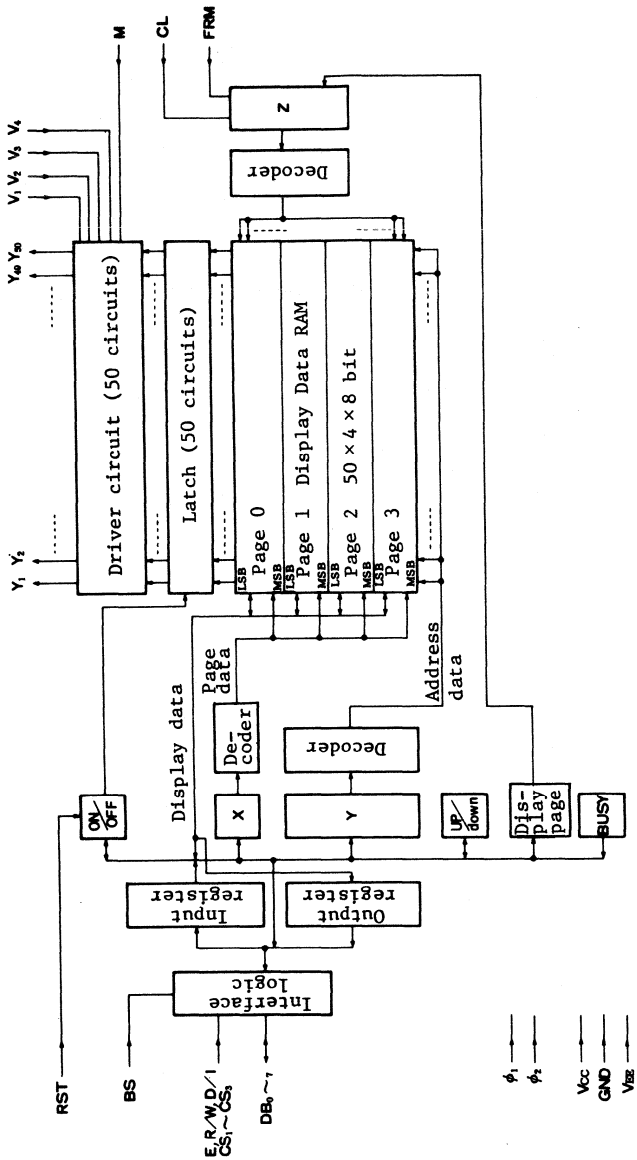


(TOP VIEW)

■ FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- Interfaceable to 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  RAM bit data "1" ..... ON
  RAM bit data "0" ..... OFF
- Display RAM capacity ..... 50 × 8 × 4 (1600 bits)
- Internal liquid crystal display driver circuit (segment output) .....
  50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  Selectable duty factors 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  Display Data Read/Write, Display ON/OFF, Set Address, Set Display Start Page, Set UP/DOWN, Read Status
- Low power dissipation
- Power supplies ..... V_{CC} 5V±10%, V_{EE} 0∿-5V
- CMOS process
- 80-pin flat plastic package

■ BLOCK DIAGRAM



■TABLE OF PIN ASSIGNMENT

No.	Power supply, Clock	Input	Output	No.	Power supply Clock	Input	Output
1			Y39	41	V_{CC}		
2			Y38	42		BS	
3			Y37	43		RST	
4			Y36	44		CS1	
5			Y35	45		CS2	
6			Y34	46		CS3	
7			Y33	47		E	
8			Y32	48		R/W	
9			Y31	49		D/I	
10			Y30	50		DB_0	DB_0
11			Y29	51		DB_1	DB_1
12			Y28	52		DB_2	DB_2
13			Y27	53		DB_3	DB_3
14			Y26	54		DB_4	DB_4
15			Y25	55		DB_5	DB_5
16			Y24	56		DB_6	DB_6
17			Y23	57		DB_7	DB_7
18			Y22	58		FRM	
19			Y21	59		CL	
20			Y20	60	ϕ_1		
21			Y19	61	ϕ_2		
22			Y18	62		N. C.	
23		N. C.		63		M	
24			Y17	64	GND		
25			Y16	65	V_{EE}		
26			Y15	66	V_1		
27			Y14	67	V_2		
28			Y13	68	V_3		
29			Y12	69	V_4		
30			Y11	70			Y50
31			Y10	71			Y49
32			Y9	72			Y48
33			Y8	73			Y47
34			Y7	74			Y46
35			Y6	75			Y45
36			Y5	76			Y44
37			Y4	77			Y43
38			Y3	78			Y42
39			Y2	79			Y41
40			Y1	80			Y40

(Note) N.C.: Nonconnection pin

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC}-13.5 ∿ V_{CC}+0.3	V	
Input voltage (1)	V_{T1}	-0.3 ∿ V_{CC}+0.3	V	1, 2
Input voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC}+0.3	V	3
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: Referred to GND=0.

Note 2: Applied to input terminals (except V1, V2, V3 and V4), and I/O common terminals.

Note 3: Applied to terminals V1, V2, V3 and V4.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, GND=0V, V_{EE}=0∿-5.5V, Ta=-20∿+75°C) (Note 4)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "High" voltage(CMOS)	V_{IHC}		0.7×V_{CC}	-	V_{CC}	V	5
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3×V_{CC}	V	5
Input "High" voltage (TTL)	V_{IHT}		2.0	-	V_{CC}	V	6
Input "Low" voltage (TTL)	V_{ILT}		0	-	+0.8	V	6
Output "High" voltage	V_{OH}	I_{OH}=-250μA	+3.5	-	-	V	7
Output "Low" voltage	V_{OL}	I_{OL}=+1.6mA	-	-	+0.4	V	7
Vi-Xj ON resistance	R_{ON}	V_{EE}=-5V±10%, Load current 100μA	-	-	7.5	kΩ	
Input leakage current (1)	I_{IL1}	V_{IN}=V_{CC}∿GND	-1	-	1	μA	8
Input leakage current (2)	I_{IL2}	V_{IN}=V_{CC}∿V_{EE}	-2	-	2	μA	9
Operating frequency	f_{CLK}	φ1,φ2 frequency	25	-	280	kHz	10
Dissipation current (1)	I_{CC1}	f_{clk}=200kHz frame=65Hz during display	-	-	100	μA	11
Dissipation current (2)	I_{CC2}	Access cycle 1MHz at access	-	-	500	μA	12

Note 4: Specified within this range unless otherwise noted.

Note 5: Applied to M, FRM, CL, BS, RST, ϕ1, ϕ2.

Note 6: Applied to CS1 to CS3, E, D/I, R/W and DB0 to DB7.

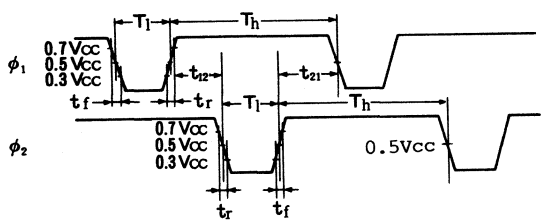
Note 7: Applied to DB0 to DB7.

Note 8: Applied to input terminals, M, FRM, CL, BS, RST, ϕ1, ϕ2, CS1 to $\overline{CS3}$, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.

Note 9: Applied to V1, V2, V3 and V4.

Note 10: ϕ1 and ϕ2 AC characteristics.

	Symbol	Min.	Typ	Max.	Unit
Duty	Duty	20	25	30	%
Fall time	t_f	-	-	100	ns
Rise time	t_r	-	-	100	ns
Phase difference time	t_{12}	0.8	-	-	µs
Phase difference time	t_{21}	0.8	-	-	µs
$T_l + T_h$		-	-	40	µs



$$f_{CLK} = \frac{1}{T_l + T_h}$$

$$D_{uty} = \frac{T_l}{T_l + T_h} \times 100\ (\%)$$

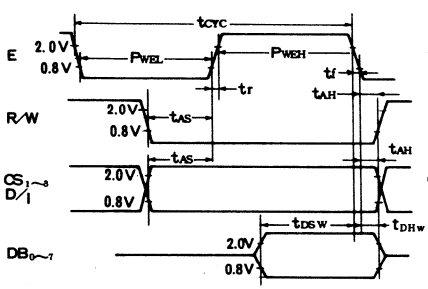
Note 11: Measured by V_{CC} terminal at no output load, at 1/32 duty, and frame frequency of 65Hz, in checker pattern display. Access from the CPU is stopping.

Note 12: Measured by V_{CC} terminal at no output load, 1/32 duty and frame frequency of 65Hz.

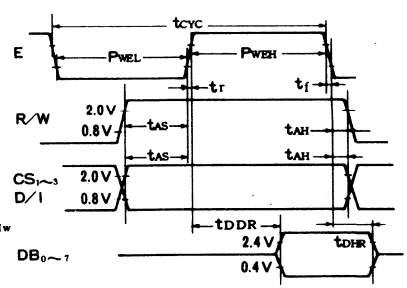
●INTERFACE AC CHARACTERISTICS

Item	Symbol	Min.	Typ	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	13, 14
E high level width	PWEH	450	-	-	ns	13, 14
E low level width	PWEL	450	-	-	ns	13, 14
E rise time	t_r	-	-	25	ns	13, 14
E fall time	t_f	-	-	25	ns	13, 14
Address setup time	t_{AS}	140	-	-	ns	13, 14
Address hold time	t_{AH}	10	-	-	ns	13, 14
Data setup time	t_{DSW}	200	-	-	ns	13
Data delay time	t_{DDR}	-	-	320	ns	14, 15
Data hold time at write	t_{DHW}	10	-	-	ns	13
Data hold time at read	t_{DHR}	20	-	-	ns	14

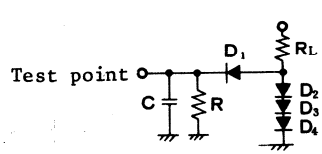
Note 13: At CPU write



Note 14: At CPU read



Note 15: DB0 to DB7 load circuits



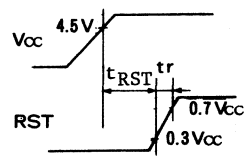
R_L = 2.4kΩ
R = 11kΩ
C = 130pF (including jig capacity)
Diodes D1 to D4 are all 1S2074 Ⓗ

Note 16: Display OFF at initial power up.

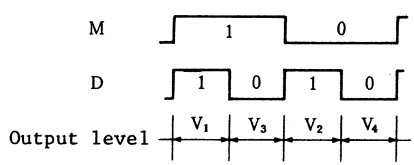
The HD44102CH can be placed in the display OFF state by setting terminal RST to "LOW" at initial power up.

No instruction other than the Read Status cannot be accepted while the RST is in the "Low" level.

	Symbol	Min.	Typ	Max.	Unit
Reset time	t_{RST}	1.0	-	-	μs
Rise time	t_r	-	-	200	ns



■ TERMINAL FUNCTIONS DESCRIPTION

Signal name	Number of terminals	I/O	Function
Y1∿Y50	50	O	Liquid crystal display drive output. Relationship among output level, M and display data (D): 
CS1∿CS3	3	I	Chip select CS1 / CS2 / CS3 / State L / L / L / Non-selected L / L / H / Non-selected L / H / L / Non-selected L / H / H / Selected read/write enable H / L / L / Selected write enable only H / L / H / Selected write enable only H / H / L / Selected write enable only H / H / H / Selected read/write enable
E	1	I	Enable At write (R/W=L): Data of DB0 to DB7 is latched at the fall of E. At read (R/W=H): Data appears at DB0 to DB7 while E is in "High" level.

<table>
<tr><th>Signal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>R/W</td><td>1</td><td>I</td><td>Read/Write
R/W=H: Data appears at DB0 to DB7 and can be read by the CPU when E=H and CS2, CS3="H".
R/W=L: DB0 to DB7 can accept input when CS2,CS3=H or CS1=H.</td></tr>
<tr><td>D/I</td><td>1</td><td>I</td><td>Data/Instruction
D/I=H: Indicates that the data of DB0 to DB7 is display data.
D/I=L: Indicates that the data of DB0 to DB7 is display control data.</td></tr>
<tr><td>DB0∿DB7</td><td>8</td><td>I/O</td><td>Data bus, Three-state I/O common terminal
<table>
<tr><th>E</th><th>R/W</th><th>CS1</th><th>CS2</th><th>CS3</th><th>State of DB0 to DB7</th></tr>
<tr><td>H</td><td>H</td><td>*</td><td>H</td><td>H</td><td>Output state</td></tr>
<tr><td>*</td><td>L</td><td>H</td><td>*</td><td>*</td><td>Input state,</td></tr>
<tr><td>*</td><td>L</td><td>*</td><td>H</td><td>H</td><td>High impedance</td></tr>
<tr><td colspan="5">Others</td><td>High impedance</td></tr>
</table></td></tr>
<tr><td>M</td><td>1</td><td>I</td><td>Signal to convert liquid crystal display drive output to AC</td></tr>
<tr><td>CL</td><td>1</td><td>I</td><td>Display synchronous signal
At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.</td></tr>
<tr><td>FRM</td><td>1</td><td>I</td><td>Display synchronous signal (frame signal)
This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.</td></tr>
<tr><td>ϕ1, ϕ2</td><td>2</td><td>I</td><td>2-phase clock signal for internal operation
The ϕ1 and ϕ2 clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.</td></tr>
<tr><td>RST</td><td>1</td><td>I</td><td>Reset signal
The display disappears and Y address counter is set in the UP counter state by setting the RST signal to "Low" level. After releasing reset, the display OFF state and up mode is held until the state is changed by the instruction.</td></tr>
<tr><td>BS</td><td>1</td><td>I</td><td>Bus select signal
BS=L: DB0 to DB7 operate in 8-bit length.
BS=H: DB4 to DB7 are valid in 4-bit length only. 8-bit data is accessed twice in the high and low order.</td></tr>
</table>

Signal name	Number of terminals	I/O	Function
V1,V2, V3,V4	4		Power supply for liquid crystal display drive. V1 and V2: Selection voltage V3 and V4: Non-selection voltage
V_{CC} GND V_{EE}	3		Power supply. V_{CC}-GND: Power supply for internal logic V_{CC}-V_{EE}: Power supply for liquid crystal display drive circuit logic

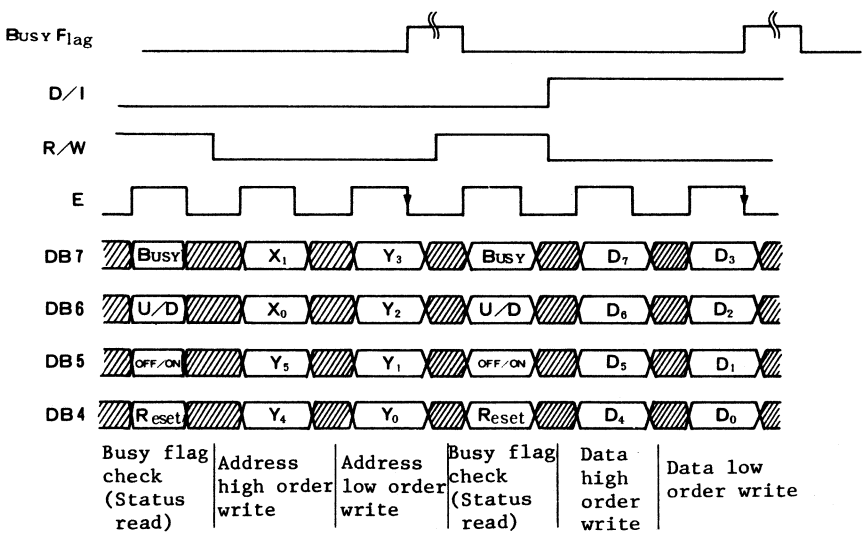
■FUNCTION OF EACH BLOCK

●Interface Logic

The HD44102CH can use the data bus in 4-bit or 8-bit word length to enable the interface to a 4-bit or 8-bit CPU.

(1) 4-bit mode (BS=H)

8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high. The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) is transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).



(Note) Execute the instructions other than Status Read in 4-bit length each. The busy flag is set at the fall of the second E signal. The Status Read is executed once. After the execution of the Status Read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

(2) 8-bit mode (BS=L)

If the BS signal is low, the 8 data buses (DB0 to DB7) are used for data transfer.

DB7 ... MSB (Most significant bit)

DB0 ... LSB (Least significant bit)

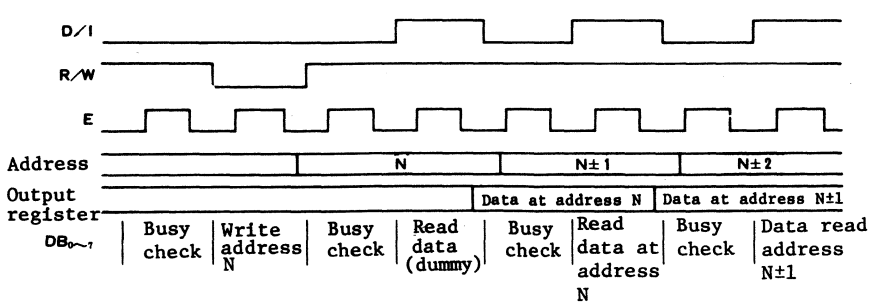
For AC timing, refer to (Note 12) to (Note 15) of "ELECTRICAL CHARACTERISTICS".

● Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of E signal when the CS is in the select state and R/W is write state.

● Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data.



● X,Y Address Counter

The X,Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit UP/DOWN counter. The address is increased or decreased by 1 by the read/write operation of display data. The UP/DOWN mode can be determined by the instruction or RST signal. The Y address register loops the values of 0 to 49 to count. The X address register has no count function.

●Display ON/OFF Flip Flop

This flip flop is set to ON/OFF state by the instruction or RST signal. In the OFF state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the ON state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display ON/OFF.

●UP/DOWN Flip Flop

This flip flop determines the count mode of the Y address counter. In the UP mode, the Y address register is increased by 1. 0 follows 49. In the DOWN mode, the register is decreased by 1. 0 is followed by 49.

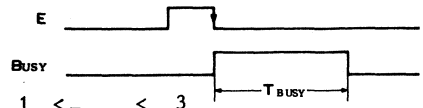
●Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

●Busy Flag

After the instruction other than Status Read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective. The value can be read out on DB7 by the Status Read instruction.

The HD44102CH cannot accept any other instructions than the Status Read in the busy state. Make sure the busy flag is reset before the issue of instruction.



$$\frac{1}{F\phi} \leqq T_{BUSY} \leqq \frac{3}{F\phi}$$

Fϕ is ϕ1, ϕ2 frequency (half of HD44103CH oscillation frequency)

● Z Address Counter

The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputing the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

● Latch

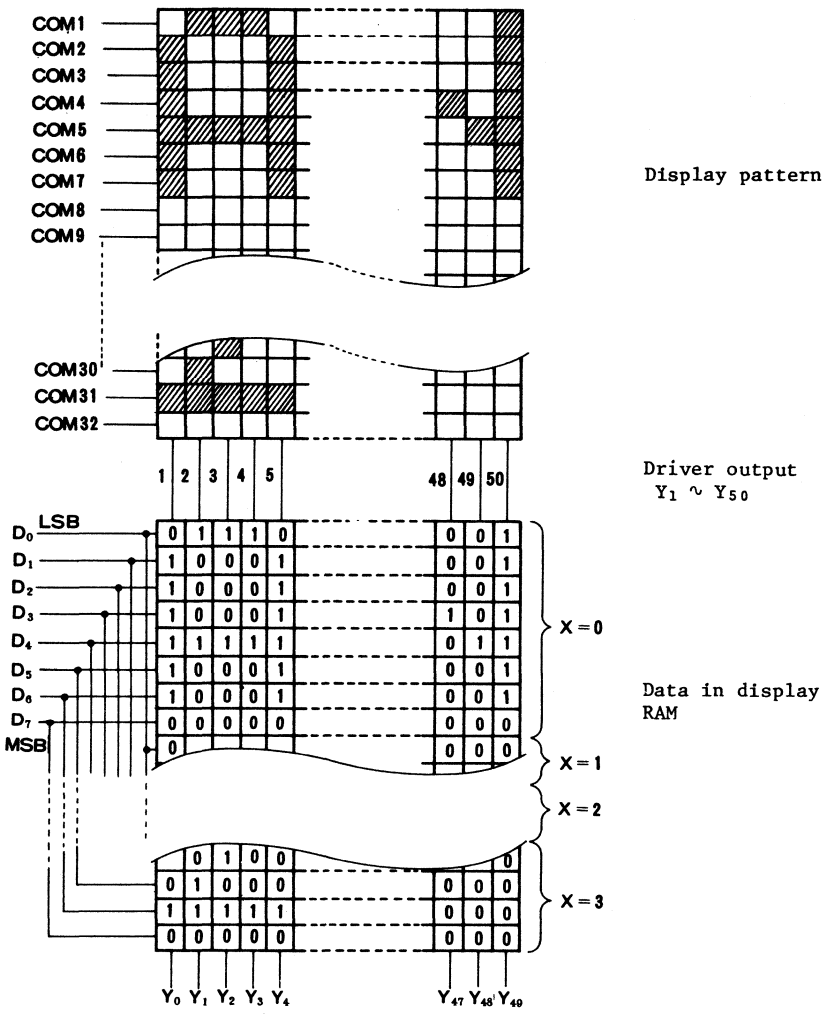
The display data from the display data RAM is latched at the rise of CL signal.

● Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of display data from latchs and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

● Display RAM

Relationship between Data in RAM and Display
(Display start page 0, 1/32 duty)



■DISPLAY CONTROL INSTRUCTIONS

(1) Read/Write Display Data

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
1	1	(Display data)								Read (CPU ← HD44102CH)
0	1	(Display data)								Write (CPU → HD44102CH)

Sends or receives data to or from the address of the display RAM specified in advance. However, the dummy read may be required for reading display data. Refer to the description of the output register in the FUNCTION OF EACH BLOCK.

(2) Display ON/OFF

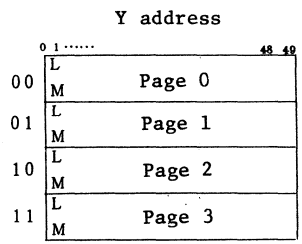
		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	0	1	Display ON
0	0	0	0	1	1	1	0	0	0	Display OFF

Controls the ON/OFF of display. RAM data is not affected.

(3) Set X/Y Address

		MSB			DB				LSB
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0						
0	0	0	1	Binary numbers of 0~49					
0	0	1	0						
0	0	1	1						

X address (page) — Y address (address)



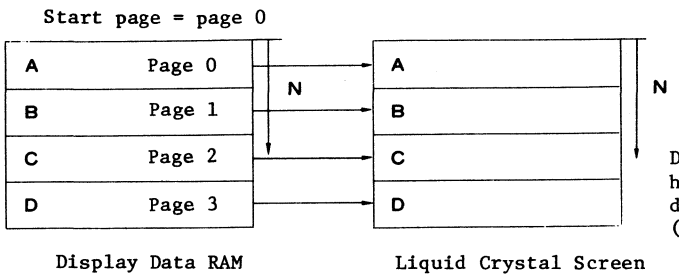
(4) Display Start Page

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	1	1	0	..... Refer to Fig. A.
0	0	0	1	1	1	1	1	1	0	..... Refer to Fig. B.
0	0	1	0	1	1	1	1	1	0	..... Refer to Fig. C.
0	0	1	1	1	1	1	1	1	0	..... Refer to Fig. D.

Display start page

Specifies a RAM page displayed at the top of the screen. Display is as shown in Figs. A, B, C and D respectively. When the display duty is more than 1/32 (For example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

Fig. A



Displayed up to here when display duty is 1/N. (N=8, 12, 16, 24, 32)

Fig. B

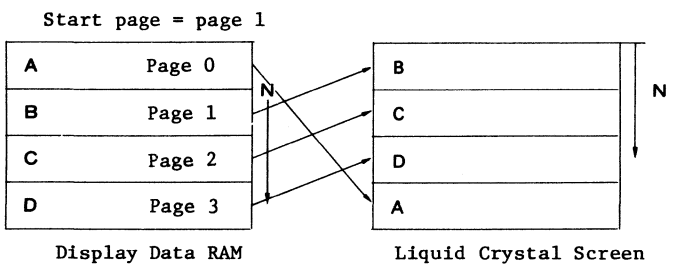


Fig. C

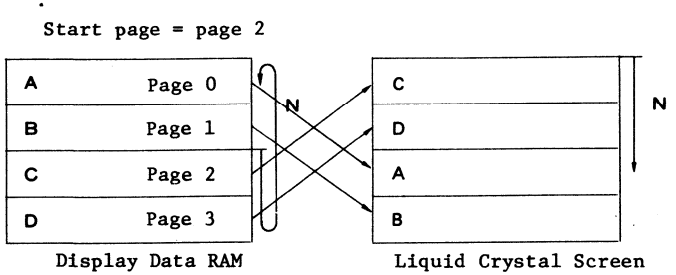
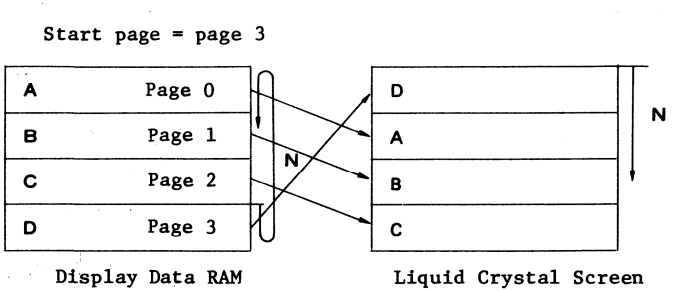


Fig. D



(5) UP/DOWN Set

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	1	1	UP mode
0	0	0	0	1	1	1	0	1	0	DOWN mode

Sets Y address register in the UP/DOWN counter mode.

(6) Status Read

		MSB			DB				LSB
R/W	D/I	7	6	5	4	3	2	1	0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0

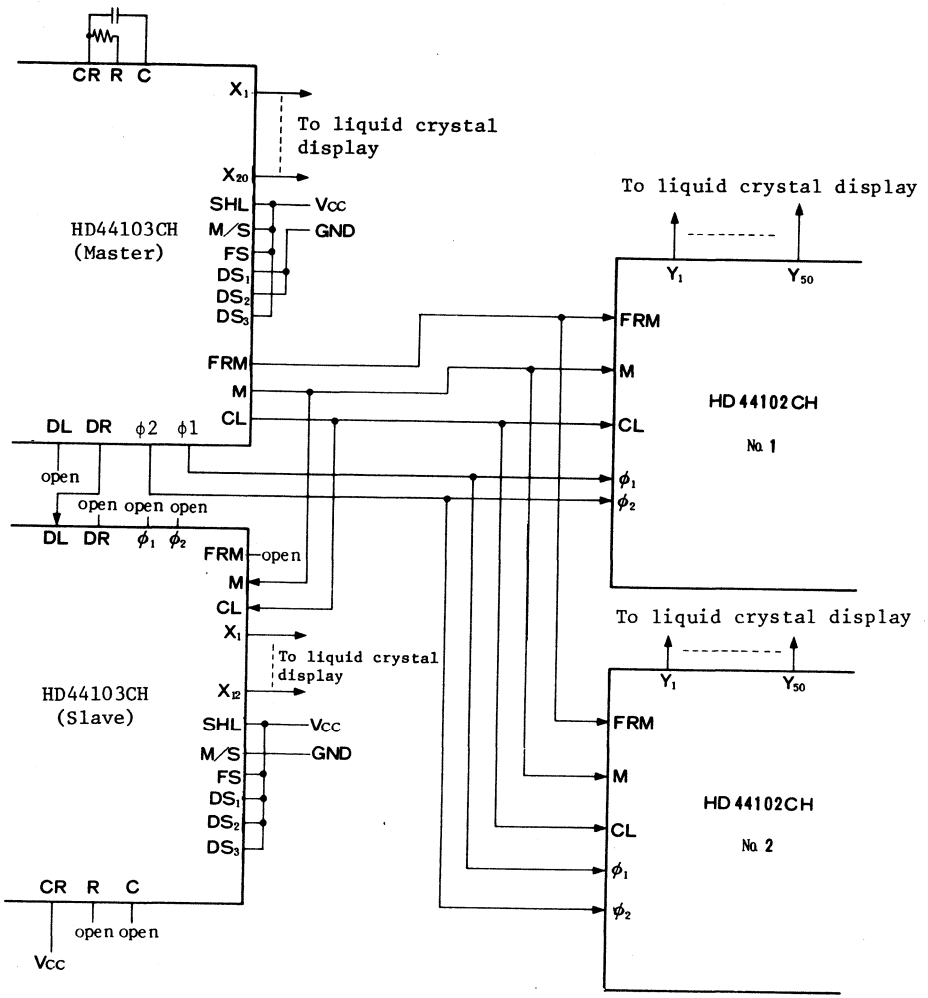
RESET → Goes to "1" when RST is in the reset state (Busy also goes to "1").
Goes to "0" when RST is in the operating state.

OFF/ON → Goes to "1" in the display OFF state.
Goes to "0" on the display ON state.

UP/DOWN → Goes to "1" when address counter is in the UP mode.
Goes to "0" when address counter is in the DOWN mode.

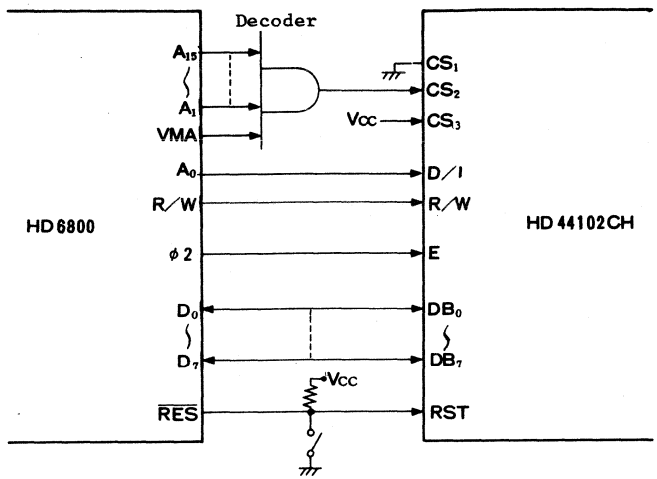
BUSY → Goes to "1" while instructions (1) ∿ (5) are being executed.
During "1", none of instructions (1) ∿ (5) are accepted.

■CONNECTION BETWEEN LCD DRIVERS (EXAMPLE OF 1/32 DUTY)



■INTERFACE TO CPU

(1) Example of connection to HD6800



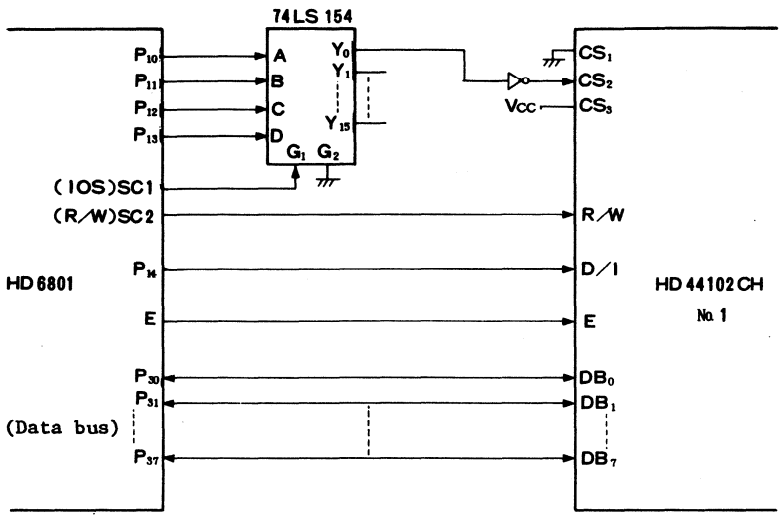
Example of Connection to HD6800 Series

In the decoder given in this example, the addresses of HD44102CH in the address space of HD6800 are:

Read/write of display data : $'FFFF'
Write of display instruction: $'FFFE'
Read of status : $'FFFE'

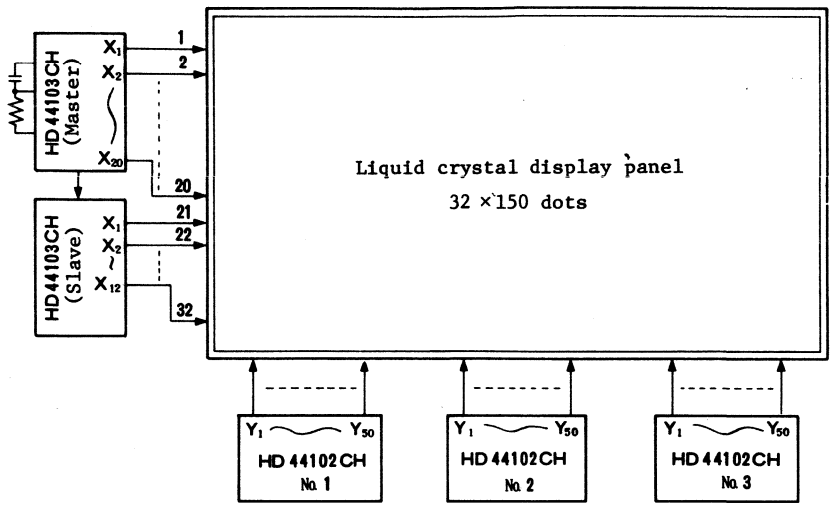
Thus, the HD44102CH can be controlled by reading/writing data at these addresses.

(2) Example of connection to HD6801

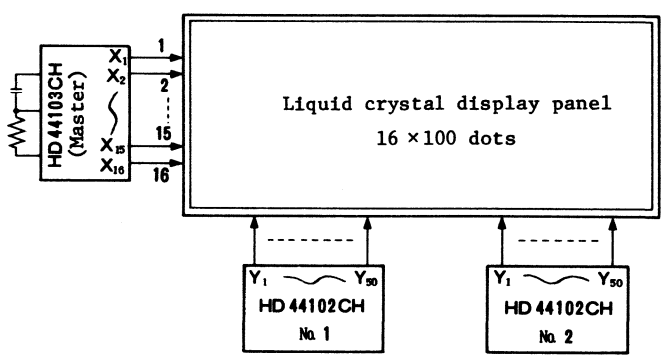


- The HD6801 is set to mode 5. P10 ∿P14 are used as output ports, and P30 ∿P37 are used as data buses.
- The 74LS154 is a 4-to-16 decoder that decodes 4 bits of P10 ∿P13 to select the chips.
- Therefore, the HD44102CH can be controlled by selecting the chips through P10 ∿P13 and specifying the D/I signal through P14 in advance, and later conducting memory Read or Write for external memory space ($0100 to $01FF) of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to each manual.

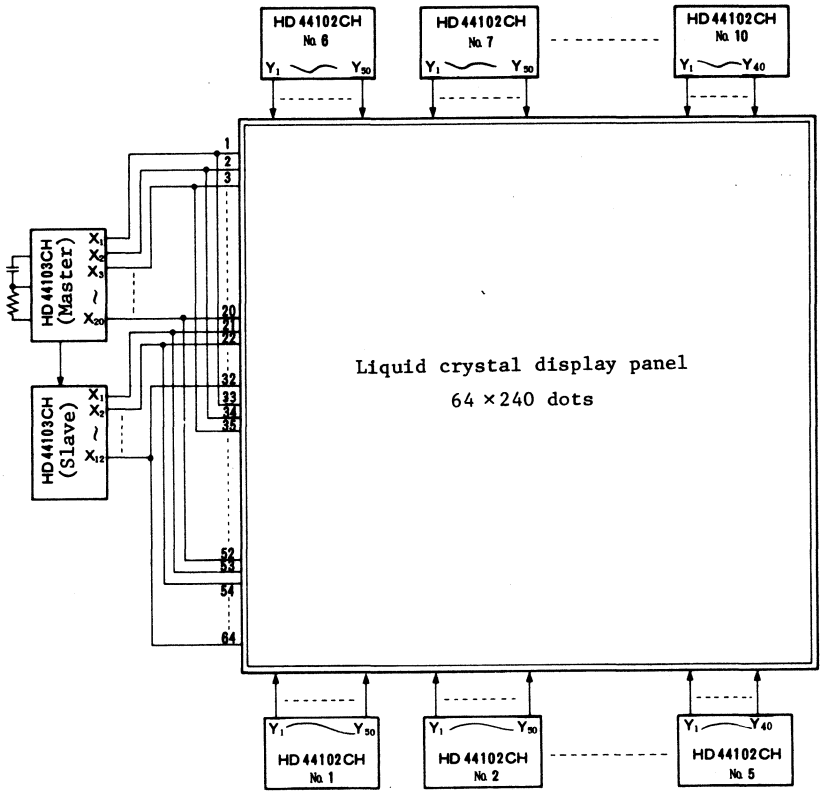
■CONNECTION TO LIQUID CRYSTAL DISPLAY



(a) Example of connection of 1/32 duty, 1-screen display



(b) Example of connection of 1/16 duty, 1-screen display



(c) Example of connection of 1/32 duty, 2-screen display

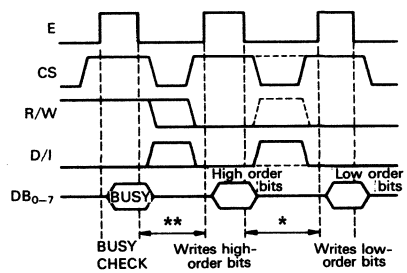
LIMITATIONS ON USING 4-BIT INTERFACE FUNCTION

The HD44102 usually transfers display control data and display data via 8-bit data bus. It also has the 4-bit interface function in which the HD44102 transfers 8-bit data by dividing it into the high-order 4 bits and the low-order 4-bits in order to reduce the number of wires to be connected. You should take an extra care in using the application with the 4-bit interface function since it has the following limitations.

LIMITATIONS

The HD44102 is designed to transfer the high-order 4-bits and the low-order 4-bits of data in that order after busy check. The LSI does not work normally if the signals are in the following state for the time period (indicated with (*) in the figure) from when the high-order 4 bits are written (or read) to when the low-order 4 bits are written (or read); R/W = high and D/I = low while the chip is being selected (CS1 = high and CS2 = CS3 = don't care, or CS1 = low and CS2 = CS3 = high).

EXAMPLE OF WRITING DISPLAY CONTROL INSTRUCTIONS



If the signals are in the limited state mentioned before for the time period indicated with (*) the LSI does not work normally. Please do not make the signals indicated with dotted lines simultaneously. As far as the time period indicated with (**), there is no problem.

The following explains how the malfunction is caused and gives the measures in application.

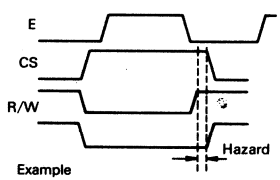
CAUSE

Busy check checks if the LSI is ready to accept the next instruction or display data, by reading the status register of the HD44102. And at the same time, it resets the internal counter counting the order of high-order data and low-order data. This function makes the LSI ready to accept only the high-order data after busy check. Strictly speaking, if R/W = high and D/I = low while the chip is being selected, the internal counter is reset and the LSI gets ready to accept high-order bits. Therefore, the LSI takes low-order data for high-order data if the state mentioned above exist in the interval between transferring high-order data and transferring low-order data.

MEASURES IN APPLICATION

1) When HD44102 Controlled Via Port
   When you control the HD44102 with the port of a single-chip microcomputer, you should take care of the software and observe the limitations strictly.

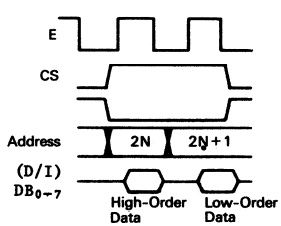
2) When HD44102 Controlled Via Bus
   a) Malfunction Caused by Hazard



Writing High-Order Data

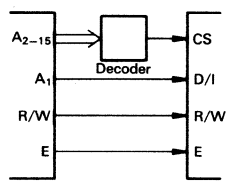
Hazard of input signals may also cause the phenomenon mentioned before. The phase shift at transition of the input signals may cause the malfunction and so the AC characteristics must be fully studied.

b) Using 2-Byte Instruction



Last 2 Machine Cycles of 2-Byte Instruction

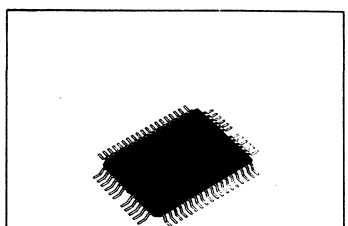
In the application with the HD6303, you can prevent malfunction by using 2-byte instructions such as STD and STX. This is because the high-order and low-order data are accessed in that order without a break in the last machine cycle of the instruction and R/W and D/I do not change in the meantime. However, you cannot use the least significant bit of the address signals as the D/I signal since the address for the second byte is added 1. And design the CS decoder so that the addresses for the HD44102 should be 2N and 2N+1, and that those addresses should be accessed when using 2-byte instructions. Fox example, in the figure shown following figure the address signal A_1 is used as D/I signal and A_2 - A_{15} are used for the CS decoder. Addresses 4N and 4N+1 are for instruction access and addresses 4N+2 and 4N+3 are for display data access.



HD44103CH

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

The HD44103CH is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102CH) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duties ratio: 1/8, 1/12, 1/16, 1/24 and 1/32. 20 driver output lines are provided, and the impedance is low (500Ω max.) to enable a large screen to be driven.

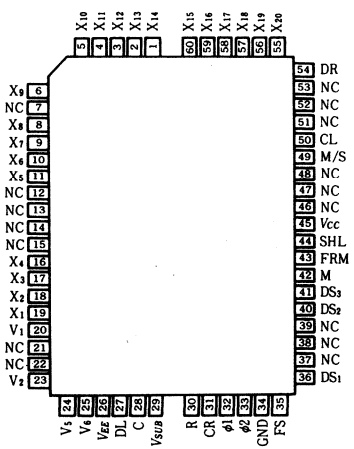


(FP-60)

■ FEATURES

- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit in it.
- Internal oscillator (Oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals.
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies: V_{CC} ...5V±10%, V_{EE} ... 0 to -5.5V
- CMOS process
- 60-pin plastic flat package

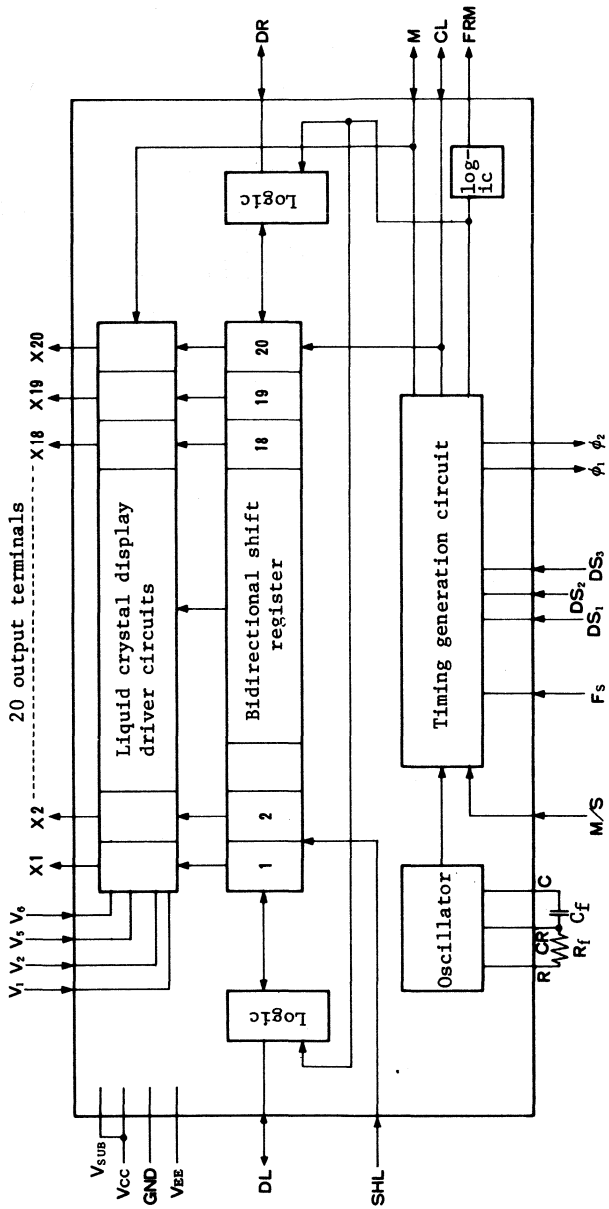
■ PIN ARRANGEMENT



(TOP VIEW)

HITACHI

■BLOCK DIAGRAM



● TERMINAL ARRANGEMENT LIST

No.	Power supply, Clock	Input	Output	No.	Power supply, Clock	Input	Output
1			X 14	31	CR		
2			X 13	32			ϕ_1
3			X 12	33			ϕ_2
4			X 11	34	GND		
5			X 10	35		FS	
6			X 9	36		DS1	
7		N. C.		37		N. C.	
8			X 8	38		N. C.	
9			X 7	39		N. C.	
10			X 6	40		DS2	
11			X 5	41		DS3	
12		N. C.		42		M	M
13		N. C.		43			FRM
14		N. C.		44		SHL	
15		N. C.		45	V_{CC}		
16			X 4	46		N. C.	
17			X 3	47		N. C.	
18			X 2	48		N. C.	
19			X 1	49		M/S	
20	V_1			50		CL	CL
21		N. C.		51		N. C.	
22		N. C.		52		N. C.	
23	V_2			53		N. C.	
24	V_5			54		DR	DR
25	V_6			55			X 20
26	V_{EE}			56			X 19
27		DL	DL	57			X 18
28	C			58			X 17
29	V_{SUB}	Connect to V_{CC}.		59			X 16
30	R			60			X 15

(Note) N.C.: Unused terminal. Don't connect any wire to these terminals. Connect V_{SUB} to V_{CC}.

● ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rated value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC}-13.5 ∿ V_{CC}+0.3	V	14
Terminal voltage (1)	V_{T1}	-0.3 ∿ V_{CC}+0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC}+0.3	V	3
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: Referred to GND=0.

Note 2: Applied to input terminals (except V1, V2, V5 and V6) and I/O common terminals.

Note 3: Applied to terminals V1, V2, V5 and V6.

Note 14: Connect a protection resistor of 220Ω±5% to V_{EE} power supply in series.

● ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, GND=0V, V_{EE}=0 to -5.5V, Ta=-20 to +75°C) (Note 4)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "high" voltage	V_{IH}		0.7×V_{CC}	-	V_{CC}	V	5
Input "low" voltage	V_{IL}		0	-	0.3×V_{CC}	V	5
Output "high" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	6
Output "low" voltage	V_{OL}	I_{OL}=+400μA	-	-	0.4	V	6
Vi-Xj ON resistance	R_{ON}	V_{EE}=-5V±10%, Load current ±150μA	-	-	500	Ω	
Input leakage current (1)	I_{IL1}	V_{IN}=V_{CC}∿GND	-1	-	1	μA	7
Input leakage current (2)	I_{IL2}	V_{IN}=V_{CC}∿V_{EE}	-2	-	2	μA	8
Shift frequency	f_{SFT}	In slave mode	-	-	50	kHz	9
Oscillation frequency	f_{OSC}	R_f=68kΩ2% C_f=10pF±5%	300	430	560	kHz	10
External clock operating frequency	f_{cp}		50	-	560	kHz	
External clock duty	Duty		45	50	55	%	11
External clock rise time	t_{rcp}		-	-	50	ns	11
External clock fall time	t_{fcp}		-	-	50	ns	11

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Dissipation power (master)	P_{w1}	CR oscillation= 430kHz	-	-	4.4	mW	12
Dissipation power (slave)	P_{w2}	Frame frequency =70Hz	-	-	1.1	mW	13

Note 4: Specified within this range unless otherwise noted.

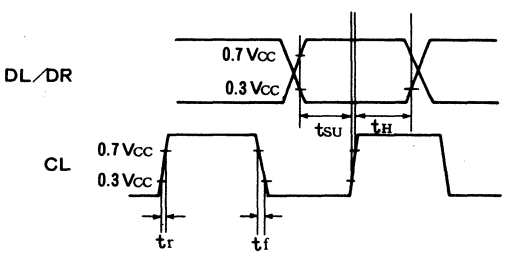
Note 5: Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR and DL.

Note 6: Applied to DL, DR, M, FRM, CL, $\phi 1$ and $\phi 2$.

Note 7: Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M and CL at high impedance.

Note 8: Applied to V1, V2, V5 and V6.

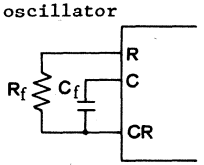
Note 9: Shift operation timing



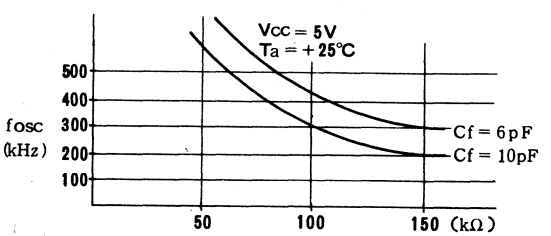
	min.	typ	max.	unit
t_{SU}	5	–	–	μs
t_H	5	–	–	μs
t_r	–	–	100	ns
t_f	–	–	100	ns

Note 10: Relationship between oscillation frequency and R_f/C_f

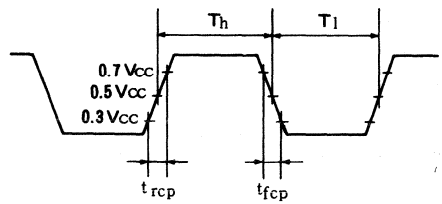
CR oscillator

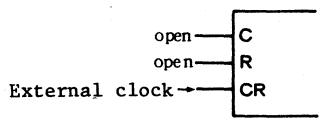


The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



Note 11:

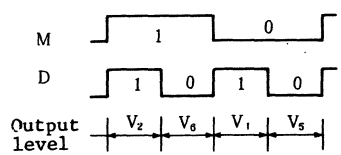
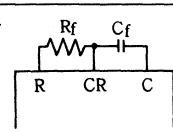




Note 12: Measured by V_{CC} terminal at output non-load of R_f=68kΩ±2% and C_f=10pF±5%, 1/32 duty in the master mode. Input terminals must be fixed at V_{CC} or GND while measuring.

Note 13: Measured by V_{CC} terminal at output non-load, 1/32 duty, frame frequency of 70Hz in the slave mode. Input terminals must be fixed at V_{CC} or GND while measuring.

● TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Function
X1∿X20	20	O	Liquid crystal display driver output. Relationship among output level, M and data (D) in shift register. 
CR, R, C	3		Oscillator  CR oscillator
M	1	I/O	Signal for converting liquid crystal display driver signal into AC Master: Output terminal Slave : Input terminal

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>Shift register shift clock.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>Frame signal, Display synchronous signal</td></tr>
<tr><td>DS1∿DS3</td><td>3</td><td>I</td><td>Display duty ratio select.
<table>
<tr><th>Display duty ratio</th><th>1/24</th><th colspan="2">1/12</th><th>X</th><th>1/32</th><th colspan="2">1/16</th><th>1/8</th></tr>
<tr><td>DS1</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>Frequency select.
The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:
FS="H": $f_{OSC} = 6144 \times f_{FPM}$ ... (1)
FS="L": $f_{OSC} = 3072 \times f_{FRM}$ ... (2)
Example 1) When FS="H", adjust Rf and Cf so that the oscillation frequency is approx. 430kHz if the frame frequency is 70Hz.
Example 2) When FS="L", adjust Rf and Cf so that the oscillation is approx. 215kHz, in order to obtain the same display waveforms as Example 1. When compared with Example 1, the power dissipation is reduced because of the operation at lower frequency. However, the operating clocks $\phi 1$ and $\phi 2$ supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102CH becomes longer.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Data I/O terminals of bidirectional shift register.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>Shift direction select of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift direction</th></tr>
<tr><td>H</td><td>DL → DR</td></tr>
<tr><td>L</td><td>DL ← DR</td></tr>
</table></td></tr>
</table>

Terminal name	Number of terminals	I/O	Function
M/S	1	I	Master/slave select. M/S="H": Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M and CL is placed in the output state. M/S="L": Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FD, DS1, DS2 and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12 or 1/16, one HD44103CH is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103CHs are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).
ϕ1, ϕ2	2	O	Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC}-GND: Power supply for internal logic V_{CC}-V_{EE}: Power supply for driver circuit logic

● BLOCK FUNCTIONS

Oscillator

The oscillator is a CR oscillator that attaches an oscillation resistor Rf and oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to ELECTRICAL CHARACTERISTICS (Note 10) to make proper adjustment.

Timing Generation Circuit

The timing generation circuit divides the signals from the oscillator and generates display timing signals (M, CL and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

This is a 20-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

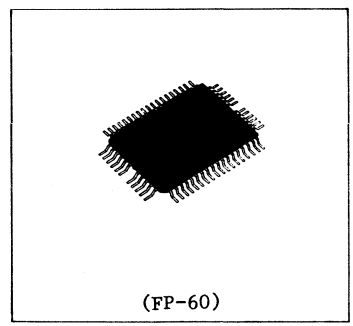
Each of 20 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

● APPLICATIONS

Refer to the applications of the HD44102CH.

HD44105H
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

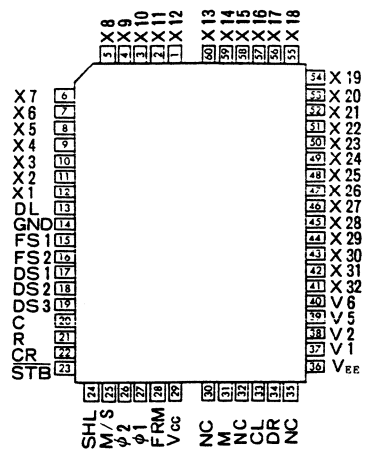
The HD44105H is a common signal driver for LCD dot matrix graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102H) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty.
It can select 7 types of display duty 1/8, 1/12, 1/16, 1/24, 1/32, 1/48 and 1/64.
It provides 32 driver output lines and the impedance is low (1kΩ max) enough to make a large screen driven.


(FP-60)

■ FEATURES

- Dot matrix graphic display common driver including the timing generation circuit.
- Internal oscillator (Oscillation frequency is selectable by attaching an oscillation resistor and an oscillation capacity.)
- Generates display timing signals.
- 32-bit bidirectional shift register for generating common signals.
- 32 liquid crystal driver circuits with low impedance.
- Selectable display duty ratio : 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64.
- Low power dissipation
- Power supplies : Vcc = +5V ± 10%
  VEE = 0 ∿ -5.5V
- CMOS process
- 60-pin flat plastic package

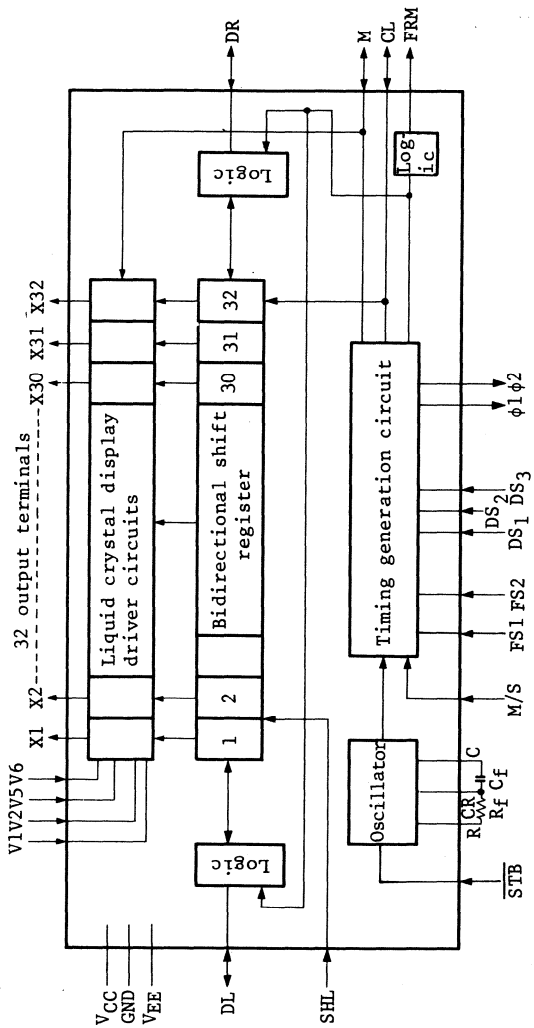
■ Pin Arrangement



(Top View)

Note) NCs show unused terminals. Don't connect any lines to them in using this LSI.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage (1)	Vcc	-0.3 ∿ +7.0	V	1
Supply voltage (2)	VEE	Vcc-13.5 ∿ Vcc+0.3	V	
Terminal voltage (1)	VT1	-0.3 ∿ Vcc+0.3	V	1, 2
Terminal voltage (2)	VT2	VEE-0.3 ∿ Vcc+0.3	V	3
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) Referred to GND = 0V.

(Note 2) Applied to input terminals (except for V1, V2, V5 and V6) and I/O common terminals.

(Note 3) Applied to terminals V1, V2, V5 and V6. Connect a protection resistor of 47Ω ± 10% to each terminal in series.

■ ELECTRICAL CHARACTERISTICS (Vcc=+5V±10%, GND=0V, VEE= 0 ∿ -5.5V, Ta= -20 ∿ +75°C) (Note 5)

Item	Symbol	Test Condition	min	typ	max	Unit	Note
Input "High" Voltage	V_{IH}		0.7×Vcc	-	Vcc	V	6
Input "Low" Voltage	V_{IL}		0	-	0.3×Vcc	V	6
Output "High" Voltage	V_{OH}	I_{OH}=-400μA	Vcc-0.4	-	-	V	7
Output "Low" Voltage	V_{OL}	I_{OL}=400μA	-	-	0.4	V	7
Vi-Xj ON Resistance	R_{ON}	V_{EE}=-5V±10%, Load Current ± 150μA	-	-	1000	Ω	
Input Leakage Current (1)	I_{IL1}	V_{IN}=Vcc ∿ GND	-1	-	1	μA	8
Input Leakage Current (2)	I_{IL2}	V_{IN}=Vcc ∿ V_{EE}	-5	-	5	μA	9
Shift Frequency	F_{SET}	in slave mode	-	-	50	kHz	10
Oscillation Frequency	f_{OSC}	Rf=68kΩ±2%, Cf=10pF±5%	300	430	560	kHz	11
External Clock Operating Frequency	f_{CP}		50	-	560	kHz	12
External Clock Duty	Duty		45	50	55	%	12
External Clock Rise Time	tr_{CP}		-	-	50	ns	12
External Clock Fall Time	tf_{CP}		-	-	50	ns	12
Dissipation Power (master)	P_{W1}	CR Oscillation, 430kHz	-	-	4.4	mW	13
Dissipation Power (Slave)	P_{W2}	Frame 70Hz	-	-	1.1	mW	14

(Note 5) Specified within this range unless otherwise noted.

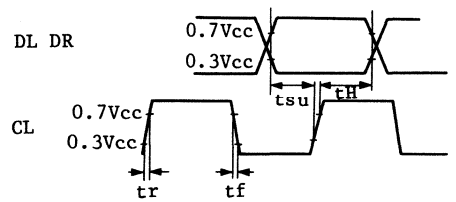
(Note 6) Applied to CR, FS1, FS2, DS1 to DS3, M, SHL, M/S, CL, DR, DL and $\overline{STB}$.

(Note 7) Applied to DL, DR, M, FRM, CL, ϕ1 and ϕ2.

(Note 8) Applied to input terminals CR, FS1, FS2, DS1 to DS3, SHL, M/S and $\overline{STB}$ and I/O common terminals DL, DR, M and CL at high impedance.

(Note 9) Applied to V1, V2, V5 and V6.

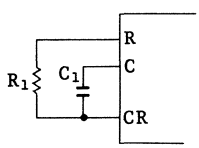
(Note 10) Shift operation timing.



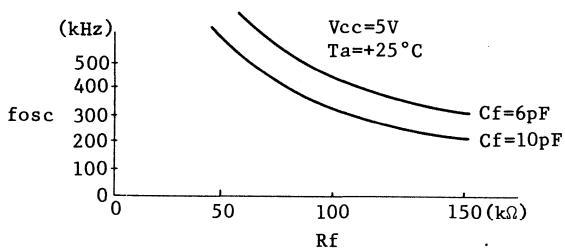
	min	typ	max	Unit
tsu	5	-	-	µs
t_H	5	-	-	µs
tr	-	-	100	ns
tf	-	-	100	ns

(Note 11) Relation between oscillation frequency and RF, Cf.

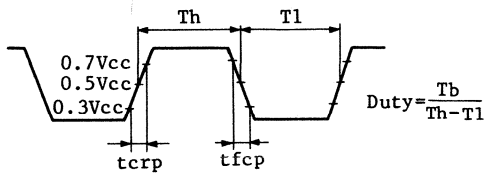
Connection

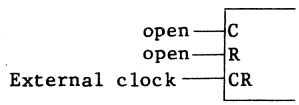


The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



(Note 12)

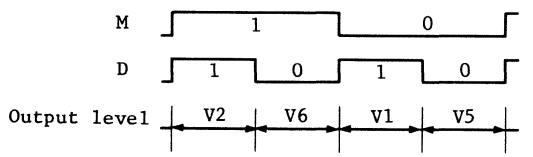
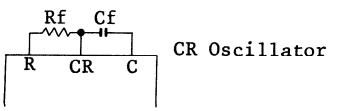




(Note 13) Measured by Vcc terminal at output non-load of Rf=68kΩ±2% and Cf=10pF±5%, and 1/32 duty in the master mode.
Input terminals are connected to Vcc or GND.

(Note 14) Measured by Vcc terminal at output non-load, 1/32 duty and frame frequency of 70Hz in the slave mode.
Input terminals are connected to Vcc or GND.

■ TERMINAL FUNCTION

<table>
<tr><th>Terminal Name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>X1 ∿ X32</td><td>32</td><td>O</td><td>Liquid crystal display driver output.
Relation among output level, M and data(D) in shift register.
 
</td></tr>
<tr><td>CR,R,C</td><td>3</td><td></td><td>Oscillator.
 

CR Oscillator</td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>Signal for converting liquid crystal display driver signal into AC.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>Shift register shift clock.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>Frame signal, Display synchronous signal</td></tr>
<tr><td>DS1∿DS3</td><td>3</td><td>I</td><td>Display duty ratio select.
<table>
<tr><th>Display duty ratio</th><th>1/8</th><th>1/16</th><th>1/32</th><th>1/64</th><th>-</th><th>1/12</th><th>1/24</th><th>1/48</th></tr>
<tr><td>DS1</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>FS1∿FS2</td><td>2</td><td>I</td><td>Selects frequency.
The relation between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows.
<table>
<tr><th>FS1</th><th>FS2</th><th>f_{OSC}(kHz)</th><th>f_{FRM}(Hz)</th><th>f_M(Hz)</th><th>f_{CP}(kHz)</th></tr>
<tr><td>L</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr>
<tr><td>H</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr>
<tr><td>L</td><td>H</td><td>215.0</td><td>70</td><td>35</td><td>107.5</td></tr>
<tr><td>H</td><td>H</td><td>430.0</td><td>70</td><td>35</td><td>215.0</td></tr>
</table>
f_{OSC}: Oscillation frequency
f_{FRM}: Frame frequency
f_M : M signal frequency
f_{CP} : Frequencies of $\phi 1$ and $\phi 2$</td></tr>
</table>

<table>
<tr><th>Terminal Name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>$\overline{STB}$</td><td>1</td><td>I</td><td>Input terminal for testing.
Connect this terminal to Vcc.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Data I/O terminals of bidirectional shift register.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift direction</th></tr>
<tr><td>H</td><td>DL → DR</td></tr>
<tr><td>L</td><td>DL ← DR</td></tr>
</table></td></tr>
<tr><td>M/S</td><td>1</td><td>I</td><td>Selects Master/Slave.
M/S='H': Master mode
The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M and CL is in the output state.
M/S='L': Slave mode
The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to Vcc. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS1, FS2, DS1, DS2, DS3, $\overline{STB}$ to Vcc.
When display duty ratio is 1/8, 1/12, 1/16, 1/24, 1/32, one HD44105H is required. Use it in the master mode.
When display duty ratio is 1/48, 1/64, two HD44105Hs are required. Use one in the master mode to drive common signals 1 to 32, and another in the slave mode to drive common signals 33 to 48(64).</td></tr>
<tr><td>ϕ1, ϕ2</td><td>2</td><td>O</td><td>Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 are half of oscillation frequency.</td></tr>
<tr><td>V1, V2, V5, V6</td><td>4</td><td></td><td>Liquid crystal display driver level power supply
V1 and V2 : Selected level
V5 and V6 : Non-selected level</td></tr>
<tr><td>V_{CC}, GND V_{EE}</td><td>3</td><td></td><td>Power supply
V_{CC} - GND : Power supply for internal logic.
V_{CC} - V_{EE} : Power supply for driver circuit logic.</td></tr>
</table>

■ BLOCK FUNCTIONS

- Oscillator

A CR oscillator that attaches an oscillation resistor Rf and an oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to ELECTRICAL CHARACTERISTICS (Note 11) to make proper adjustment.

- Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS1, FS2 and DS1 to DS3. However, connect them to Vcc to prevent floating current.

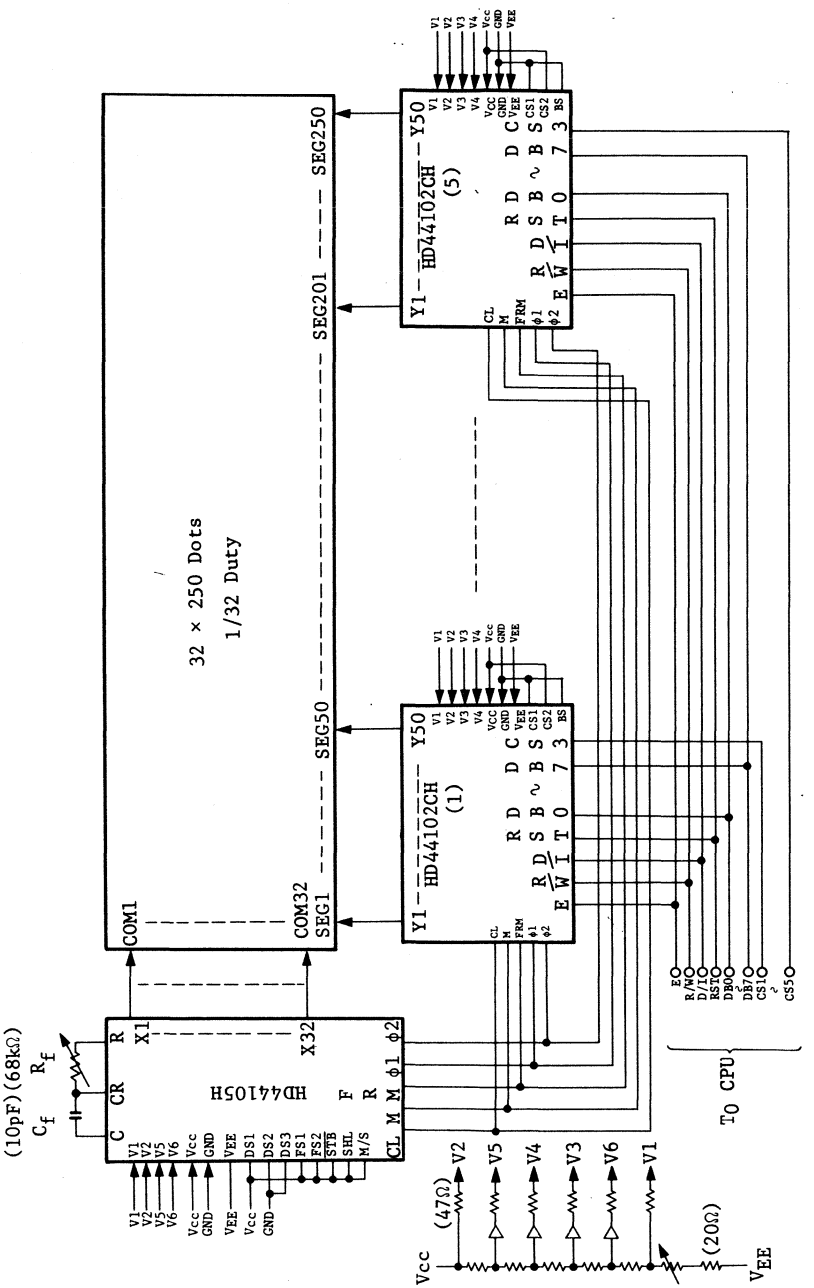
- Bidirectional Shift Register

A 32-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

- Liquid Crystal Display Driver Circuit

Each of 32 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

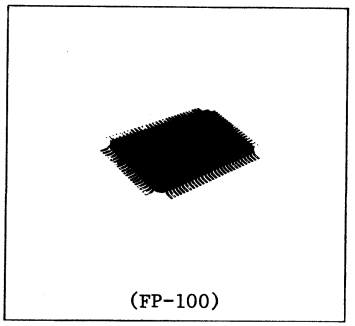
■ Connection between HD44105H and HD44102CH



HD61100A
(LCD Driver with 80-Channel Output)

The HD61100A is a driver LSI for liquid crystal display systems. It receives serial display data from a micro computer or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

It has liquid crystal driving outputs which corresponds to internal 80-bit flip flops. Both static drive and dynamic drive are possible according to the combination of transfer clock frequency and latch clock frequency.



(FP-100)

■ FEATURES

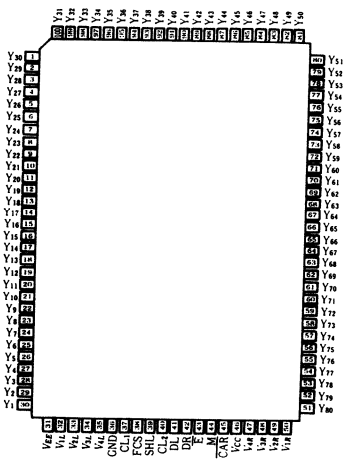
- Liquid crystal display driver with serial/parallel conversion function.
- Internal liquid crystal display driver
  ..... 80 drivers
- Display duty

  Any duty is selectable according to combination of transfer clock and latch clock.
- Data transfer rate .... 2.5 MHz max
- Power supply

  Vcc - +5V±10% (Internal logic)

  VEE - 0 ∿ -11.5V (Liquid crystal display driver circuit)
- Liquid crystal driving level....17.0V max.
- CMOS process
- 100-pin flat plastic package (FP-100)

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	Vcc-19.0 to Vcc+0.3	V	
Terminal voltage (1)	V_{T1}	-0.3 to Vcc +0.3	V	2, 3
Terminal voltage (2)	V_{T2}	VEE-0.3 to Vcc+0.3	V	4
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destoryed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, $\overline{E}$ and M.

(Note 4) Applies to V_{1L} V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain

$V_{CC} \geq V_{1L}=V_{1R} \geq V_{3L}=V_{3R} \geq V_{4L}=V_{4R} \geq V_{2L}=V_{2R} \geq V_{EE}$.

Connect a protection resistor of 15Ω±10% to each terminals in series.

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS

(Vcc=5V±10%, GND=0V, V_{EE}=0∿-11.5V, Ta=-20∿+75°C)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Input "High" voltage	V_{IH}		0.7xV_{CC}	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		-	-	0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=+400μA	-	-	0.4	V	2
Driver ON Resistance	R_{ON}	VEE=-10V, Load current= 100μA	-	-	7.5	kΩ	3
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1	-	+1	μA	1
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-2	-	+2	μA	4
Dissipation Current(1)	I_{GND}		-	-	1.0	mA	5
Dissipation Current(2)	I_{EE}		-	-	0.1	mA	5

(Note 1) Applies to CL1, CL2, FCS, SHL, $\overline{E}$, M, DL and DR.

(Note 2) Applies to DL, DR and $\overline{CAR}$.

(Note 3) Applies to Y1 ∿ Y80.

(Note 4) Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}.

(Note 5) Specified when display data is transfered under following conditions.

CL2 frequency f_{CP2} = 2.5MHz (data transfer rate)

CL1 frequency f_{CP1} = 4.48kHz (data latch frequency)

M frequency f_M = 30Hz (frame frequency/2)

Specified when V_{IH}=V_{CC}, V_{IL}=GND and no load on outputs.

I_{GND} : currents between V_{CC} and GND.

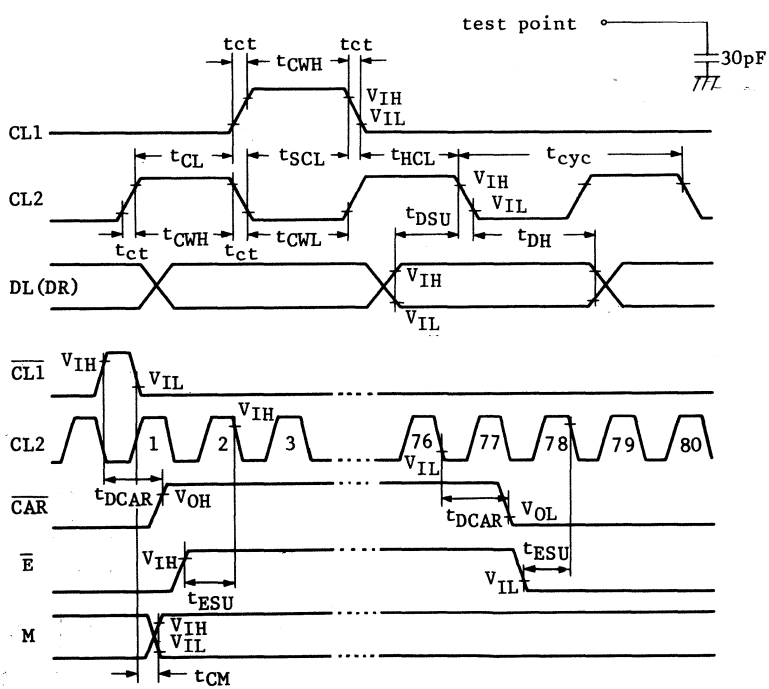
I_{EE} : currents between V_{CC} and V_{EE}.

- AC CHARACTERISTICS

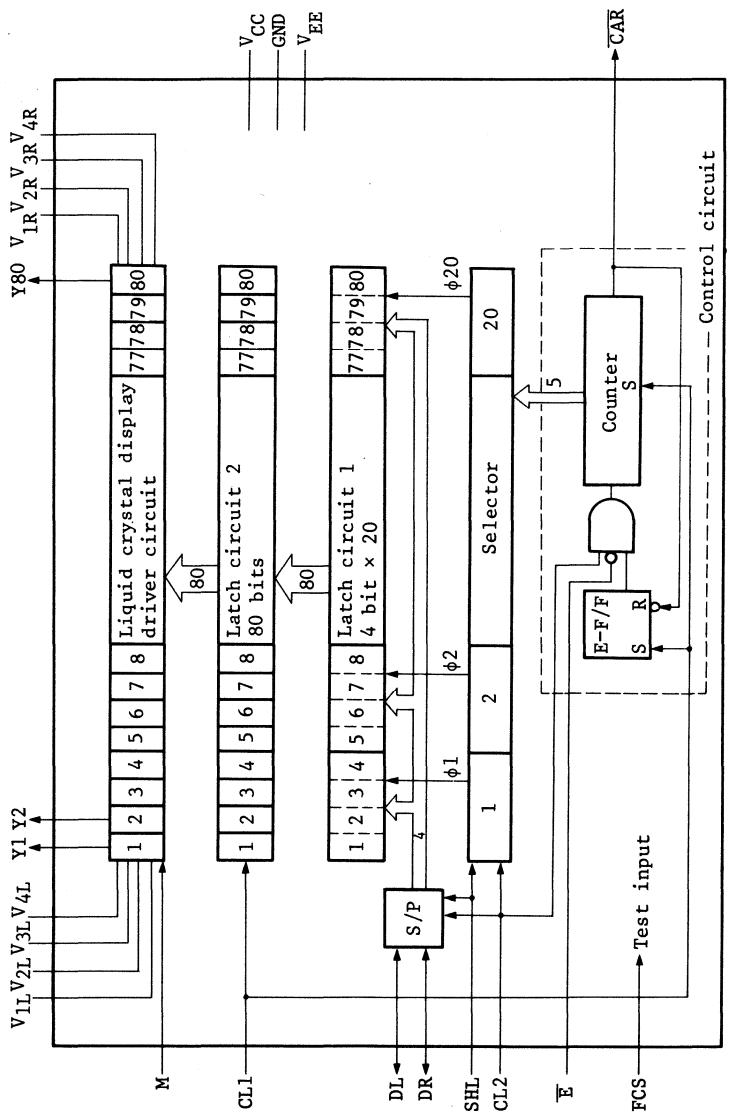
(V_{CC}=5V±10%, GND=0V, V_{EE}=0V∿-11.5V, Ta=-20∿+75°C)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Clock cycle time	t_{CYC}		400	-	-	ns	
Clock high level width	t_{CWH}		150	-	-	ns	
Clock low level width	t_{CWL}		150	-	-	ns	
Clock setup time	t_{SCL}		100	-	-	ns	
Clock hold time	t_{HCL}		100	-	-	ns	
Clock rise/fall time	t_{Ct}		-	-	30	ns	
Clock phase different time	t_{CL}		100	-	-	ns	
Data setup time	t_{DSu}		80	-	-	ns	
Data hold time	t_{DH}		100	-	-	ns	
E setup time	t_{ESu}		200	-	-	ns	
Output delay time	t_{DCAR}		-	-	300	ns	1
M phase difference time	t_{CM}		-	-	300	ns	

(Note 1) The following load circuits are connected for specification:



■ BLOCK DIAGRAM



■ BLOCK FUNCTION

• Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

• 80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

• S/P

Serial/Parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is "L" level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR which is in the output status.
When SHL is "H" level, input data from terminal DR without connecting any lines to terminal DL.

• 80-bit Latch Circuit 1

The 4-bit data is latched at $\phi 1 \sim \phi 20$ and output to latch circuit 2. When SHL is "L" level, the data from DL are latched one in order of 1→2→3 ... →80 of each latch. When SHL is "H" level, they are latched in a reverse order (80→79→78 ... →1).

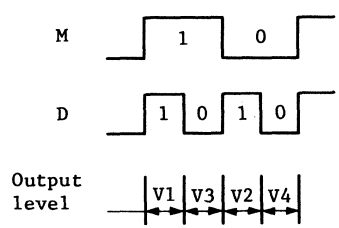
• Selector

The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1 \sim \phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

• Control Circuit

Controls operation : When E-F/F (enable F/F) indicates "1", S/P conversion is started by inputting "L" level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into "L" level and E-F/F is reset to "0", and consequently the conversion stops. E-F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at "H" level of CL1.
Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into "H" level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61100A.

■ TERMINAL FUNCTIONS DESCRIPTION

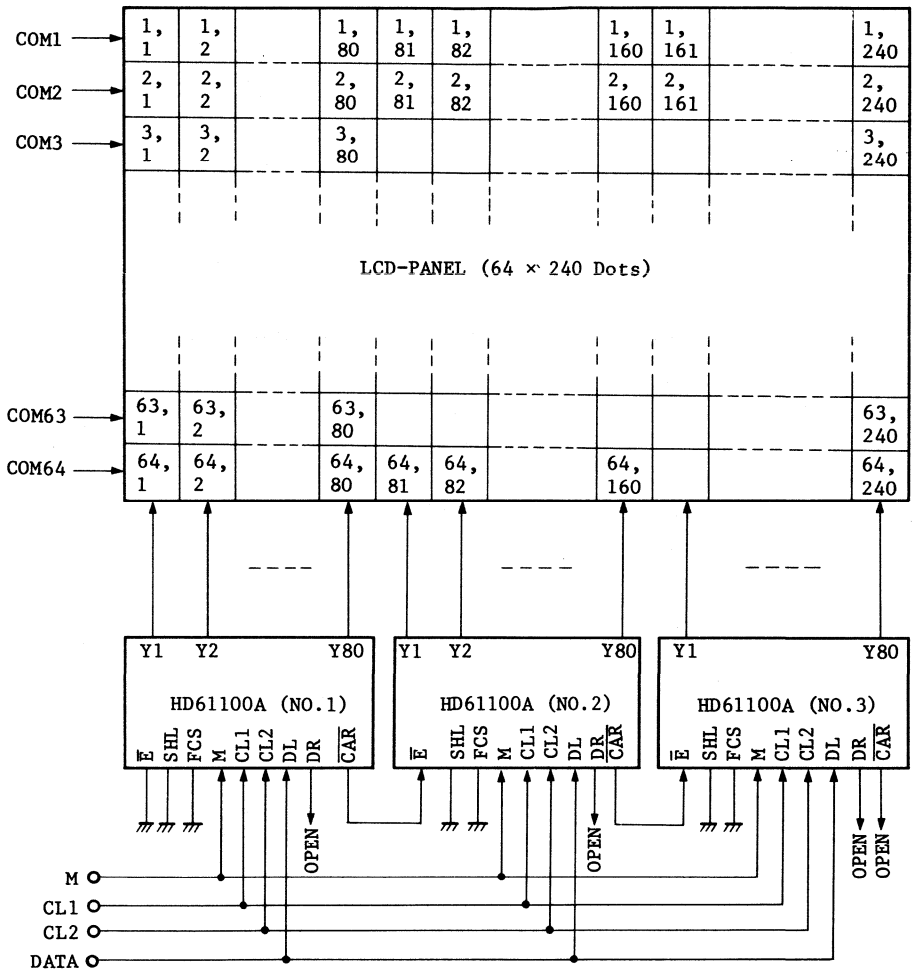
Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC}-GND : Power supply for internal logic V_{CC}-V_{EE} : Power supply for LCD drive circuit
V_{1L}∿V_{4L} V_{1R}∿V_{4R}	8		Power supply	Power supply for liquid crystal drive V_{1L} (V_{1R}), V_{2L} (V_{2R})...selection level V_{3L} (V_{3R}), V_{4L} (V_{4R})...non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1∿Y80	80	O	LCD	Liquid crystal driver outputs Selects one of the 4 levels, V1, V2, V3 and V4. Relation among output level, M and display data (D) is as follows. 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger). Synchronizing with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D) Fall edge trigger

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Controller</td><td>Input of serial display data (D)
<table>
<tr><th>(D)</th><th>Liquid crystal driver output</th><th>Liquid crystal display</th></tr>
<tr><td>1 (H level)</td><td>selection level</td><td>ON</td></tr>
<tr><td>0 (L level)</td><td>non-selection level</td><td>OFF</td></tr>
</table>
I/O status of DL and DR terminals depends on SHL input level.
<table>
<tr><th>SHL</th><th>DL</th><th>DR</th></tr>
<tr><td>H level</td><td>O</td><td>I</td></tr>
<tr><td>L level</td><td>I</td><td>O</td></tr>
</table></td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of serial data. When the serial data (D) is input in order of D1→···→D80, the relations between the data (D) and output Y are as follows.
<table>
<tr><td>SHL</td><td>Y1</td><td>Y2</td><td>Y3</td><td>....</td><td>Y80</td></tr>
<tr><td>"L"</td><td>D1</td><td>D2</td><td>D3</td><td>....</td><td>D80</td></tr>
<tr><td>"H"</td><td>D80</td><td>D79</td><td>D78</td><td>....</td><td>D1</td></tr>
</table>
When SHL is "L", data is input from the terminal DL. Any lines should not be connected to the terminal DL, as it is in the state of output.
When SHL is "H", the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61100A</td><td>Controls the S/P conversion.
The operation stops with "H" level, and the S/P conversion starts with "L" level.</td></tr>
</table>

Terminal name	Number of terminals	I/O	Connected to	Functions
$\overline{CAR}$	1	O	the input terminal $\overline{E}$ of the HD61100A	Used for cascade connection with the HD61100A to increase the number of bit which can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

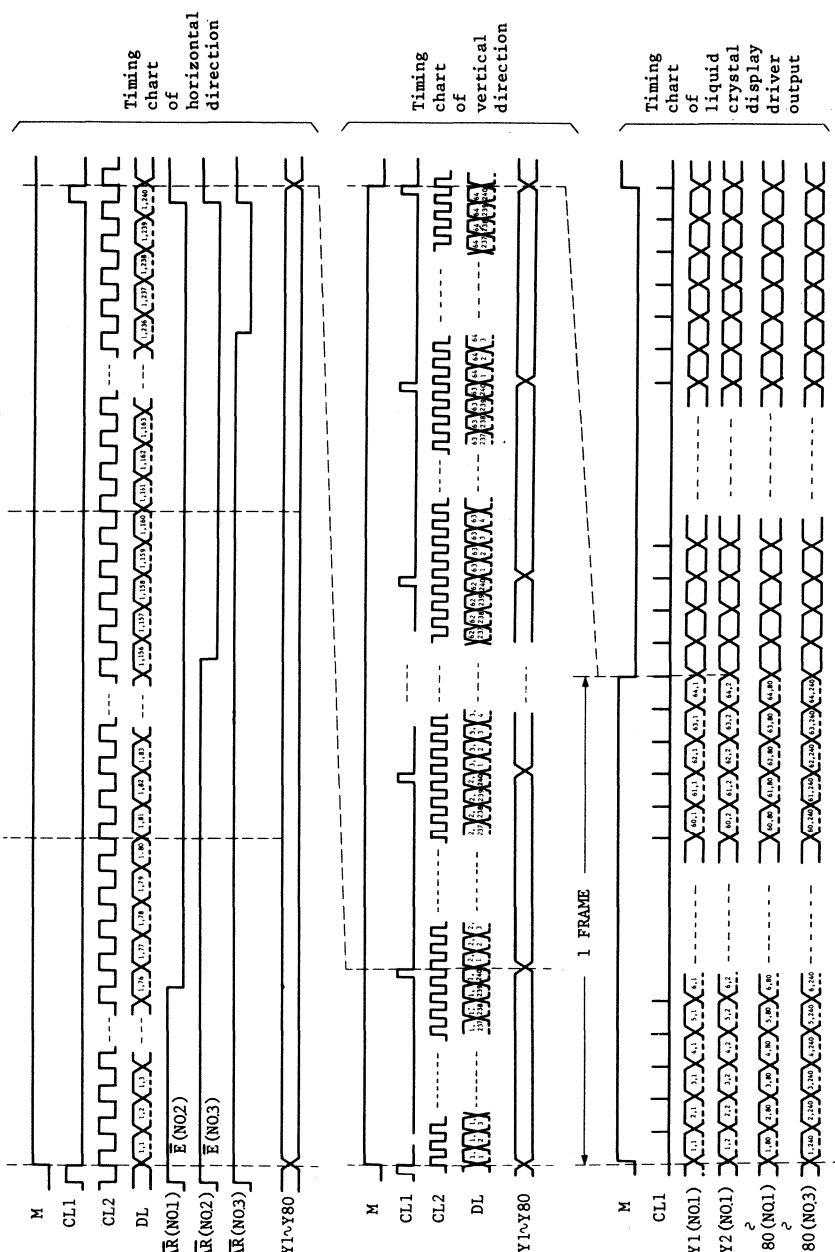
■ THE OPERATION OF THE HD61100A

The following is the LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty dynamic drive. Fig. 1 is an example of liquid crystal display and connection to HD61100A's. Fig. 2 shows a time chart of I/O signals of HD61100A.



Cascade three HD61100As. Input data to the terminal DL of NO.1, NO.2 and NO.3. Connect $\overline{E}$ of NO.1 to GND. Don't connect any lines to $\overline{CAR}$ of NO.3. Connect common signal terminals (COM1 ∿ COM64) to X1 ∿ X64 of common driver HD61103A. (m,n) of LCD panel is the address corresponding to each dot.

Fig. 1 LCD driver with 64 × 240 dots

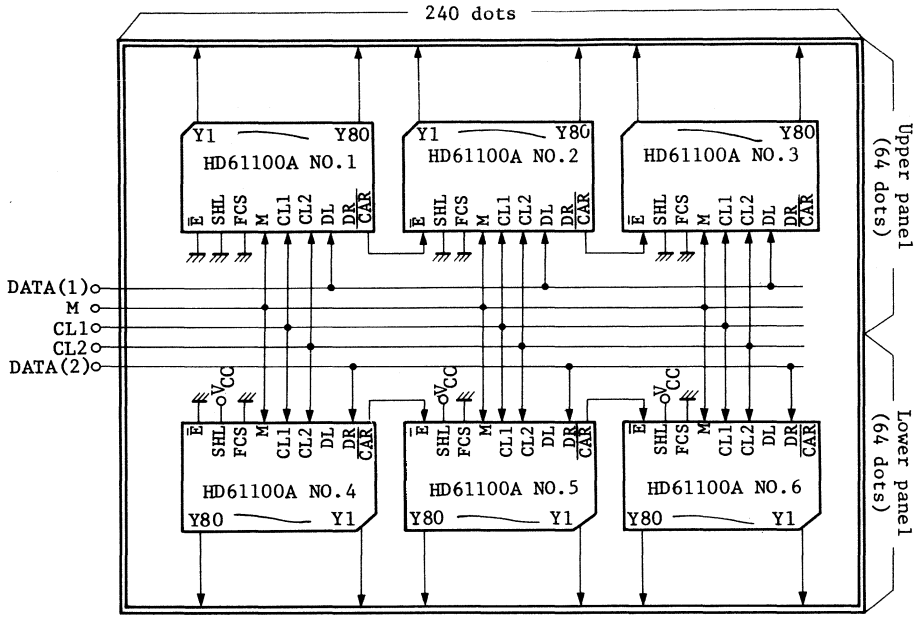


Timing chart in the example of connection of Fig.1. DL input (m,n) is the data which corresponds to each address (m,n) of LCD panel.

Fig. 2 HD61100A Timing Chart

■ EXAMPLE OF APPLICATION

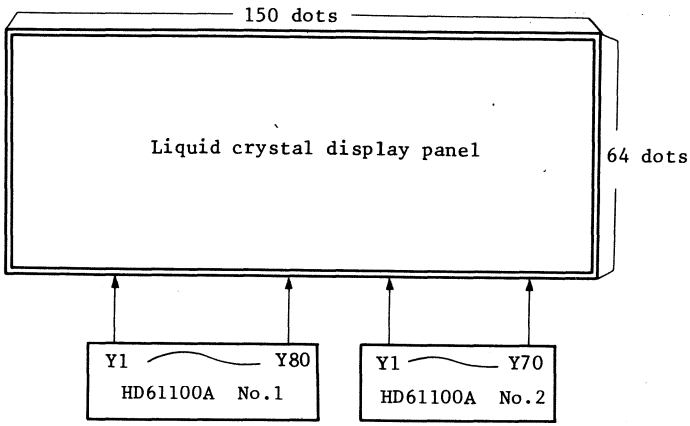
- An example of 128 × 240 dot liquid crystal display (1/64 duty)



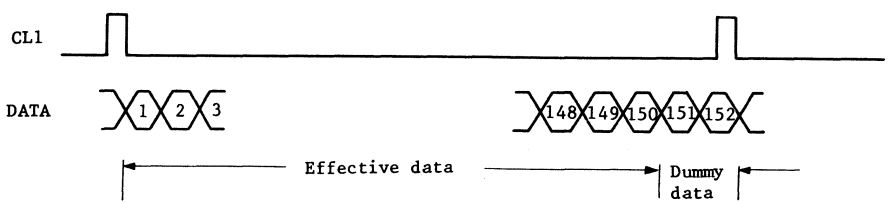
Liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61100As of No.1 ∿ No.3 drive upper half. Serial data, which are input from DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} terminal of No.1, then at $Y_1 \rightarrow Y_2 \rightarrow$-- Y_{80} of No.2 and then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No.3 in order where they were input. (in the case of SHL=L). HD61100As of No.4 ∿ No.6 drive lower half. Serial data, which are input from DATA(2) terminal, appear at $Y_{80} \rightarrow T_{79} \rightarrow$ -- Y_1 of No.4, then at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.5 and then $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.6 in order where they were input (in the case of SHL=H).

As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

- Example of 64 × 150 dot liquid crystal display (1/64 duty, SHL=L)



4-bit parallel process is used in this LSI to lessen the power dissipation. Thus, the sum of the dots in lateral direction has to be multiple of 4. If not, as this example, consideration is needed to input signals.



As the sum of dots in lateral direction is 150, 2 more dummy data bits are transferred. (152=4 × 38).
Dummy data, which is output from Y71 and Y72 of NO.2, can be either "0" or "1" because these terminals do not connect with the liquid crystal display panel.

HD61102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

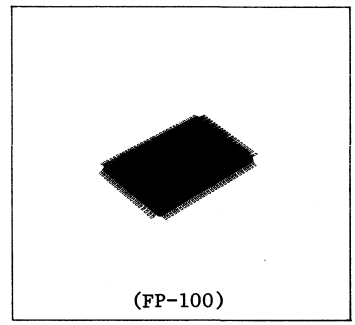
HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-computer in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

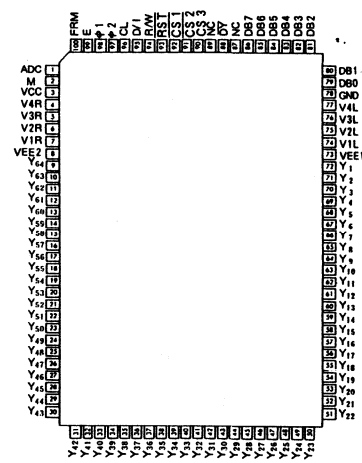
The HD61102, which is produced in the CMOS process, can accomplish a portable battery drive equipment by combining a CMOS micro-computer, utilizing the liquid crystal display's lower power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration by combining the row (common) driver HD61103A.



(FP-100)

■ PIN ARRANGEMENT



(Top view)

■ FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- RAM data direct display by internal display RAM
  RAM bit data "1" ..... ON
  RAM bit data "0" ..... OFF
- Internal display RAM address counter
  preset, increment
- Display RAM capacity ..... 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit 64
- Display duty
  Combination of frame control signal and data latch synchronization signal make it possible to select out of static through an optional duty.
- Wide range of instruction function
  Display Data Read/Write, Display ON/OFF,
  Set address, Set Display Start line,
  Read Status
- Lower power dissipation ———during display 2mW max
- Power supply Vcc ———+5V ± 10%
  VEE ——— 0V ∿ -10V
- Liquid crystal display driving level——15.5V max
- CMOS process
- 100 - pin flat plastic package (FP-100)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	2
	V_{EE}	V_{CC} -16.5 ∿ V_{CC} +0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} -0.3 ∿ V_{CC} +0.3	V	4
Terminal voltage (2)	V_{T2}	-0.3 ∿ V_{CC} +0.3	V	2, 5
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) LSI's may be destroyed for ever, if being used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them observing the recommended operation conditions.
Using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=OV.

(Note 3) Apply the same supply voltage to V_{EE} 1 and V_{EE}2.

(Note 4) Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R and V4R.
Maintain
$Vcc \geq V1L=V1R \geq V3L=V3R \geq V4L=V4R \geq V2L=V2R \geq VEE$

(Note 5) Applies to M, FRM, CL, $\overline{RST}$, ADC, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC and DB0∿7.

■ ELECTRICAL CHARACTERISTICS
(GND=0V, VCC=4.5 ∿ 5.5V, VEE=0∿-10V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit	Note
			min	typ	max		
Input "High" voltage	V_{IHC}		0.7×Vcc	-	Vcc	V	1
	V_{IHT}		2.0	-	Vcc	V	2
Input "Low" voltage	V_{ILC}		0	-	0.3×Vcc	V	1
	V_{ILT}		0	-	0.8	V	2
Output "High" voltage	V_{OH}	IOH=-205μA	2.4	-	-	V	3
Output "Low" voltage	V_{OL}	IOL=1.6mA	-	-	0.4	V	3
Input leakage current	I_{IL}	Vin=GND∿Vcc	-1.0	-	+1.0	μA	4
Three state (OFF) input current	I_{TSL}	Vin=GND∿Vcc	-5.0	-	+5.0	μA	5
Liquid crystal supply leakage current	I_{LSL}	Vin=VEE∿Vcc	-2.0	-	+2.0	μA	6
Driver ON resistance	R_{ON}	Vcc-VEE=15V $\pm I_{LOAD}$=0.1mA	-	-	7.5	KΩ	7
Dissipation current	Icc(1)	During display	-	-	100	μA	8
	Icc(2)	During access, access cycle=1MHz	-	-	500	μA	8

(Note 1) Applies to M, FRM, CL, $\overline{RST}$, ADC, ADC, φ1 and φ2.

(Note 2) Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I and DB0 ∿ 7.

(Note 3) Applies to DB0 ∿ 7.

(Note 4) Applies to terminals except for DB0 ∿ 7.

(Note 5) Applies to DB0 ∿ 7 at high impedance.

(Note 6) Applies to V1L ∿ V4L and V1R ∿ V4R.

(Note 7) Applies to Y1 ∿ Y64.

(Note 8) Specified when liquid crystal display is in 1/64 duty.
Operation frequency f_{CLK}=250 kHz (φ1 and φ2 frequency)
Frame frequency f_M =70 Hz (FRM frequency)

Specified in the state of
Output terminal ----- not loaded
Input level --------- V_{IH}=Vcc(V)
V_{IL}=GND (V)

Measured at Vcc terminal

● INTERFACE AC CHARACTERISTICS

(1) MPU Interface

(GND=0V, Vcc=4.5 ∿ 5.5V, V_{EE}=0 ∿ -10V, Ta=-20 ∿ +75°C)

Item	Symbol	min	typ	max	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	P_{WEH}	450	-	-	ns	1, 2
E low level width	P_{WEL}	450	-	-	ns	1, 2
E rise time	tr	-	-	25	ns	1, 2
E fall time	tf	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	20	-	-	ns	2

(Note 1)

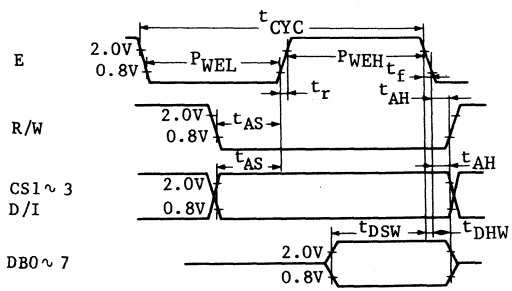


Fig. 1 CPU Write Timing

(Note 2)

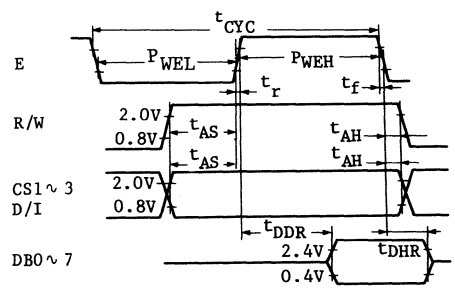
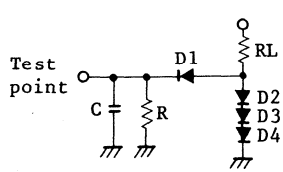


Fig. 2 CPU Read Timing

(Note 3) DB0 ∿ 7 : load circuit



RL=2.4KΩ

R =11KΩ

C =130pF (including jig capacity)

Diodes D1 to D4 are all 1S2074Ⓗ.

(2) Clock Timing

(GND=0V, Vcc=4.5 ∿ 5.5V, V_{EE}=0 ∿ -10V, Ta=20 ∿ +75°C)

Item	Symbol	Test condition	Limit			Unit
			min	typ	max	
φ1, φ2 cycle time	tcyc	Fig. 3	2.5	-	20	μs
φ1 "Low" level width	$t_{WL\phi1}$	Fig. 3	625	-	-	ns
φ2 "Low" level width	$t_{WL\phi2}$	Fig. 3	625	-	-	ns
φ1 "High" level width	$t_{WH\phi1}$	Fig. 3	1875	-	-	ns
φ2 "High" level width	$t_{WH\phi2}$	Fig. 3	1875	-	-	ns
φ1-φ2 phase difference	t_{D12}	Fig. 3	625	-	-	ns
φ2-φ1 phase difference	t_{D21}	Fig. 3	625	-	-	ns
φ1, φ2 rise time	tr	Fig. 3	-	-	150	ns
φ1, φ2 fall time	tf	Fig. 3	-	-	150	ns

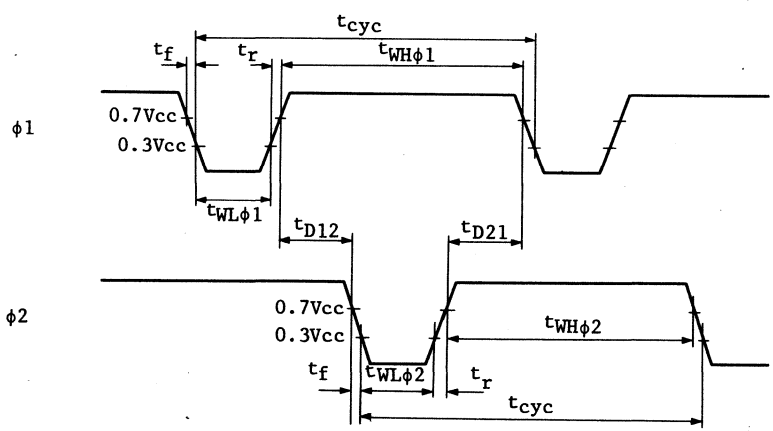


Fig. 3 External Clock Waveform

(3) Display Control Timing

(GND=0V, V_{CC}=4.5 ∿ 5.5V, V_{EE}=0 ∿ -10V, Ta=-20 ∿ +75°C)

Item	Symbol	Test condition	Limit			Unit
			min	typ	max	
FRM delay time	t_{DFRM}	Fig. 4	-2	-	+2	µs
M delay time	t_{DM}	Fig. 4	-2	-	+2	µs
CL "Low" level width	t_{WLCL}	Fig. 4	35	-	-	µs
CL "High" level width	t_{WHCL}	Fig. 4	35	-	-	µs

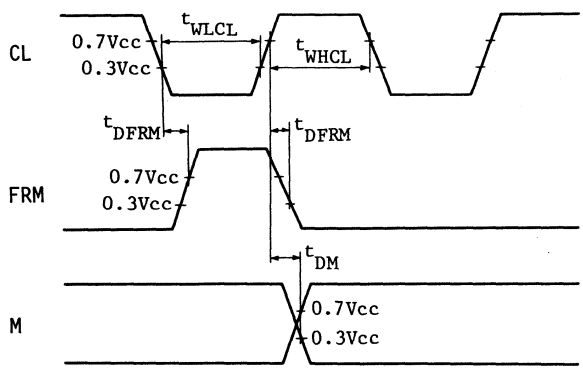
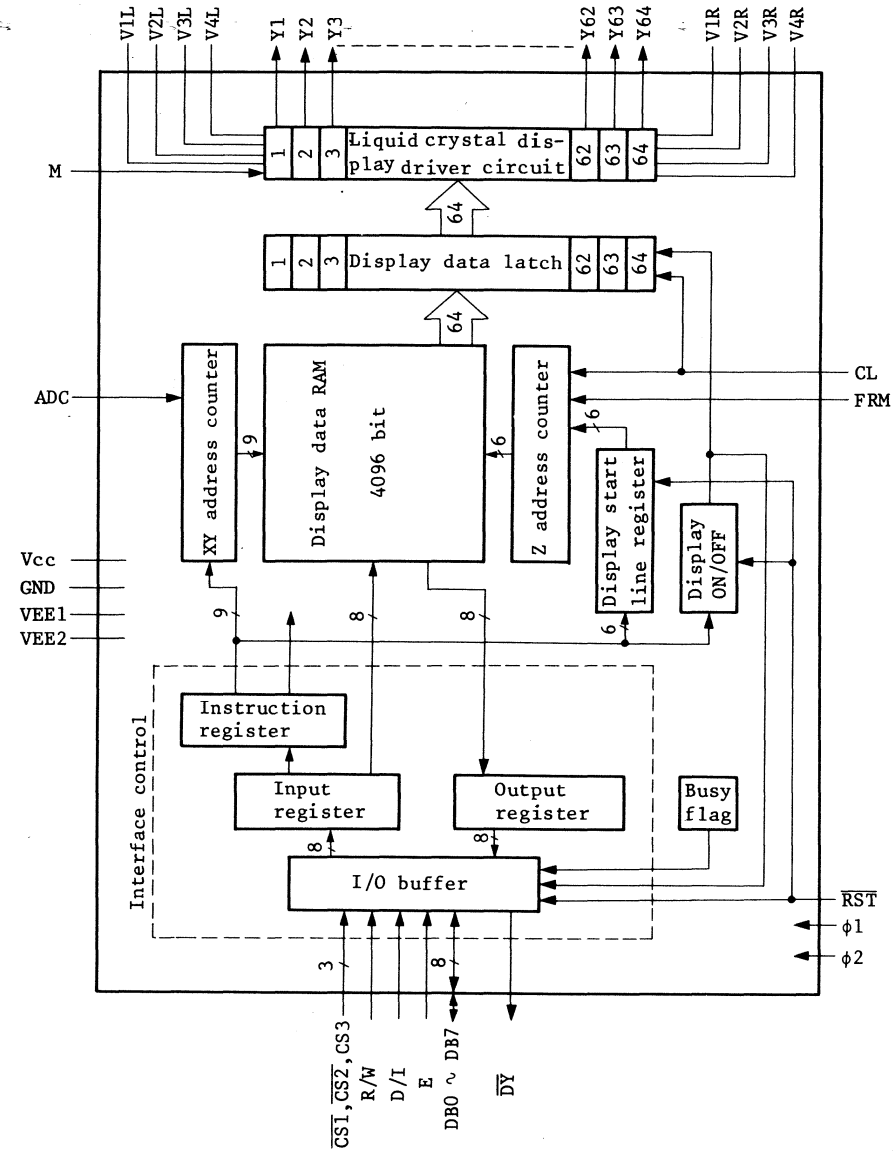


Fig. 4 Display Control Signal Waveform

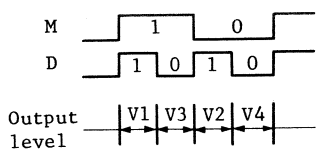
■ BLOCK DIAGRAM



■ TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0V V_{CC} = +5V ± 10%
V_{EE} 1 V_{EE} 2	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V_{CC} - 15 to GND. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L(V1R), V2L(V2R)---Selection level V3L(V3R),V4L(V4R)----Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the next conditions. Terminal name: $\overline{CS1}$ $\overline{CS2}$ CS3 Condition: 'L' 'L' 'H'
E	1	I	MPU	Enable At write(R/W=L) : Data of DB0 to DB7 is latched at the fall of E. At read(R/W=H) : Data appears at DB0 to DB7 while E is in "High" level.

Terminal name	Number of terminals	I/O	Connected to	Functions
R/W	1	I	MPU	Read/Write R/W=H : Data appears at DB0 to DB7 and can be read by the CPU When E=H, $\overline{CS1}$, $\overline{CS2}$=L and CS3=H. R/W=L : DB0 to DB7 can accept at fall of E when $\overline{CS1}$, $\overline{CS2}$=L and CS3=H.
D/I	1	I	MPU	Data/Instruction D/I=H : Indicates that the data of DB0 to DB7 is display data. D/I=L : Indicates that the data of DB0 to DB7 is display control data.
ADC	1	I	V_{CC}/GND	Adress control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H : Y1-$0, Y64-$63 ADC=L : Y64-$0, Y1-$63
DB0∿DB7	8	I/O	MPU	Data bus, three-state I/O common terminal
M	1	I	HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61103A	Display synchronous signal (frame signal) This signal presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61103A	Syncronous signal to latch display data. The CL signal indicates to count up the display output adress counter and latch the display data at rising.
Φ1,Φ2	1	I	HD61103A	2-phase clock signal for internal operation. The Φ1 and Φ2 clocks are used to perform the operations (I/O of display data and execution of instructions) other than display.

Terminal name	Number of terminals	I/O	Connected to	Functions
Y1∿Y64	64	O	Liquid criptal display	Liquid crystal display column (segment) drive output. These pins outputs light ON level when "1" is in the display RAM, and light OFF level with "0" in it. Relation among output level, M and display data (D) is as follows. 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to "Low" level. (1) ON/OFF register 0 set (display OFF) (2) Display start line register 0 line set (displays from 0 line) After releasing reset, this condition can be changed only by the instruction.
$\overline{DY}$	1	O	Open	Output terminal for test. Usually, don't connect any lines to this terminal.
NC	2		Open	Unused terminals. Don't connect any lines to these terminals.

(Note) "1" corresponds to "High level" in positive logic.

■ FUNCTION OF EACH BLOCK

• ● Interface Control

(1) I/O buffer

Data is transferred through 8 data buses (DB0 ∿ DB7).

DB7 .... MSB (Most Significant Bit)

DB0 .... LSB (Least Significant Bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, namely, the internal state is maintained and no instruction excute. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

(2) Register

Both input register and output register are provided to interface to MPU of which the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

Table 1. Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

① Input register

Input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of E signal.

② Output register

Output register is used to store data temporarily which is read from display data RAM. To read out the data from output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With READ instruction, data stored in the output register is output while E is "H" level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address can not be output with READ instruction soon after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Fig. 5 shows the CPU read timing.

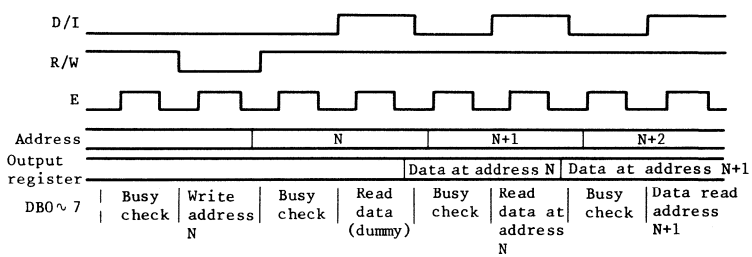
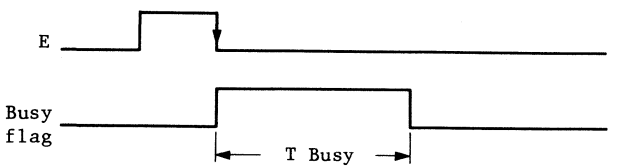


Fig. 5 CPU Read Timing

- Busy Flag

"1" of busy flag indicates that HD61102 is on the move and any instructions except Status Read instruction can not be accepted. The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset ("0") before the issue of instruction.



$1/f_{CLK} \leqq T\ Busy \leqq 3/f_{CLK}$

f_{CLK} is $\phi 1$, $\phi 2$ frequency

- Display ON/OFF Flip Flop

Display ON/OFF flip flop selects one of two states, ON state and OFF state of segments Y1 to Y64. In ON state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in OFF state independent of the data in RAM.
It is controlled by display ON/OFF instruction. 'O' of $\overline{RST}$ signal sets the segments in OFF state. The status of the flip flop is output to DB5 by Status Read instruction. Display ON/OFF instruction does not influence data in RAM. To control display data latch by this flip flop, CL signal (display synchronous signal) should be input correctly.

- Display Start Line Register

The register specifies a line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.
6-bit display start line information is written into this register by display start line set instruction, with 'H' level of FRM signal instructing to start the display, the information in this register is transferred to Z address counter which controls the display address, and the Z address counter is preset.

- X, Y Address Counter

This is a 9-bit counter which designates addresses of internal display data RAM. X address counter of upper 3 bits and Y address counter of lower 6 bits should be set each address by respective instruction.

(1) X address counter

Ordinary register with no count functions. An address is set in by instructions.

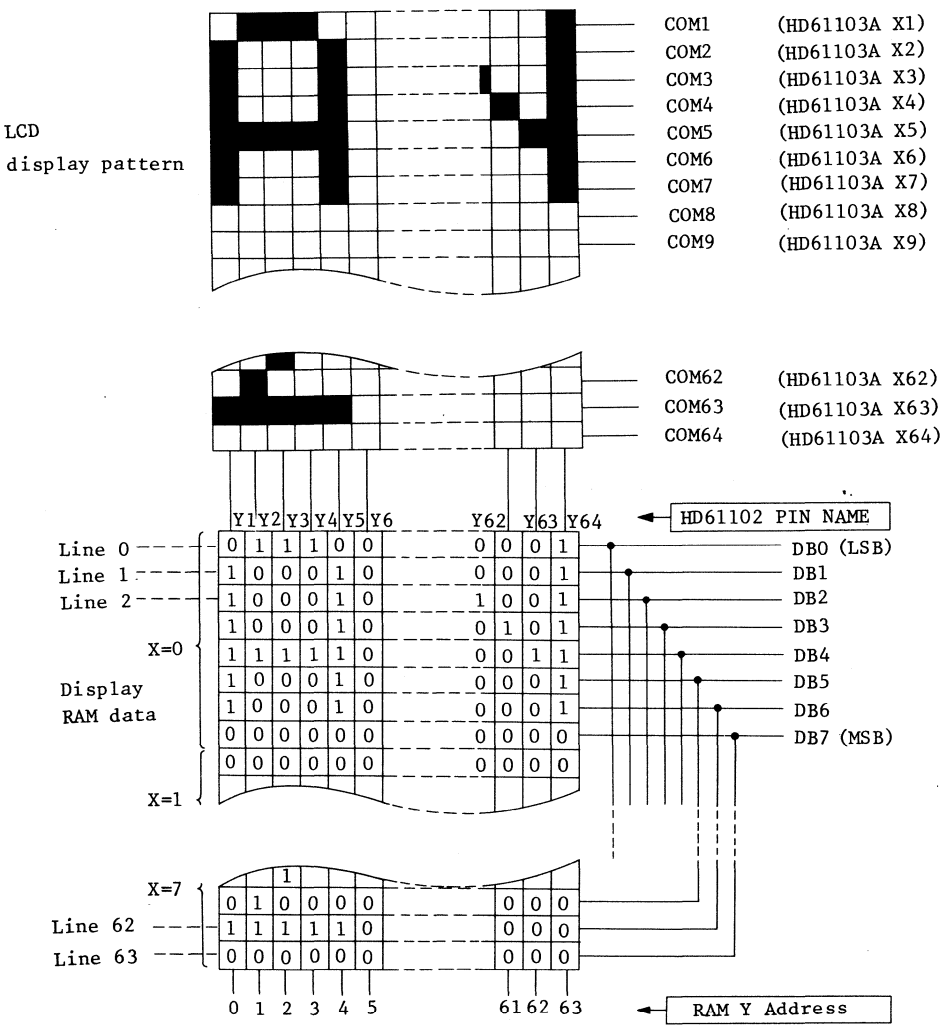
(2) Y address counter

An address is set in by instruction and it is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

- Display Data RAM

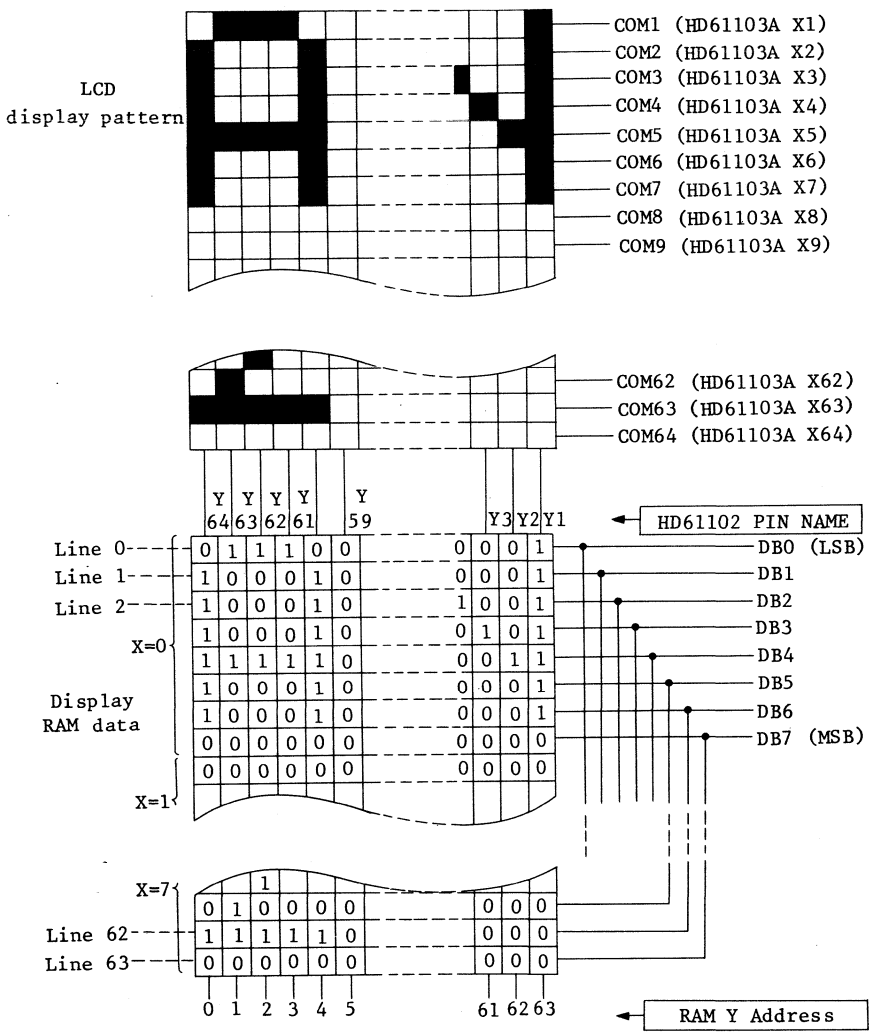
Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light ON (data=1) and light OFF (data=0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.
As ADC signal controls Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Fig. 6 shows the relations between Y address of RAM and segment pins in the cases of ADC=1 and ADC=0. (display start line=0, 1/64 duty).



(a) ADC="1" (Connected to Vcc)

Fig. 6 Relation between RAM Data and Display



(b) ADC="0" (Connected to GND)

Fig. 6 Relation Between RAM Data and Display

- Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6-bit and counts up at the fall of CL signal. With "H" level of FRM, the contents of the display start line register is preset at the Z counter.

- Display data Latch

The display data latch stores the display data temporarily which is output from display data RAM to liquid crystal driving circuit.
Data is latched at the rise of CL signal. Display ON/OFF instruction controls the data in this latch and does not influence data in display data RAM.

- Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

- Reset

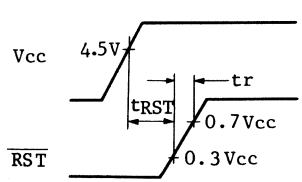
The system can be initialized by setting $\overline{RST}$ terminal at "Low" level when turning power ON.

1) Display-OFF
2) Set display start line register 0 line.

While $\overline{RST}$ is in Low level, any instruction except Status Read cannot be accepted. Therefore, Carry out other instructions after making sure that DB4=0 (clear RESET) and DB7=0 (Ready) by Status Read instruction.
The conditions of Power Supply at initial power up are as follows.

Item	Symbol	Min.	Typ	Max.	Unit
Reset time	t_{RST}	1.0	-	-	μs
Rise time	t_r	-	-	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the register except ON/OFF register and in RAM.



■ DISPLAY CONTROL INSTRUCTIONS

• Outline

Table 2 shows the instructions. Read/Write (R/W) signal, Data/Instruction (D/I) signal and Data bus signal (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.
These explanations are detailed from the following page. Generally, there are following three kinds of instructions.

(1) Instruction to give addresses in the internal RAM
(2) Instruction to transfer data from/to the internal RAM
(3) Other instructions

In general use, the instruction (2) are used most frequently. But, since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be lessened. During the execution of an instruction, the system cannot accept other instructions than Status Read instruction. Send instructions from MPU after making sure if the busy flag is "0", which is the proof an instruction is not being excuted.

Table 2. Instructions

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1 Display ON/OFF	0	0	0	0	1	1	1	1	1	1/0	Controls the ON/OFF of display. RAM data and internal status are not affected. 1:ON, 0:OFF.	
2 Display start line	0	0	1	1	display start line (0∿63)						Specifies a RAM line displayed at the top of the screen.	
3 Set page (X address)	0	0	1	0	1	1	1	Page (0∿7)			Sets the page (X address) of RAM at the page (X address) register.	
4 Set Y address	0	0	0	1	Y address (0∿63)						Sets the Y address at the Y address counter	
5 Status Read	1	0	Busy	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: reset 0:normal ON/OFF 1: display OFF 0:display ON Busy 1: on the internal operation 0: Ready	
6 Write display data	0	1	Write Data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
7 Read display data	1	1	Read Data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note 1) Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.

$$(1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK})$$

- Detailed Explanation

(1) Display ON/OFF

	R/W	D/I	DB7						DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order-bit　　low-order-bit →

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

(2) Display start line

	R/W	D/I	DB7						DB0
Code	0	0	1	1	A	A	A	A	A	A

← high-order-bit　　low-order-bit →

Z address AAAAAA (binary) of the display data RAM is set at the display start line register and displayed at the top of the screen.
Fig. 7 are the examples of display (1/64 duty) when the start line=0 ∿ 3.
When the display duty is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

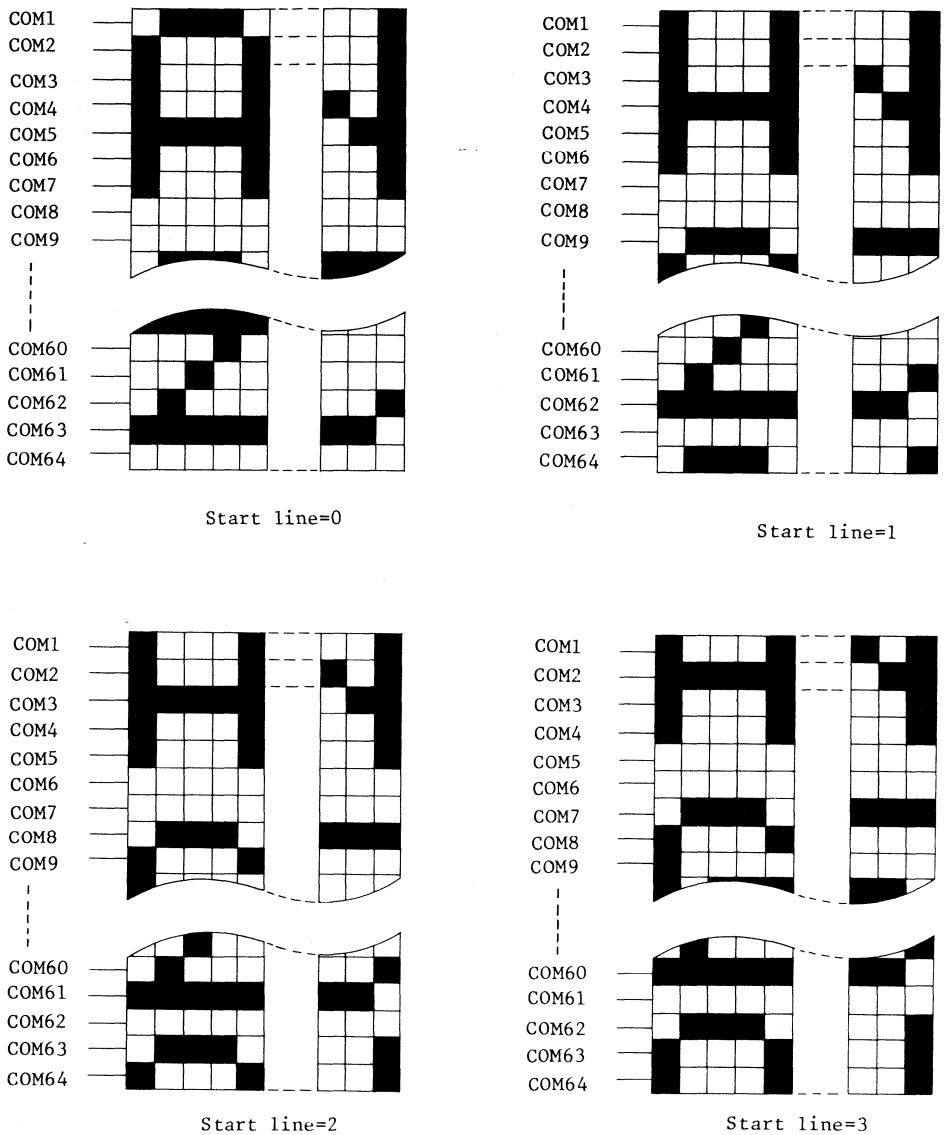


Fig. 7 Relation Between Start Line and Display

(3) Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order-bit low-order-bit →

X address AAA (binary) of the display data RAM is set at the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

(4) Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Y address AAAAAA (binary) of the display data RAM is set at the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

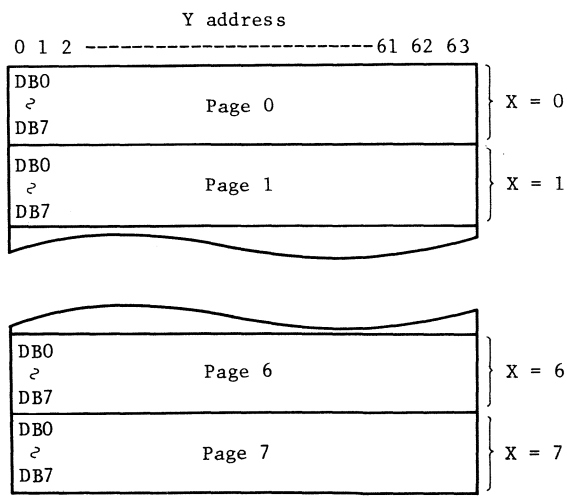
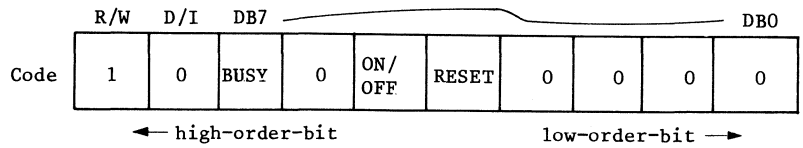


Fig. 8 Address Configuration of Display Data RAM

(5) Status Read

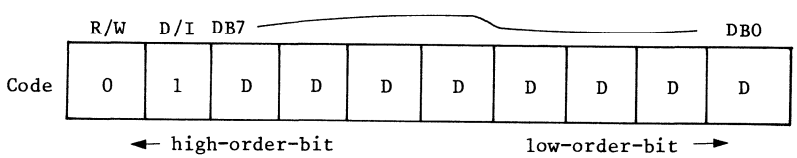


BUSY: When BUSY is 1, the LSI is in internal operation. No instructions are accepted while BUSY is 1, so you should make sure that BUSY is 0 before writing the next instruction.

ON/OFF: This bit shows the liquid crystal display conditions - ON condition or OFF condition.
When ON/OFF is 1, the display is in OFF condition.
When ON/OFF is 0, the display is in ON condition.

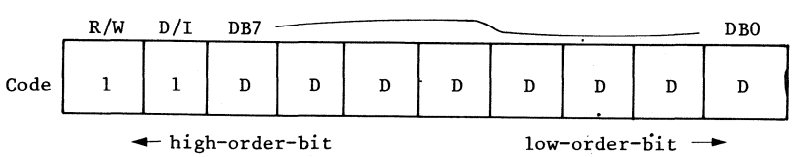
RESET: RESET=1 shows that the system is being initialized. In this condition, any instructions except Status Read instruction cannot be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation.

(6) Write Display Data



Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

(7) Read Display Data

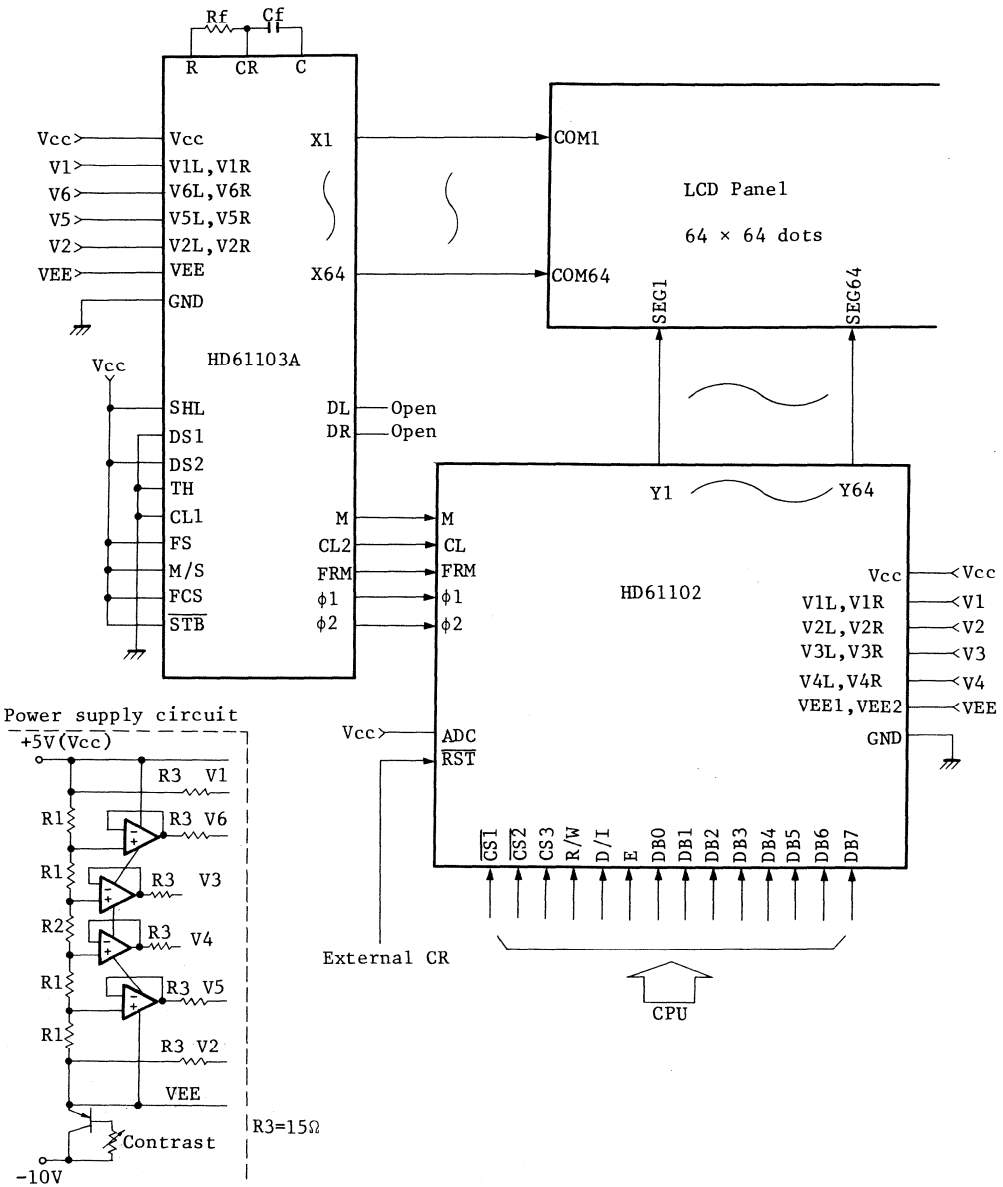


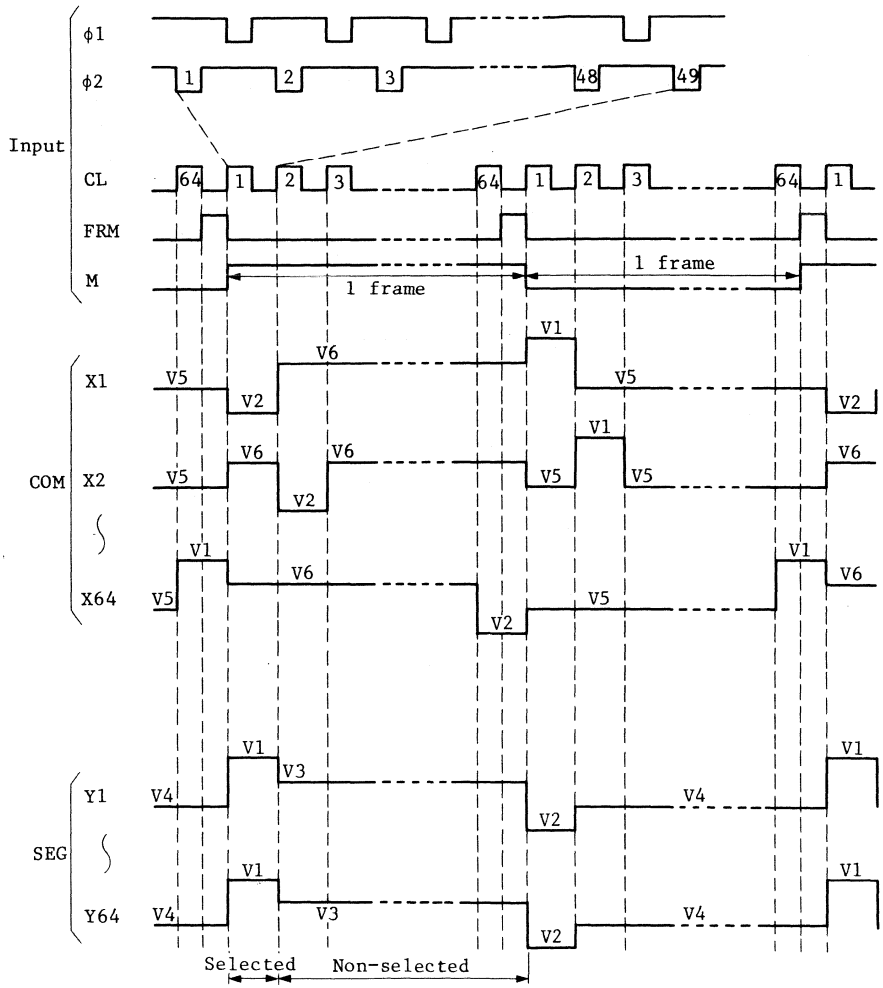
Read out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary soon after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

■ THE USAGE OF HD61102

- Interface with HD61103A (1/64 duty)



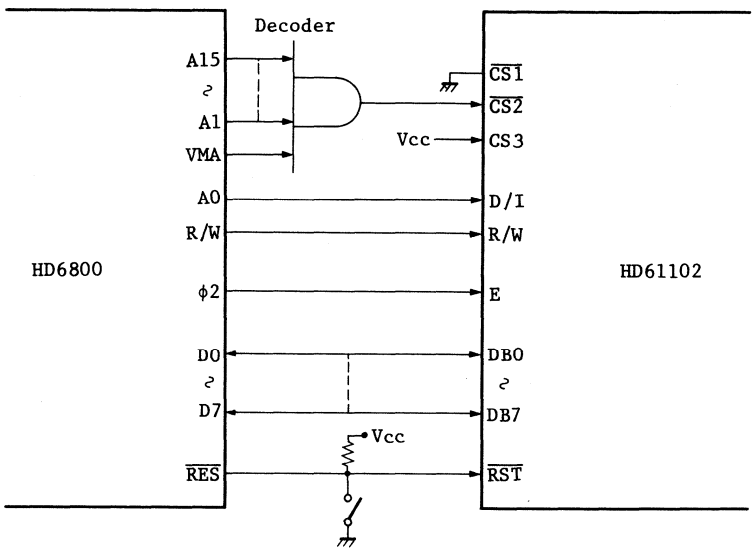


The wave forms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Fig. 9 LCD Driver Timing Chart (1/64 duty)

- Interface with CPU

a) Example of connection with HD6800



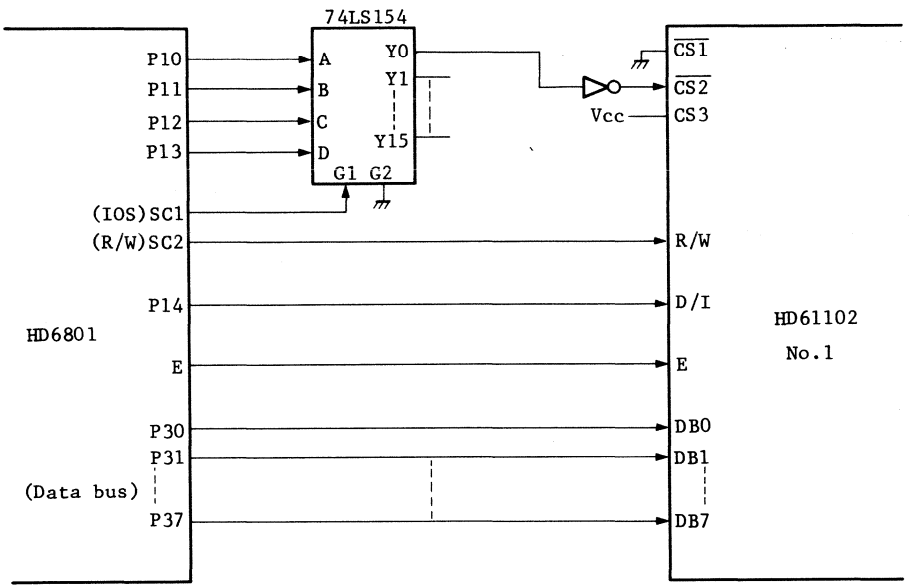
The example of connection with HD6800 series

In this decoder, addresses of HD61102 in the address area of HD6800 are:

Read/Write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

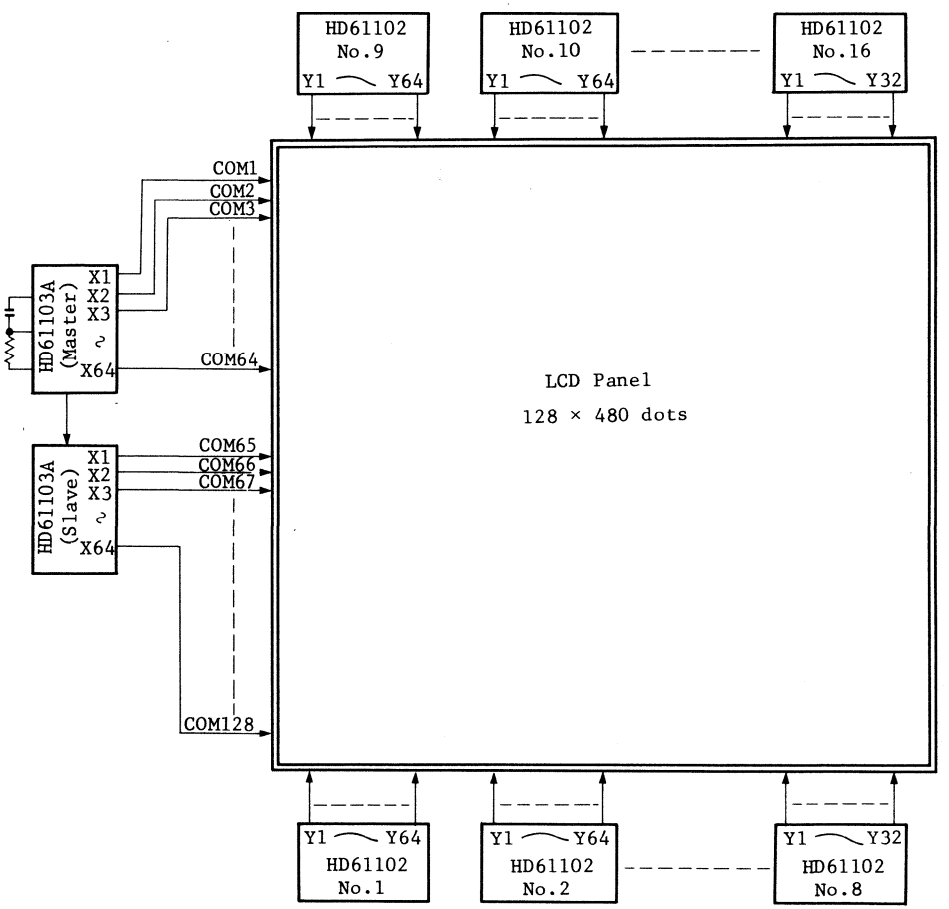
Therefore, you can control HD61102 by reading/writing the data at these addresses.

b) Example of connection with HD6801



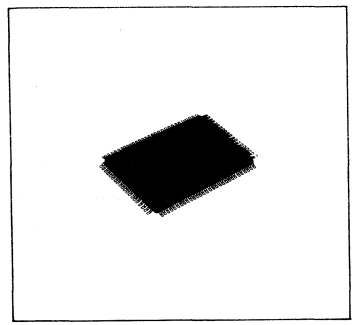
- Set HD6801 in Mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 is 4 to 16 decoder and genelate chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after making the operation possible by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61102. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to the each manual.

- Example of Application



Note) In this example, two HD61103A's output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, you had better drive in 2 rows as this example to guarantee the display quality.

HD61103A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)



The HD61103A is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

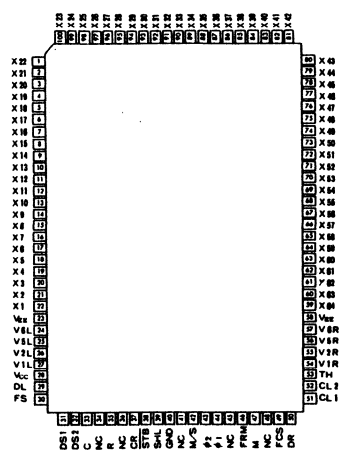
As the HD61103A is produced in a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61103A and the column (segment) driver HD61102.

■ FEATURES

- Dot matrix liquid crystal graphic display common driver with low impedance.
- Low impedance —1.5kΩ max.
- Internal liquid crystal display driver circuit —— 64 circuits
- Internal dynamic display timing generator circuit
- Selectable display duty ratio factor 1/48, 1/64, 1/96, 1/128.
- Can be used as a column driver transferring data serially.
- Low power dissipation

  —— during display 5mW

■ PIN ARRANGEMENT



(Top View)

- Power supplies : V_{CC} — +5V ± 10%
  V_{EE} — 0 ∿ -11.5V
- LCD drive level — 17.0V max
- CMOS process
- 100-pin flat plastic package (FP-100)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	2
Power Supply Voltage (2)	V_{EE}	V_{CC}-19.0 ∿ V_{CC} +0.3	V	5
Terminal Voltage (1)	V_{T1}	-0.3 ∿ V_{CC} +0.3	V	2, 3
Terminal Voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC} +0.3	V	4, 5
Operating Temperature	Topr	-20 ∿ +75	°C	
Storage Temperature	Tstg	-55 ∿ +125	°C	

Note 1) If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

Note 2) Based on GND=0V

Note 3) Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) and I/O common terminals at high impedance.

Note 4) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R.

Note 5) Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V_{5R}, V6L and V6R, V_{EE}(23 pin) and V_{EE}(58 pin) respectively.
Maintain $V_{CC} \geq V1L=V1R \geq V6L=V6R \geq V5L=V5R$
$\geq V2L=V2R \geq V_{EE}$

■ ELECTRICAL CHARACTERISTICS

- DC Characteristics (V_{CC}=+5V ± 10%, GND=0V, V_{EE}=0 ∿ -11.5V Ta= -20 ∿ +75°C)

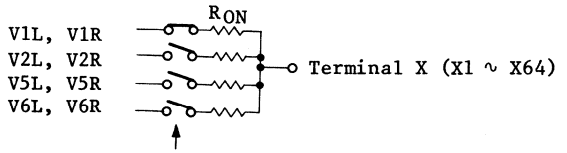
Test Item	Symbol	Test conditions	Specifications			Unit	Note
			Min	Typ	Max		
Input "High" voltage	V_{IH}		0.7×Vcc	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		GND	-	0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-0.4mA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=+0.4mA	-	-	+0.4	V	2
Vi-Xj ON resistance	R_{ON}	V_{CC}-V_{EE}=10V Load current ±150μA	-	-	1.5	KΩ	3
Input Leakage Current	I_{IL1}	Vin=0∿V_{CC}	-1.0	-	+1.0	μA	4
Input Leakage Current	I_{IL2}	Vin=V_{EE}∿V_{CC}	-2.0	-	+2.0	μA	5
Operating Frequency	f_{opr1}	In master mode External clock operation	50	-	600	kHz	6
Operating Frequency	fopr2	In slave mode Shift register	50	-	1500	kHz	7
Oscillation Frequency	fosc	Cf=20pF±5% Rf=47KΩ±2%	315	450	585	kHz	8,13
Dissipation Current (1)	I_{GG1}	In master mode 1/128 duty Cf=20pF Rf=47kΩ	-	-	1.0	mA	9,10
Dissipation Current (2)	I_{GG2}	In slave mode 1/128 duty	-	-	200	μA	9,11
Dissipation Current	I_{EE}	In master mode 1/128 duty	-	-	100	μA	9,12

Note 1) Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1 and TH and I/O common terminals DL, M, DR and CL2 in the input status.

Note 2) Applies to output terminals, φ1, φ2 and FRM and I/O common terminals DL, M, DR and CL2 in the output status.

Note 3) Resistance value between terminal X (one of X1 to X64) and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current is applied to each terminal X.

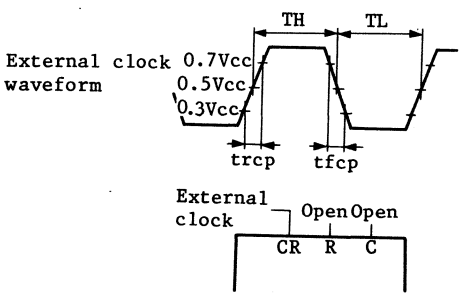
Equivalent circuit between terminal X and terminal V.



Note 4) Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1 and TH, I/O common terminals DL, M, DR and CL2 in the input status and NC terminals.

Note 5) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R.
Don't connect any lines to X1 to X64.

Note 6) External clock is as follows.

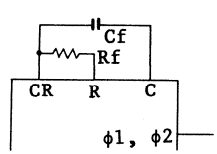


$$\text{Duty} = \frac{TH}{TH+TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty	45	50	55	%
trcp	-	-	50	ns
tfcp	-	-	50	ns

Note 7) Applies to the shift register in the slave mode. For details, refer to AC Characteristics.

Note 8) Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency ($f\phi$) at $\phi 1$ or $\phi 2$.



Cf=20pF
Rf=47kΩ fosc=2 × fφ

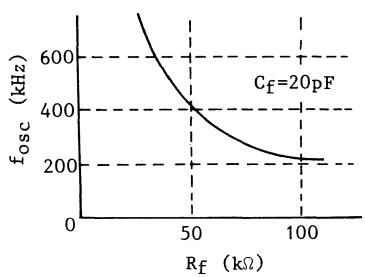
Note 9) No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH}=V_{CC}$ and $V_{IL}=GND$.

Note 10) This value is specified about current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$ and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in Note 8.

Note 11) This value is specified about current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH and M/S to GND and the terminals CL2, M and DL are respectively connected to terminals CL2, M and DL of the HD61103A under the condition described in Note 10.

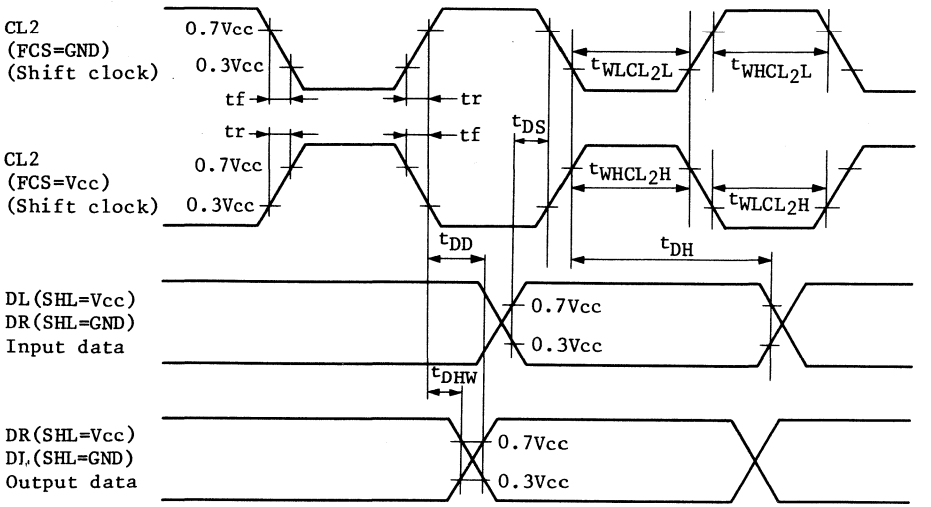
Note 12) This value is specified about current flowing through V_{EE} under the condition described in Note 10). Don't connect any lines to terminal V.

Note 13) This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting condition.



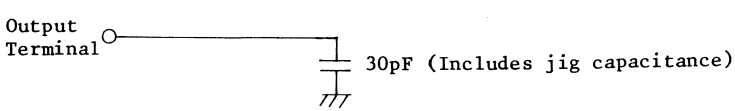
- AC Characteristics (V_{CC}=+5V±10% GND=0V, V_{EE}= 0 ∿ -11.5V Ta=-20 ∿ +75°C)

(1) In the slave mode (M/S=GND)



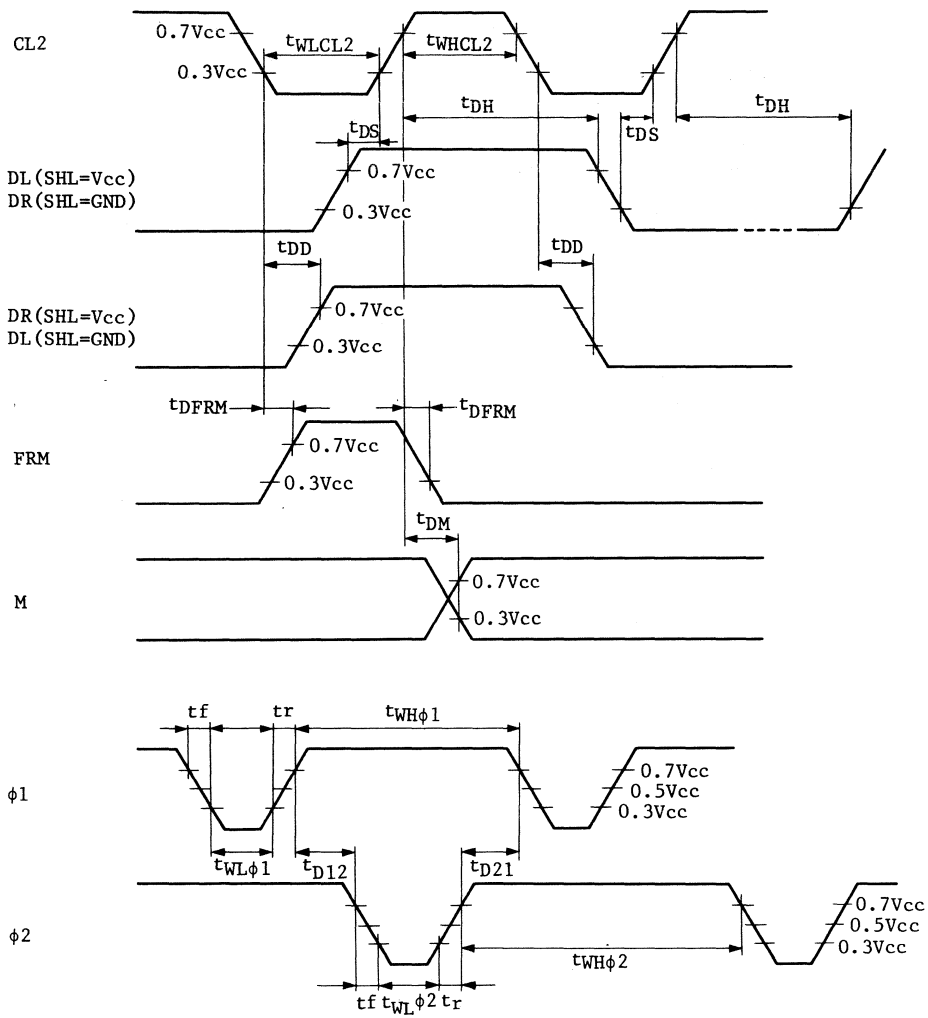
Item	Symbol	min.	typ.	max.	Unit	Note
CL2 "Low" level width (FCS=GND)	t_{WLCL2L}	450	-	-	ns	
CL2 "High" level width (FCS=GND)	t_{WHCL2L}	150	-	-	ns	
CL2 "Low" level width (FCS=V_{CC})	t_{WLCL2H}	150	-	-	ns	
CL2 "High" level width (FCS=V_{CC})	t_{WHCL2H}	450	-	-	ns	
Data setup time	t_{DS}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_{DD}	-	-	200	ns	1
Data hold time	t_{DHW}	10	-	-	ns	
CL2 rise time	tr	-	-	30	ns	
CL2 fall time	tf	-	-	30	ns	

Note 1) The following load circuit is connected for specification.



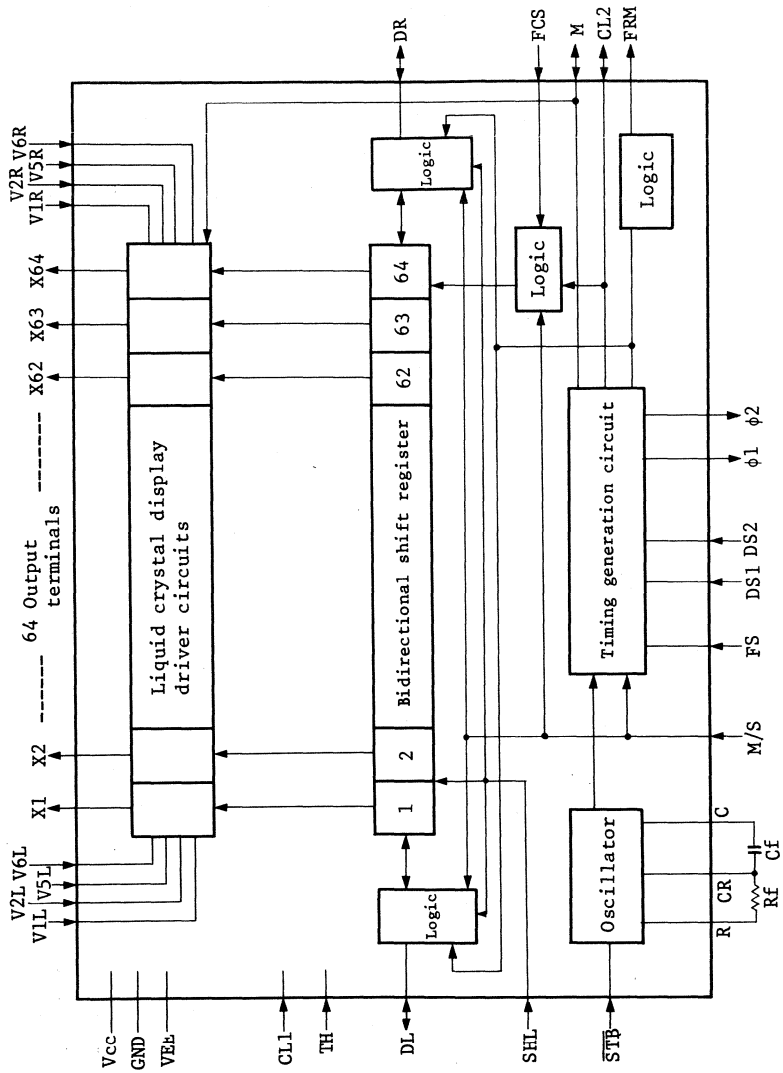
(2) In the master mode

($M/S=V_{CC}$, $FCS=V_{CC}$, Cf=20pF, Rf=47KΩ)



Item	Symbol	min	typ	max	Unit	Note
Data setup time	t_{DS}	20	-	-	µs	
Data hold time	t_{DH}	40	-	-	µs	
Data delay time	t_{DD}	5	-	-	µs	
FRM delay time	t_{DFRM}	-2	-	+2	µs	
M delay time	t_{DM}	-2	-	+2	µs	
CL_2 "Low" level width	t_{WLCL2}	35	-	-	µs	
CL_2 "High" level width	t_{WHCL2}	35	-	-	µs	
$\phi 1$ "Low" level width	$t_{WL\phi 1}$	700	-	-	ns	
$\phi 2$ "Low" level width	$t_{WL\phi 2}$	700	-	-	ns	
$\phi 1$ "High" level width	$t_{WH\phi 1}$	2100	-	-	ns	
$\phi 2$ "High" level width	$t_{WH\phi 2}$	2100	-	-	ns	
$\phi 1$-$\phi 2$ phase difference	t_{D12}	700	-	-	ns	
$\phi 2$-$\phi 1$ phase difference	t_{D21}	700	-	-	ns	
$\phi 1$, $\phi 2$ rise time	tr	-	-	150	ns	
$\phi 1$, $\phi 2$ fall time	tf	-	-	150	ns	

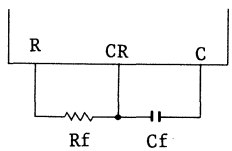
■ BLOCK DIAGRAM

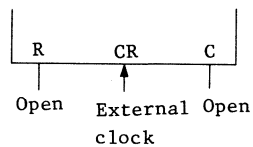


Block Functions

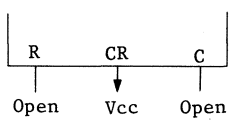
- Oscillator

The oscillator is a CR oscillator that generates display timing signals and operating clocks for the HD61102. It is required when the HD61103A is used with the HD61102. It attaches an oscillation resistor Rf and an oscillation capacity Cf as shown in the following figure and terminal $\overline{STB}$ is connected to "high" level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminal R and C.





Oscillator is not required when the HD61103A is used with the HD61830. Then, connect terminal CR to "high" level and don't connect any lines to terminals R and C.



- Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61102. This circuit is required when the HD61103A is used with the HD61102. Then connect terminal M/S to "high" level. (master mode).
It is not necessary when display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals FS, DS1 and DS2 to "high" level and M/S to "low" level. (Slave mode)

- Bidirectional Shift Register

This is a 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the side of DL, corresponds to X1 and the highest order bit on the side of DR corresponds to X64.

- Liquid Crystal Display Driver Circuit

  The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

Data from the shift register	M	Output level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

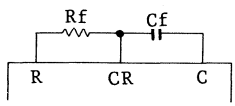
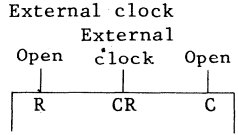
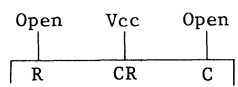
■ HD61103A TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Connected to	Function
VCC GND VEE	1 1 2		Power supply	V_{CC}-GND: Power supply for internal logic. V_{CC}-V_{EE}: Power supply for driver circuit logic.
V1L,V2L, V5L,V6L, V1R,V2R, V5R,V6R	8		Power supply	Liquid crystal display driver level power supply. V1L(V1R), V2L(V2R): Selected level V5L(V5R), V6L(V6R): Non-selected level voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects Master/Slave M/S=V_{CC}: In master mode When the HD61103A is used with the HD61102, timing generation circuit operates to supply display timing signals and operation clock to the HD61102. Each of I/O common terminals DL, DR, CL2 and M is in the output state. M/S=GND: In slave mode The timing operation circuit stops operating. The HD61103A is used in this mode when combined with the HD61830. Even if combined with the HD61102, this mode is used when display timing signals (M, data, CL2 etc.) are supplied by another HD61103A in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.

- to be continued

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift clock phase
FCS=V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61103A is used with HD61102 or when MA of the HD61830 connects to CL2 in the combination with the HD61830.
FCS=GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in the combination with the HD61830.</td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects frequency
When the frame frequency is 70Hz, the oscillation frequency should be:
fosc=430kHz at FCS=V_{CC}
fosc=215kHz at FCS=GND
This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.</td></tr>
<tr><td>DS1,DS2</td><td>2</td><td>I</td><td>V_{CC} or GND</td><td>Selects display duty factor
<table><tr><td>Display Duty</td><td>1/48</td><td>1/64</td><td>1/96</td><td>1/128</td></tr><tr><td>DS1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr><tr><td>DS2</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr></table>This terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.</td></tr>
<tr><td>$\overline{STB}$
TH
CL1</td><td>1
1
1</td><td>I</td><td>V_{CC} or GND</td><td>Input terminal for testing
Connect $\overline{STB}$ to V_{CC}.
Connect TH and CL1 to GND.</td></tr>
<tr><td>CR,R,C</td><td>3</td><td></td><td></td><td>Oscillator.
In the master mode, use these terminals as shown below.</td></tr>
</table>

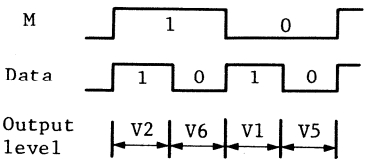
- to be continued

Terminal name	Number of terminals	I/O	Connected to	Function
CR,R,C	3			Usage of these terminal in the master mode Internal oscillation  External clock  In the slave mode, stop the oscillator as shown below. 
ϕ1, ϕ2	2	O	HD61102	Operating clock output terminals for the HD61102. Master mode: Connect these terminals to terminals ϕ1 and ϕ2 of the HD61102 respectively. Slave mode : Don't connect any lines to these terminals.
FRM	1	O	HD61102	Frame signal Master mode: Connect this terminal to terminals FRM of the HD61102. Slave mode : Don't connect any lines to this terminal.
M	1	I/O	MB of HD61830 or M of HD61102	Signal to convert LCD driver signal into AC. Master mode: Output terminal. Connect this terminal to terminal M of the HD61102. Slave mode : Input terminal. Connect this terminal to terminal MB of the HD61830.
CL2	1	I/O	CL1 or MA of HD61830 or CL of HD61102	Shift clock Master mode: Output terminal Connect this terminal to terminal CL of the HD61102.

- to be continued

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830
or
CL of HD61102</td><td>Slave mode : Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register.
DL corresponds to X1's side and DR to X64's side.
Master mode : Output common scanning signal.
Don't connect any lines to these terminals normally.
Slave mode : Connect terminal FLM of the HD61830 to DL (when SHL=V_{CC}) or DR (when SHL=GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don't connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><td>SHL</td><td>Shift direction</td><td>Common scanning direction</td></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
<tr><td>X1∿X64</td><td>64</td><td>O</td><td>Liquid crystal display</td><td>Liquid crystal display driver output.
Output one of the four liquid crystal display driver levels V1, V2, V5 and V6 with the combination of the data from the shift register and M signal.</td></tr>
</table>

- to be continued

Terminal name	Number of terminals	I/O	Connected to	Functions
X1~X64	64	O	Liquid crystal display	 Data "1" — Selected level "0" — Non-selected level When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

■ EXAMPLE OF APPLICATION

HD61103A Connection List

H...V_{CC} } Fixed
L...GND }

"-" meanse "open".

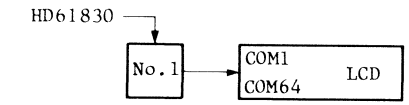
Rf...Oscillation resistor
Cf...Oscillation capacity

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	ϕ1	ϕ2	FRM	M	CL2	SHL	DL	DR	X1 ∿ X64
A	L	L	L	L	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	-	COM1 ∿COM64
																	L	-	from FLM of HD61830	COM64 ∿COM1
B	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61103A No.2	COM1 ∿COM64
																	L	to DL/DR of HD61103A No.2	from FLM of HD61830	COM64 ∿COM1
C	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61103A No.1	-	COM65 ∿COM128
																	L	-	from DL/DR of HD61103A No.1	COM128∿COM65
D	H	L	L	H	H	L or L H	L	H	Rf Cf	Rf	Cf	to ϕ1 of HD61102	to ϕ2 of HD61102	to FRM of HD61102	to M of HD61102	to CL of HD61102	H	-	-	COM1 ∿COM64
																	L	-	-	COM64 ∿COM1
E	H	L	L	H	H	L or L H	L	H	Rf Cf	Rf	Cf	to ϕ1 of HD61102	to ϕ2 of HD61102	to FRM of HD61102	to M of HD61102 HD61103A	to CL of HD61102 to CL2 of HD61103A	H	-	to DL/DR of HD61103A No.2	COM1 ∿COM64
																	L	to DL/DR of HD61103A No.2	-	COM64 ∿COM1
F	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from M of HD61103A No.1	from CL2 of HD61103A No.1	H	from DL/DR of HD61103A No.1	-	COM1 ∿COM64
																	L	-	from DL/DR of HD61103A No.1	COM64 ∿COM1

Outline of HD61103A System Configuration

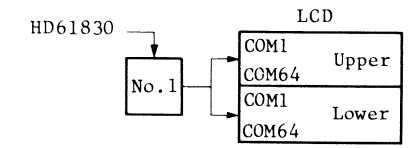
1) Use with HD61830

a) When display duty ratio of LCD is more than 1/64



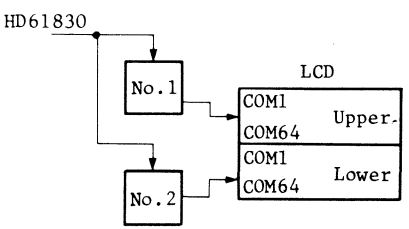
One HD61103A drives common signals.

Refer to Connection list 'A'



One HD61103A drives common signals for upper and lower panels.

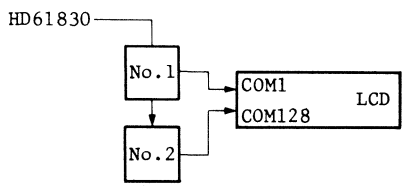
Refer to Connection list 'A'



Two HD61103A's drive upper and lower panel separately to ensure the quality of display. No.1 and No.2 operate in parallel.

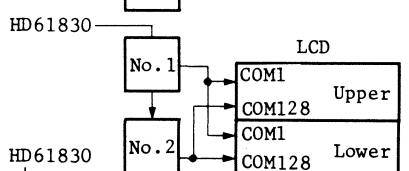
For both of No.1 and No.2, refer to Connection list 'A'

b) When display duty ratio of LCD is from 1/65 to 1/128



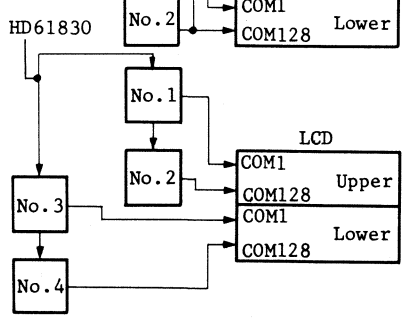
Two HD61103A's connected serially drive common signals.

Refer to Connection list 'B' for No.1.
Refer to Connection list 'C' for No.2.



Two HD61103A's connected serially drive upper and lower panels in parallel.

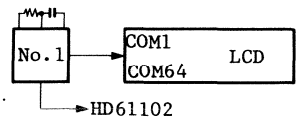
Refer to Connection list 'B' for No.1.
Refer to Connection list 'C' for No.2.



Two sets of HD61103A's connected serially drive upper and lower panels in parallel to ensure the quality of display.

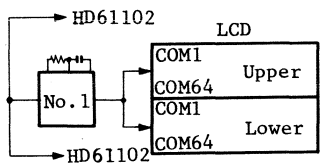
Refer to Connection list 'B' for No.1 and 3.
Refer to Connection list 'C' for No.2 and 4.

2) Use with HD61102 (1/64 duty)



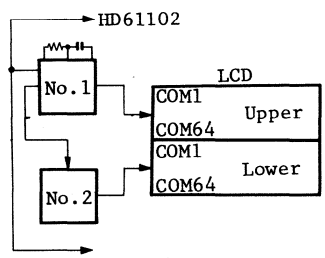
One HD61103A drives common signals and supplies timing signals to the HD61102's.

Refer to Connection list 'D'



One HD61103A drives upper and lower panels and supplies timing signals to the HD61102's.

Refer to Connection list 'D'



Two HD61103A's drive upper and lower panels in parallel to ensure the quality of display. No.1 supplies timing signals to No.2 and the HD61102's.

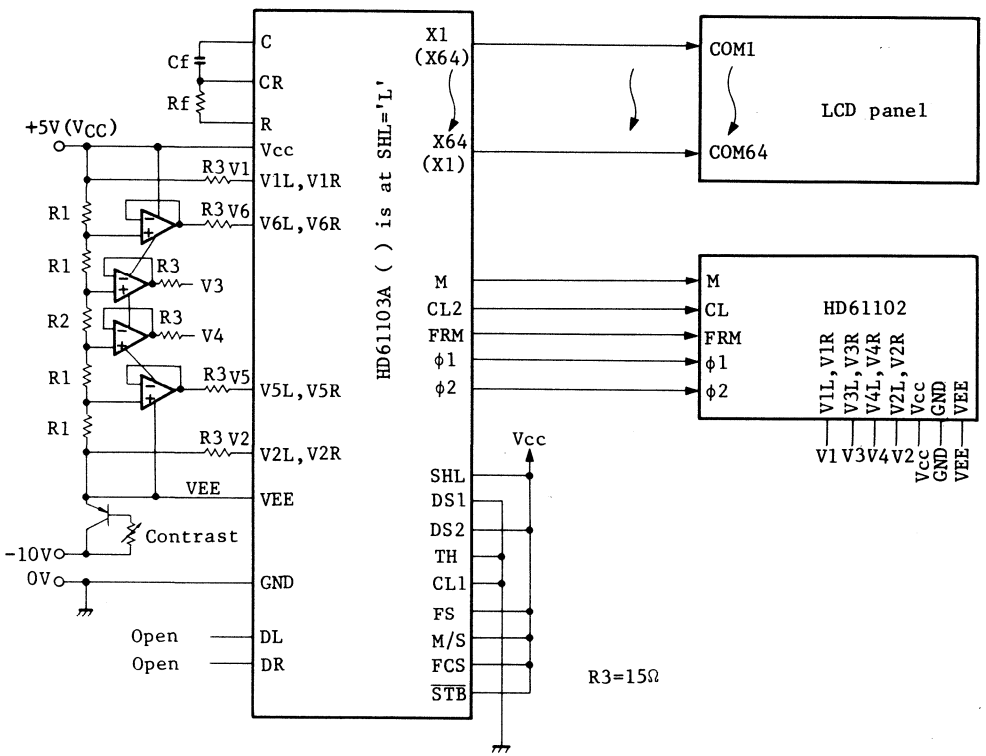
Refer to Connection list 'E' for No.1

Refer to Connection list 'F' for No.2

- Example of Connection 1)

  ° Use with HD61102 (RAM type segment driver)

  a) 1/64 duty ratio (See Connection List "D")



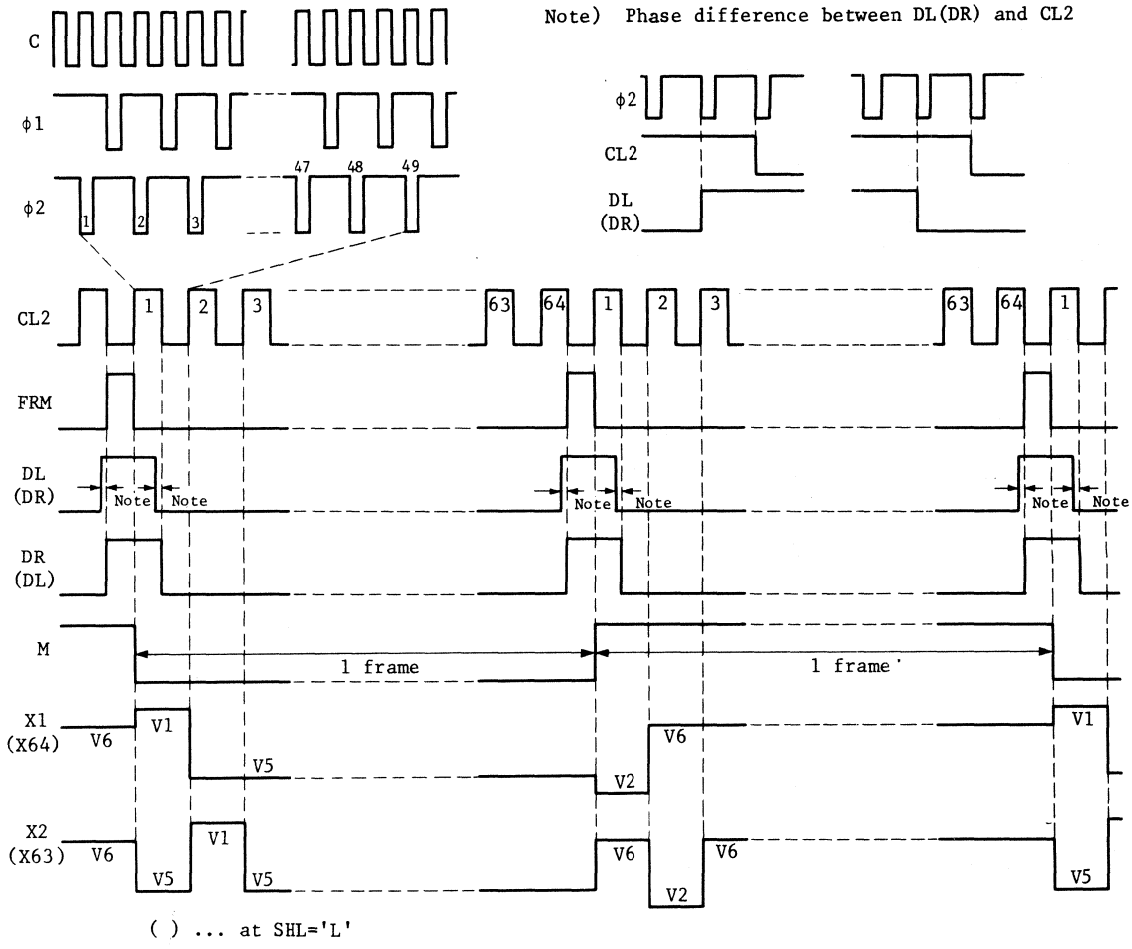
Note 1) The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1=3kΩ, R2=15kΩ

Example of Waveform (RAM type, 1/64 duty)



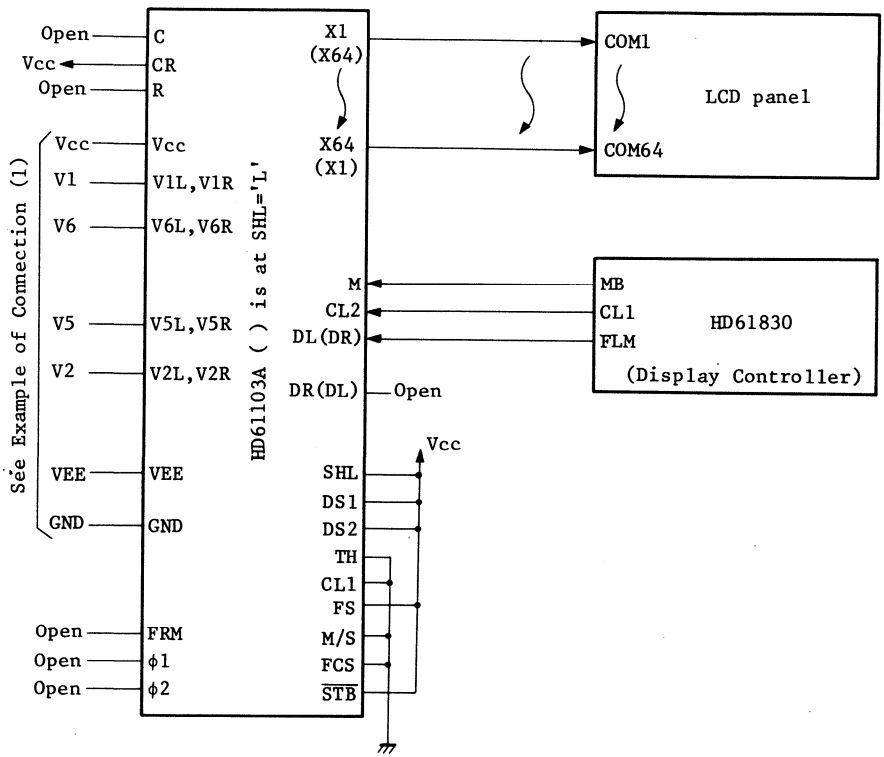
Note) Phase difference between DL(DR) and CL2

( ) ... at SHL='L'

Example of Connection 2)

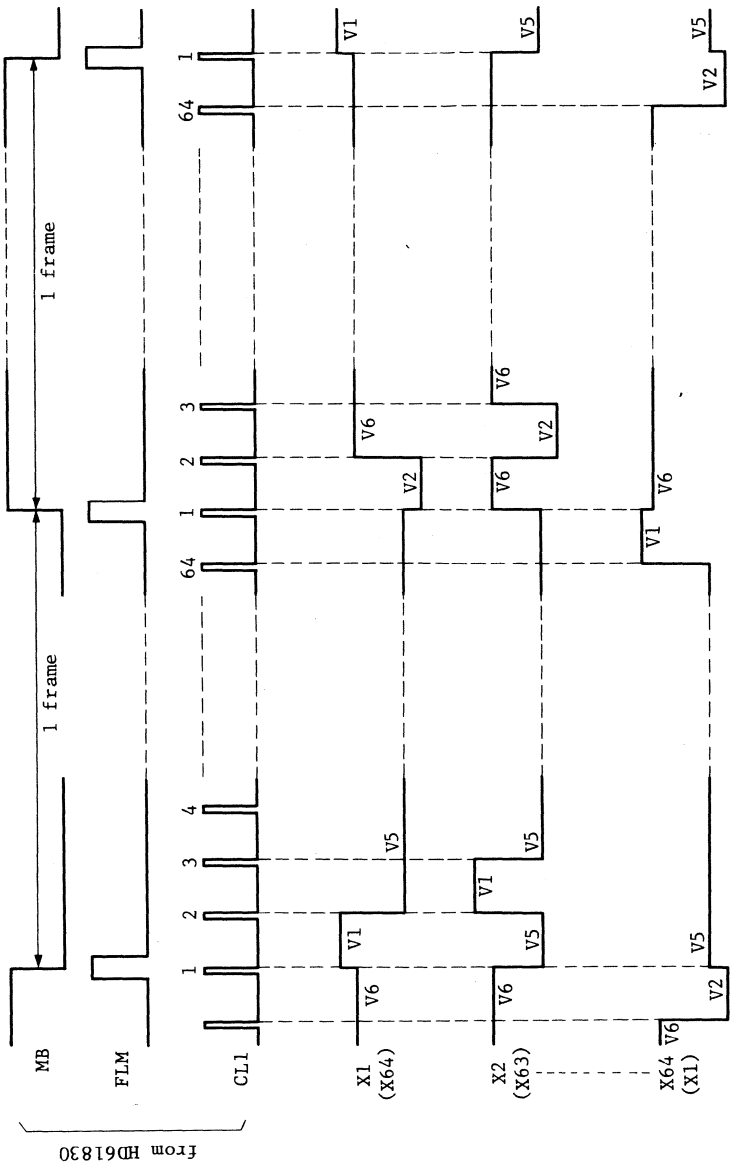
- Use with HD61830 (Display controller)

a) 1/64 duty ratio (See Connection List "A")

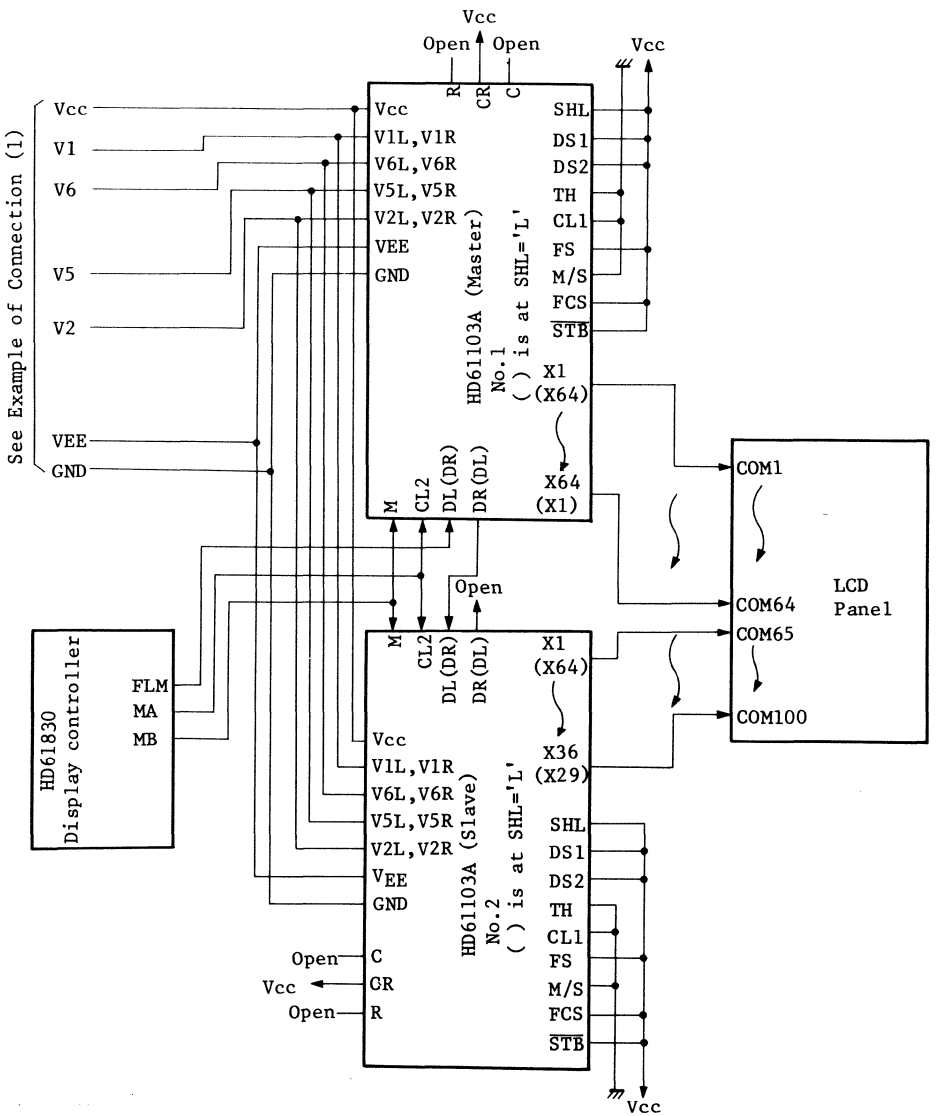


Example of Waveform

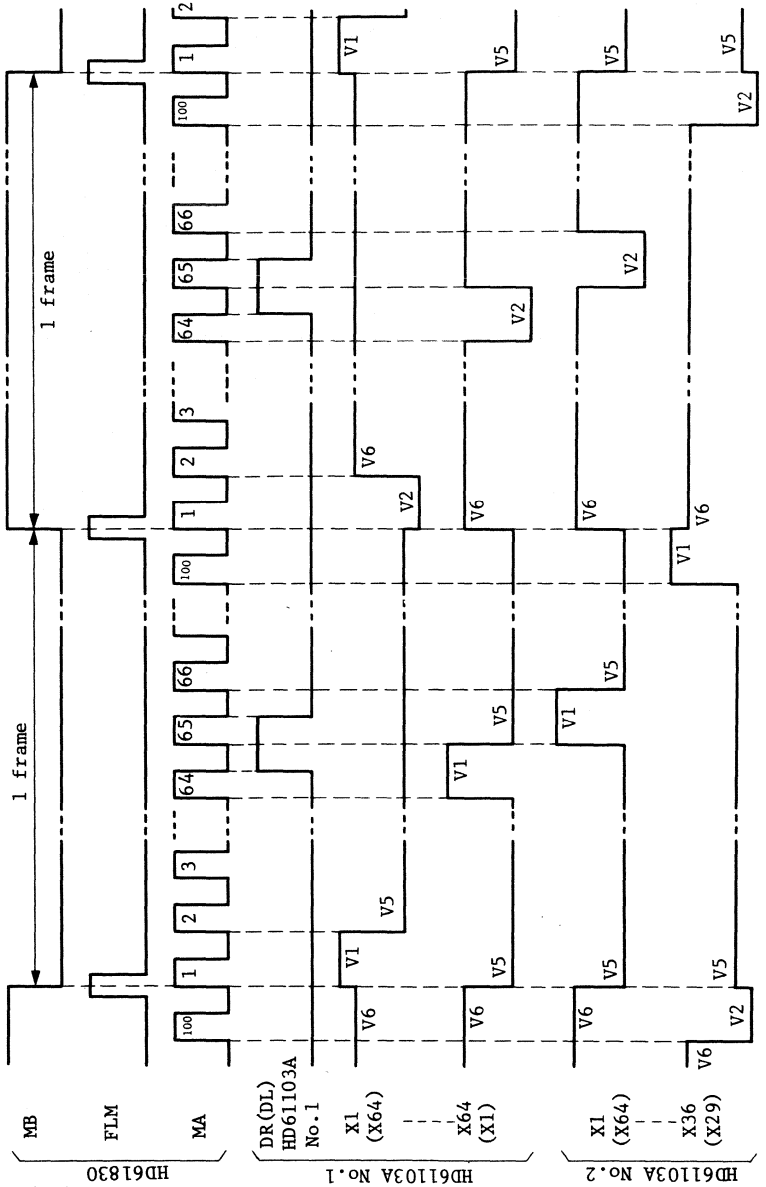
a) 1/64 duty ratio



b) 1/100 duty ratio (See Connection List 'B' 'C')



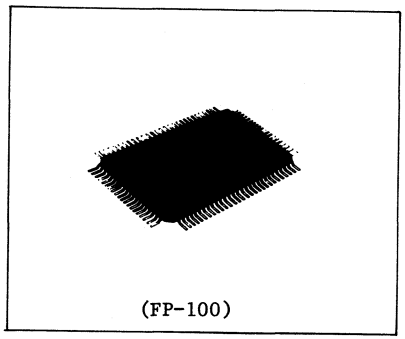
Example of Waveform b) 1/100 duty



( ): Case of SHL=Low level.

HD61200
(LCD Driver with 80-Channel Output)

The HD61200 is a colume driver LSI for a large-area dot matrix LCD. This employs 1/32 or more duty multiplexing method. It receives serial display data from a microcomputer or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

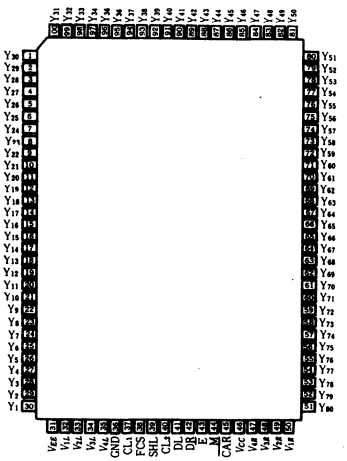


(FP-100)

FEATURES

- Liquid crystal display driver with serial/parallel conversion function.
- Internal liquid crystal display driver ..... 80 drivers
- Driyes liquid crystal panels with 1/32 - 1/128 duty multiplexing.
- Capable of interfacing to LCD controllers, HD61830 and HD61830B.
- Data transfer rate .... 2.5 MHz max
- Power supply
  Vcc - 5V±10% (Internal logic)
- Power supply voltage for liquid crystal display drive ... 8V ∿ 17V
- CMOS process
- 100-pin flat plastic package (FP-100)

PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{cc}-19.0 to V_{cc}+0.3	V	
Terminal voltage (1)	V_{T1}	-0.3 to V_{cc} +0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE}-0.3 to V_{cc}+0.3	V	4
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, $\overline{E}$ and M.

(Note 4) Applies to V_{1L}, V_{1R} V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain

$$V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}.$$

Connect a protection resistor of 47Ω±10% to each terminals in series.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(Vcc=5V±10%, GND=0V, Vcc-VEE=8V∿17V Ta=-20∿75°C)

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Input "High" voltage	V_{IH}		0.7×V_{CC}	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		0	-	0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=400μA	-	-	0.4	V	2
Driver ON Resistance	R_{ON}	Load current= 100μA	-	-	7.5	kΩ	5
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1	-	1	μA	1
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-2	-	2	μA	3
Dissipation Current(1)	I_{GND}		-	-	1.0	mA	4
Dissipation Current(2)	I_{EE}		-	-	0.1	mA	4

(Note 1) Applies to CL1, CL2, SHL, $\overline{E}$, M, DL and DR.

(Note 2) Applies to $\overline{CAR}$.

(Note 3) Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}.

(Note 4) Specified when display data is transfered under following conditions.

CL2 frequency f_{CP2} = 2.5MHz (data transfer rate)

CL1 frequency f_{CP1} = 4.48kHz (data latch frequency)

M frequency f_M = 35Hz (frame frequency/2)

Specified at V_{IH}=V_{CC} (V), V_{IL}=0V and no load on outputs.

I_{GND} : currents between V_{CC} and GND.

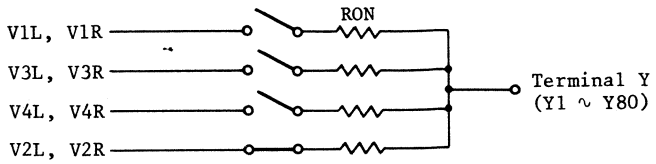
I_{EE} : currents between V_{CC} and V_{EE}.

(Note 5) Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition.

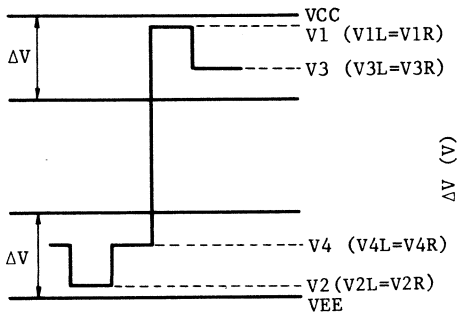
VCC - VEE = 17 V

V1L=V1R, V3L=V3R = VCC-2/7(VCC-VEE)

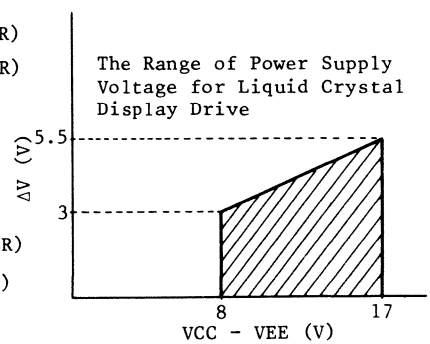
V2L=V2R, V4L=V4R = VEE+2/7(VCC-VEE)



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice the ΔV depends on power supply voltage VCC-VEE.



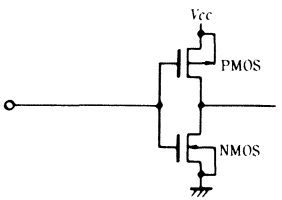
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage VCC-VEE and ΔV

TERMINAL CONFIGURATION

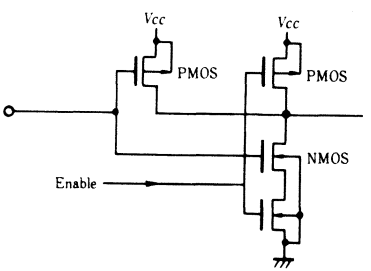
- Input Terminal

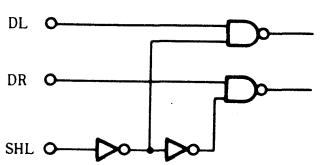


Applicable terminals :
CL1, CL2, SHL, $\overline{E}$, M

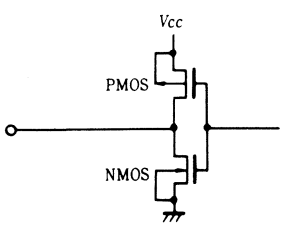
- Input Terminal (with Enable)

Applicable terminal: DL DR





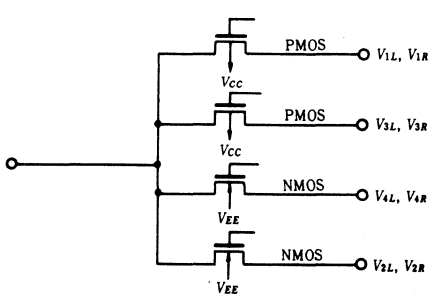
- Output Terminal



Applicable terminal : $\overline{CAR}$

- Output Terminal

Applicable terminals:
Y1 ∿ Y80

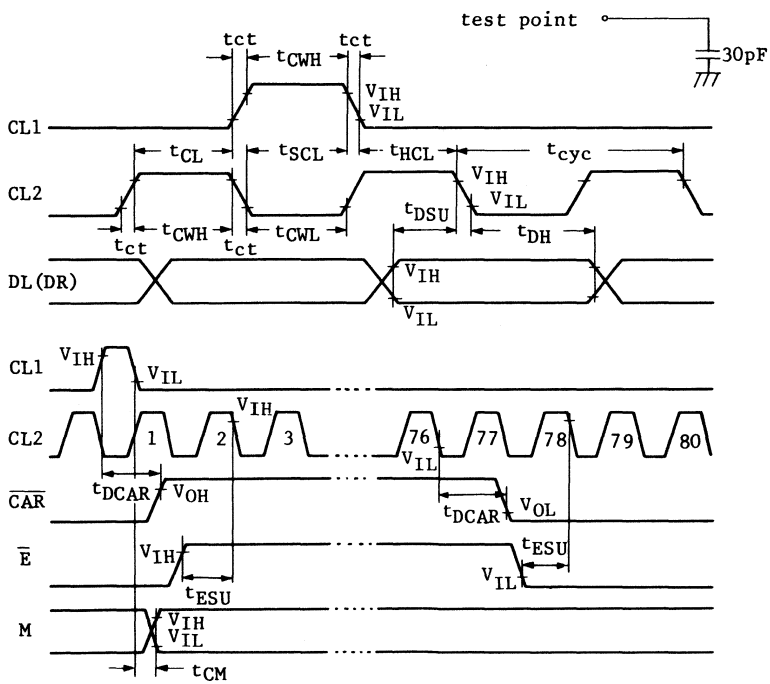


- AC CHARACTERISTICS

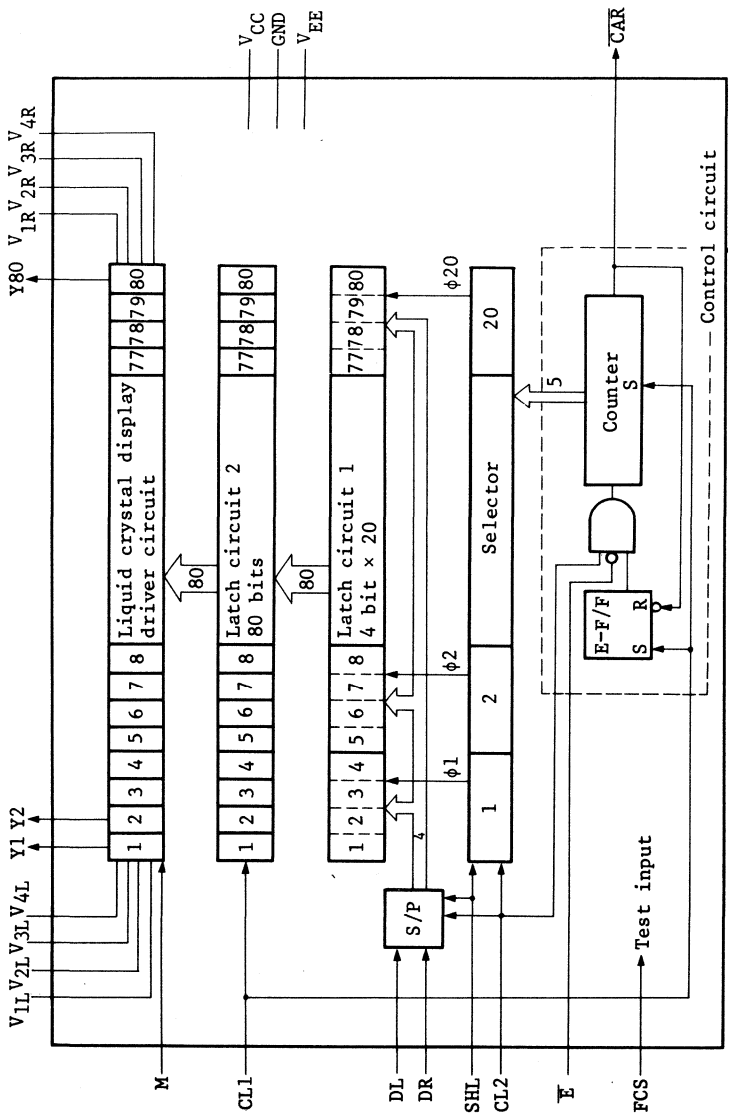
  (Vcc=5V±10%, GND=0V, Ta=-20∿+75°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Clock cycle time	t_{CYC}		400	-	-	ns	
Clock high level width	t_{CWH}		150	-	-	ns	
Clock low level width	t_{CWL}		150	-	-	ns	
Clock setup time	t_{SCL}		100	-	-	ns	
Clock hold time	t_{HCL}		100	-	-	ns	
Clock rise/fall time	t_{Ct}		-	-	30	ns	
Clock phase different time	t_{CL}		100	-	-	ns	
Data setup time	t_{DSU}		80	-	-	ns	
Data hold time	t_{DH}		100	-	-	ns	
E setup time	t_{ESU}		200	-	-	ns	
Output delay time	t_{DCAR}		-	-	300	ns	1
M phase difference time	t_{CM}		-	-	300	ns	

(Note 1) The following load circuits are connected for specification:



■ BLOCK DIAGRAM



BLOCK FUNCTION

- Liquid Crystal Display Driver Circuit

  The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

- 80-bit Latch Circuit 2

  The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

- S/P

  Serial/Parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is "L" level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR.

  When SHL is "H" level, input data from terminal DR without connecting any lines to terminal DL.

- 80-bit Latch Circuit 1

  The 4-bit data is latched at $\phi 1 \sim \phi 20$ and output to latch circuit 2. When SHL is "L" level, the data from DL are latched one in order of 1→2→3 ... →80 of each latch. When SHL is "H" level, they are latched in a reverse order (80→79→78 ... →1).

- Selector

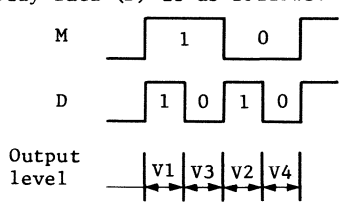
  The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1 \sim \phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

- Control Circuit

  Controls operation : When E-F/F (enable F/F) indicates "1", S/P conversion is started by inputting "L" level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into "L" level and E-F/F is reset to "0", and consequently the conversion stops. E-F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at "H" level of CL1.

  Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into "H" level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61200.

TERMINAL FUNCTIONS DESCRIPTION

Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC}-GND : Power supply for internal logic V_{CC}-V_{EE} : Power supply for LCD drive circuit
V_{1L}∿V_{4L} V_{1R}∿V_{4R}	8		Power supply	Power supply for liquid crystal drive V_{1L} (V_{1R}), V_{2L} (V_{2R})...selection level V_{3L} (V_{3R}), V_{4L} (V_{4R})...non-selection level Power supplies connected with V_{1L} and V_{1R}(V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1∿Y80	80	O	LCD	Liquid crystal driver outputs Selects one of the 4 levels, V1, V2, V3 and V4. Relation among output level, M and display data (D) is as follows. 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Synchronous Signal (a counter is reset at "High" level) Latch clock of display data (fall edge trigger). Synchronizing with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D) Fall edge trigger

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>DL, DR</td><td>2</td><td>I</td><td>Controller</td><td>Input of serial display data (D)
<table>
<tr><th>(D)</th><th>Liquid crystal driver output</th><th>Liquid crystal display</th></tr>
<tr><td>1 (H level)</td><td>selection level</td><td>ON</td></tr>
<tr><td>0 (L level)</td><td>non-selection level</td><td>OFF</td></tr>
</table></td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of serial data.
When the serial data (D) is input in order of D1→ ... →D80, the relations between the data (D) and output Y are as follows.
<table>
<tr><td>SHL</td><td>Y1</td><td>Y2</td><td>Y3</td><td>....</td><td>Y80</td></tr>
<tr><td>"L"</td><td>D1</td><td>D2</td><td>D3</td><td>....</td><td>D80</td></tr>
<tr><td>"H"</td><td>D80</td><td>D79</td><td>D78</td><td>....</td><td>D1</td></tr>
</table>
When SHL is "L", data is input from the terminal DL. Any lines should not be connected to the terminal DR.
When SHL is "H", the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61200</td><td>Controls the S/P conversion.
The operation stops with "H" level, and the S/P conversion starts with "L" level.</td></tr>
</table>

Terminal name	Number of terminals	I/O	Connected to	Functions
$\overline{CAR}$	1	O	the input terminal $\overline{E}$ of the HD61200	Used for cascade connection with the HD61200 to increase the number of bit which can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

THE OPERATION OF THE HD61200

The following is the LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty dynamic drive. Fig. 1 is an example of liquid crystal display and connection to HD61200 's. Fig. 2 shows a time chart of I/O signals of HD61200

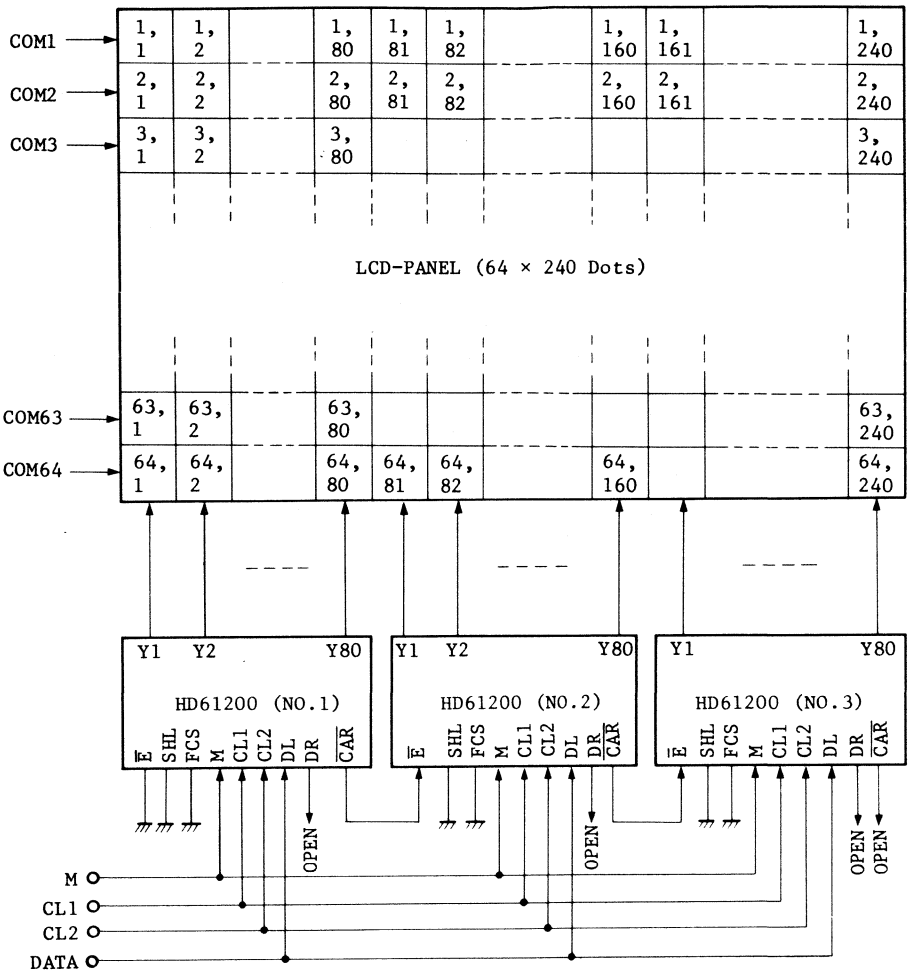
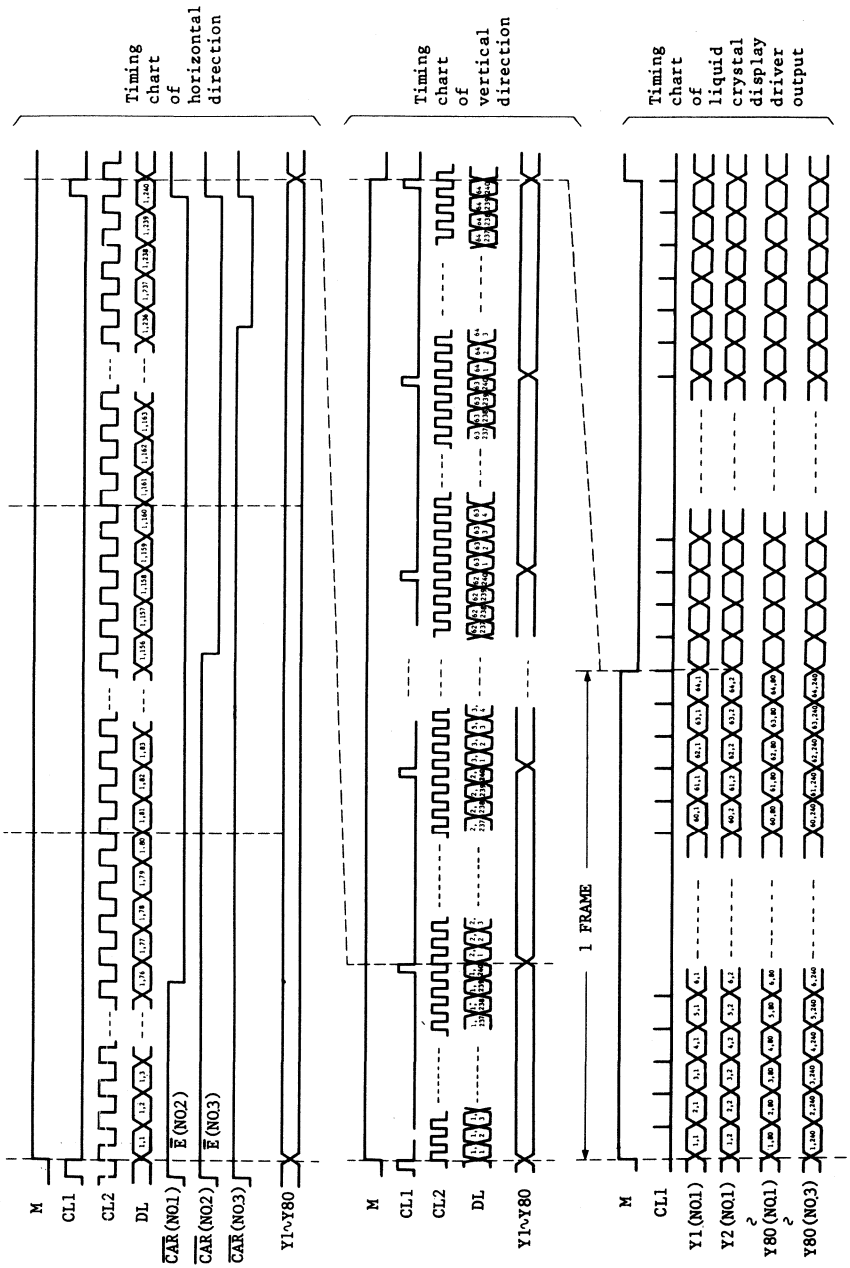


Fig. 1 LCD driver with 64 × 240 dots

Cascade three HD61200 s. Input data to the terminal DL of NO.1, NO.2 and NO.3. Connect $\overline{E}$ of NO.1 to GND. Don't connect any lines to $\overline{CAR}$ of NO.3. Connect common signal terminals (COM1 ∿ COM64) to X1 ∿ X64 of common driver HD61203. (m,n) of LCD panel is the address corresponding to each dot.

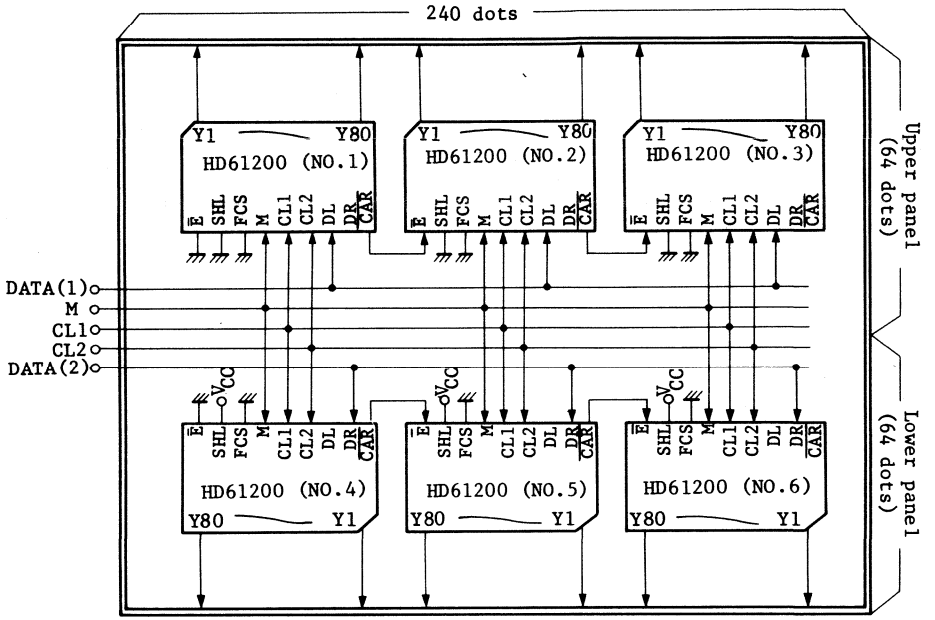


Timing chart in the example of connection of Fig.1. DL input (m,n) is the data which corresponds to each address (m,n) of LCD panel.

Fig. 2 HD61200 Timing Chart

■ EXAMPLE OF APPLICATION

- An example of 128 × 240 dot liquid crystal display (1/64 duty)



Liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61200s of No.1 ∿ No.3 drive upper half. Serial data, which are input from DATA (1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} terminal of No.1, then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No.2 and then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No.3 in order where they were input. (in the case of SHL=L). HD61200s of No.4 ∿ No.6 drive lower half. Serial data, which are input from DATA (2) terminal, appear at $Y_{80} \rightarrow T_{79} \rightarrow$ -- Y_1 of No.4, then at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.5 and then $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.6 in order where they were input (in the case of SHL=H).

As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

HD61202
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

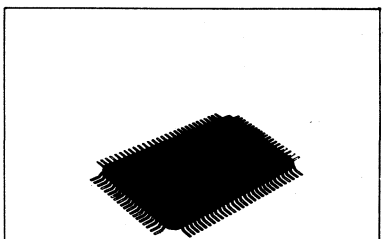
HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit microcomputer in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

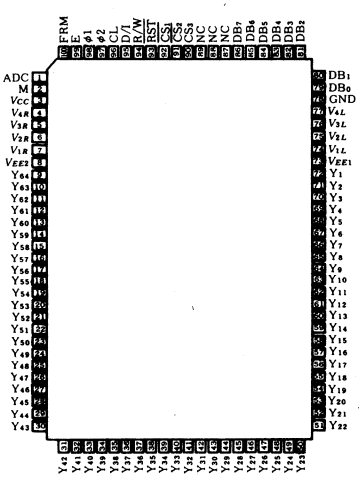
The HD61202 which is produced in the CMOS process, can accomplish a portable battery drive equipment by combining a CMOS micro-computer, utilizing the liquid crystal display's lower power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration by combining the row (common) driver HD61203.



(FP-100)

PIN ARRANGEMENT



(Top View)

FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- RAM data direct display by internal display RAM
  RAM bit data "1" ..... ON
  RAM bit data "0" ..... OFF
- Internal display RAM address counter preset, increment
- Display RAM capacity ..... 512 bytes (4096 bits)

- 8-bit parallel interface
- Internal liquid crystal display driver circuit 64
- Display duty
  Drives liquid crystal panels with 1/32 ∿ 1/64 duty multiplexing.
- Wide range of instruction function
  Display Data Read/Write, Display ON/OFF, Set address, Set Display Start line, Read Status
- Lower power dissipation.....during display 2mW max
- Power supply Vcc_____5V ± 10%
- Liquid crystal display driving voltage___8V ∿ 17.0V
- CMOS process
- 100 - pin flat plastic package (FP-100)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} -19.0 ∿ V_{CC} +0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} -0.3 ∿ V_{CC} +0.3	V	4
Terminal voltage (2)	V_{T2}	-0.3 ∿ V_{CC} +0.3	V	2, 5
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) LSI's may be destroyed for ever, if being used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them observing the recommended operation conditions.
Using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Apply the same supply voltage to V_{EE} 1 and V_{EE2}.

(Note 4) Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R and V4R.
Maintain
Vcc≧V1L=V1R≧V3L=V3R≧V4L=V4R≧V2L=V2R≧VEE

(Note 5) Applies to M, FRM, CL, $\overline{RST}$, ADC, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0∿7.

■ ELECTRICAL CHARACTERISTICS

(GND=0V, VCC=4.5 ∿ 5.5V, Vcc-VEE=8∿17.0V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit	Note
			Min.	Typ.	Max.		
Input "High" voltage	V_{IHC}		0.7×Vcc	-	Vcc	V	1
	V_{IHT}		2.0	-	Vcc	V	2
Input "Low" voltage	V_{ILC}		0	-	0.3×Vcc	V	1
	V_{ILT}		0	-	0.8	V	2
Output "High" voltage	V_{OH}	IOH=-205μA	2.4	-	-	V	3
Output "Low" voltage	V_{OL}	IOL=1.6mA	-	-	0.4	V	3
Input leakage current	I_{IL}	Vin=GND∿Vcc	-1.0	-	+1.0	μA	4
Three state (OFF) input current	I_{TSL}	Vin=GND∿Vcc	-5.0	-	+5.0	μA	5
Liquid crystal supply leakage current	I_{LSL}	Vin=VEE∿Vcc	-2.0	-	+2.0	μA	6
Driver ON resistance	RON	Vcc-VEE=15V $\pm I_{LOAD}$=0.1mA	-	-	7.5	kΩ	8
Dissipation current	Icc(1)	During display	-	-	100	μA	7
	Icc(2)	During access / During access cycle= 1MHz	-	-	500	μA	7

(Note 1) Applies to M, FRM, CL, $\overline{RST}$, φ1 and φ2.

(Note 2) Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I and DB0 ∿ 7.

(Note 3) Applies to DB0 ∿ 7.

(Note 4) Applies to terminals except for DB0 ∿ 7.

(Note 5) Applies to DB0 ∿ 7 at high impedance.

(Note 6) Applies to V1L ∿ V4L and V1R ∿ V4R.

(Note 7) Specified when liquid crystal display is in 1/64 duty.

Operation frequency f_{CLK}=250 kHz (φ1 and φ2 frequency)

Frame frequency f_M = 70 Hz (FRM frequency)

Specified in the state of

Output terminal ----- not loaded

Input level --------- V_{IH}=Vcc (V)

V_{IL}=GND (V)

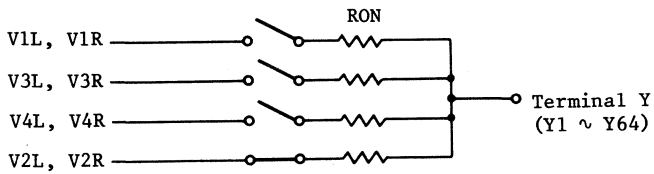
Measured at Vcc terminal

(Note 8) Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition.

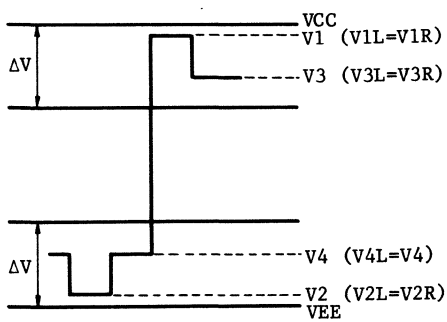
VCC - VEE = 15.5V

V1L=V1R, V3L=V3R = VCC-2/7 (VCC-VEE)

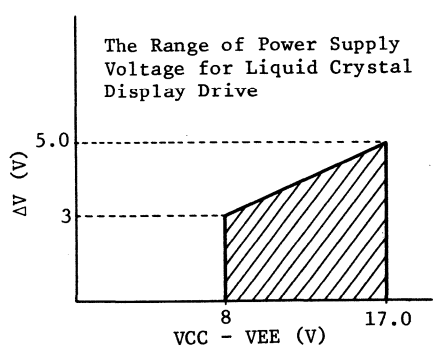
V2L=V2R, V4L=V4R = VEE+2/7 (VCC-VEE)



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage VCC-VEE.



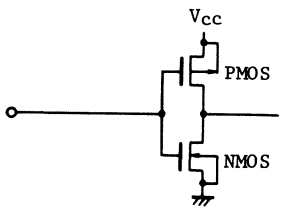
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage VCC-VEE and ΔV

Terminal Configuration

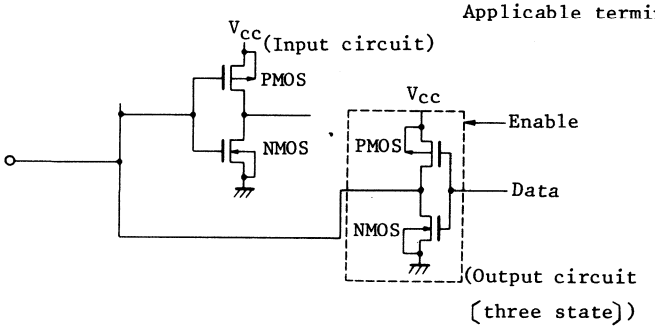
● Input Terminal



Applicable terminals :
M, FRM, CL, $\overline{RST}$, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3,
E, R/W, D/I, ADC

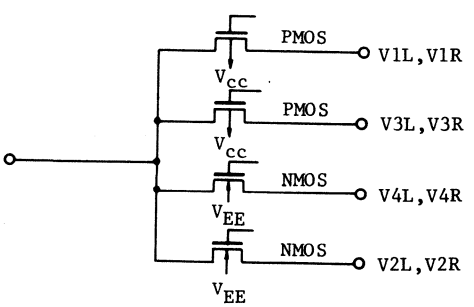
● Input/Output Terminal

Applicable terminals : DB0∿DB7



● Output Terminal

Applicable terminals:
Y1 ∿ Y64



● INTERFACE AC CHARACTERISTICS

(1) MPU Interface

(GND=0V, Vcc=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	P_{WEH}	450	-	-	ns	1, 2
E low level width	P_{WEL}	450	-	-	ns	1, 2
E rise time	tr	-	-	25	ns	1, 2
E fall time	tf	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	20	-	-	ns	2

(Note 1)

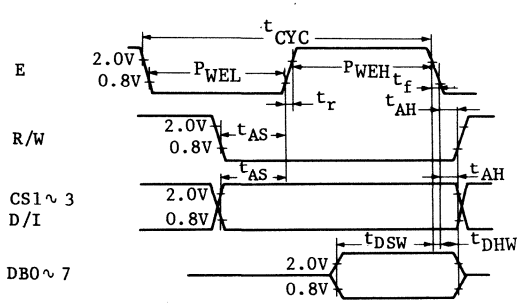


Fig. 1 CPU Write Timing

(Note 2)

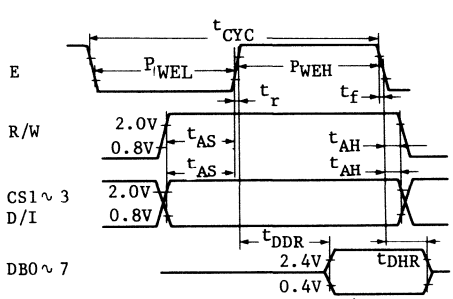
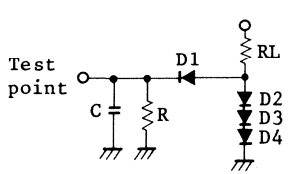


Fig. 2 CPU Read Timing

(Note 3) DB0 ∿ 7 : load circuit



RL=2.4KΩ

R =11KΩ

C =130pF (including jig capacity)

Diodes D1 to D4 are all 1S2074Ⓗ.

(2) Clock Timing

(GND=0V, Vcc=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit
			Min.	Typ.	Max.	
φ1, φ2 cycle time	tcyc	Fig. 3	2.5	-	20	μs
φ1 "Low" level width	$t_{WL\phi1}$	Fig. 3	625	-	-	ns
φ2 "Low" level width	$t_{WL\phi2}$	Fig. 3	625	-	-	ns
φ1 "High" level width	$t_{WH\phi1}$	Fig. 3	1875	-	-	ns
φ2 "High" level width	$t_{WH\phi2}$	Fig. 3	1875	-	-	ns
φ1-φ2 phase difference	t_{D12}	Fig. 3	625	-	-	ns
φ2-φ1 phase difference	t_{D21}	Fig. 3	625	-	-	ns
φ1, φ2 rise time	tr	Fig. 3	-	-	150	ns
φ1, φ2 fall time	tf	Fig. 3	-	-	150	ns

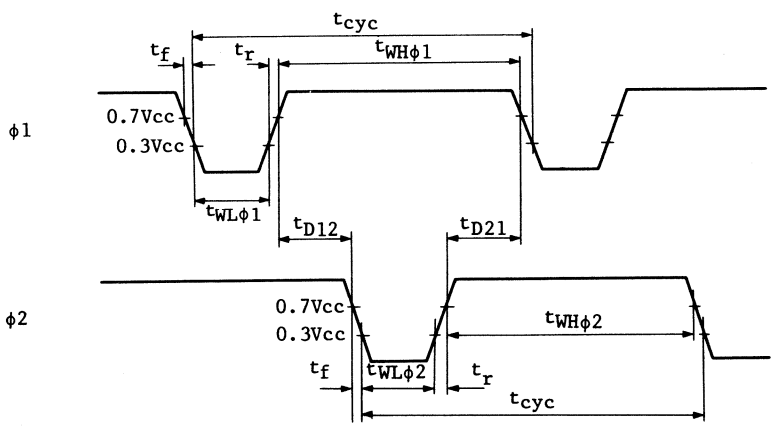


Fig. 3 External Clock Waveform

(3) Display Control Timing

(GND=0V, V_{CC}=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit
			Min.	Typ.	Max.	
FRM delay time	t_{DFRM}	Fig. 4	-2	-	+2	µs
M delay time	t_{DM}	Fig. 4	-2	-	+2	µs
CL "Low" level width	t_{WLCL}	Fig. 4	35	-	-	µs
CL "High" level width	t_{WHCL}	Fig. 4	35	-	-	µs

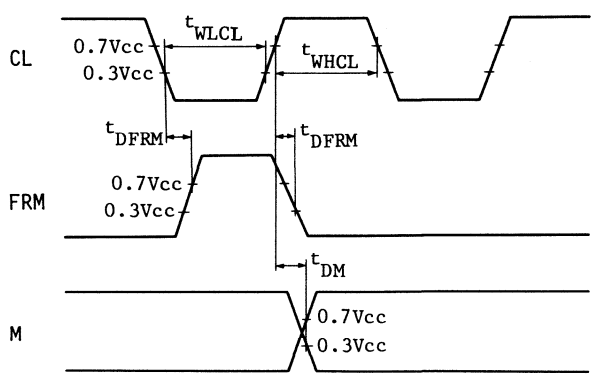
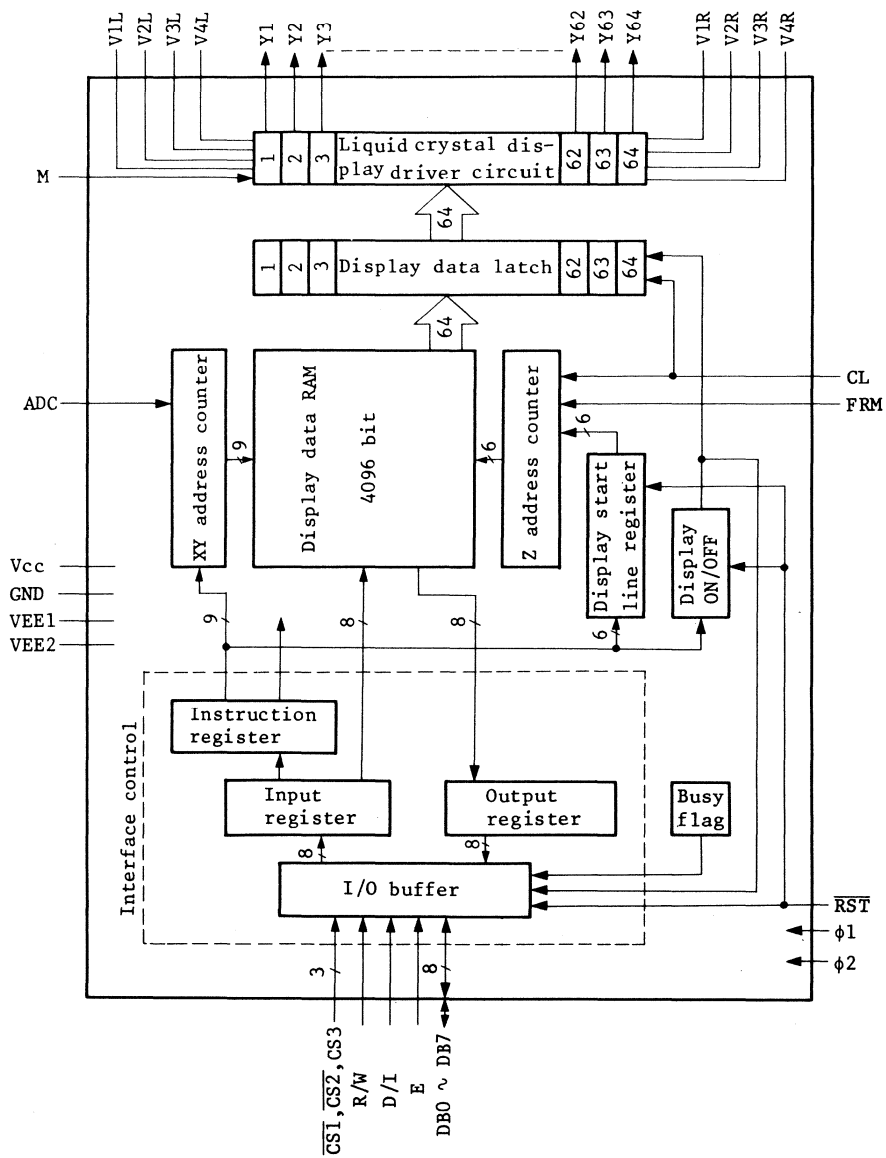


Fig. 4 Display Control Signal Waveform

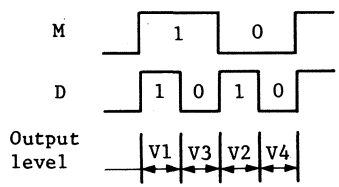
■ BLOCK DIAGRAM



TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0V V_{CC} = 5V ± 10%
V_{EE} 1 V_{EE} 2	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is Vcc-VEE=8 ∿ 15.5V. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L(V1R), V2L(V2R)---Selection level V3L(V3R), V4L(V4R)---Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the next conditions. Terminal name: $\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ Condition: 'L' 'L' 'H'
E	1	I	MPU	Enable At write(R/W=L) : Data of DB0 to DB7 is latched at the fall of E. At read(R/W=H) : Data appears at DB0 to DB7 while E is in "High" level.

Terminal name	Number of terminals	I/O	Connected to	Functions
R/W	1	I	MPU	Read/Write R/W=H : Data appears at DB0 to DB7 and can be read by the CPU When E=H, $\overline{CS1}$, $\overline{CS2}$=L and CS3=H. R/W=L : DB0 to DB7 can accept at fall of E when $\overline{CS1}$, $\overline{CS2}$=L and CS3=H.
D/I	1	I	MPU	Data/Instruction D/I=H : Indicates that the data of DB0 to DB7 is display data. D/I=L : Indicates that the data of DB0 to DB7 is display control data.
ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H : Y1-$0, Y64-$63 ADC=L : Y64-$0, Y1-$63
DB0∿DB7	8	I/O	MPU	Data bus, three-state I/O common terminal
M	1	I	HD61203	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203	Display synchronous signal (frame signal). This signal presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203	Synchronous signal to latch display data. The CL signal indicates to count up the display output adress counter and latch the display data at rising.

Terminal name	Number of terminals	I/O	Connected to	Functions
$\phi1, \phi2$	2	I	HD61203	2-phase clock signal for internal operation. The $\phi1$ and $\phi2$ clocks are used to perform the operations (I/O of display data and execution of instructions) other than display.
Y1∿Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins outputs light ON level when "1" is in the display RAM, and light OFF level with "0" in it. Relation among output level, M and display data (D) is as follows. 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to "Low" level. (1) ON/OFF register 0 set (display OFF) (2) Display start line register 0 line set (displays from 0 line) After releasing reset, this condition can be changed only by the instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

(Note) "1" corresponds to "High level" in positive logic.

FUNCTION OF EACH BLOCK

● Interface Control

(1) I/O buffer

Data is transferred through 8 data buses (DB0 ∿ DB7).

DB7 .... MSB (Most Significant Bit)

DB0 .... LSB (Least Significant Bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, namely, the internal state is maintained and no instruction excute. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

(2) Register

Both input register and output register are provided to interface to MPU of which the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

Table 1. Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

① Input register

Input register is used to store data temporarily before writing it into display data RAM.
The data from MPU is written into input register, then into display data RAM automatically by internal operation.
When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of E signal.

② Output register

Output register is used to store data temporarily which is read from display data RAM. To read out the data from output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With READ instruction, data stored in the output register is output while E is "H" level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.
The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address can not be output with READ instruction soon after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Fig. 5 shows the CPU read timing.

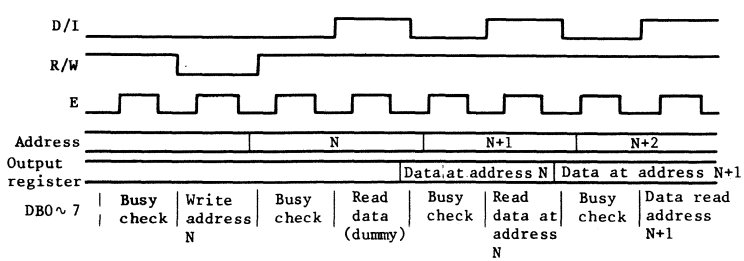
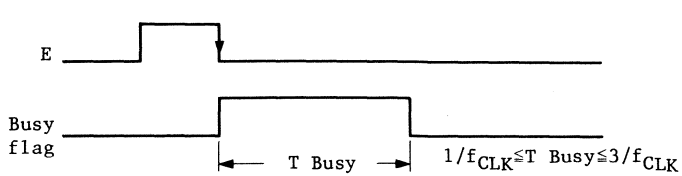


Fig. 5 CPU Read Timing

● Busy Flag

"1" of busy flag indicates that HD61202 is on the move and any instructions except Status Read instruction can not be accepted. The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset ("0") before the issue of instruction.



f_{CLK} is $\phi 1$, $\phi 2$ frequency

- Display ON/OFF Flip Flop

Display ON/OFF flip flop selects one of two states, ON state and OFF state of segments Y1 to Y64. In ON state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in OFF state independent of the data in RAM. It is controlled by display ON/OFF instruction '0' of $\overline{RST}$ signal sets the segments in OFF state. The status of the flip flop is output to DB5 by Status Read instruction. Display ON/OFF instruction does not influence data in RAM. To control display data latch by this flip flop, CL signal (display synchronous signal) should be input correctly.

- Display Start Line Register

The register specifies a line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by display start line set instruction, with 'H' level of FRM signal instructing to start the display, the information in this register is transferred to Z address counter which controls the display address, and the Z address counter is preset.

- X, Y Address Counter

This is a 9-bit counter which designates addresses of internal display data RAM. X address counter of upper 3 bits and Y address counter of lower 6 bits should be set each address by respective instruction.

(1) X address counter

Ordinary register with no count functions. An address is set in by instructions.

(2) Y address counter

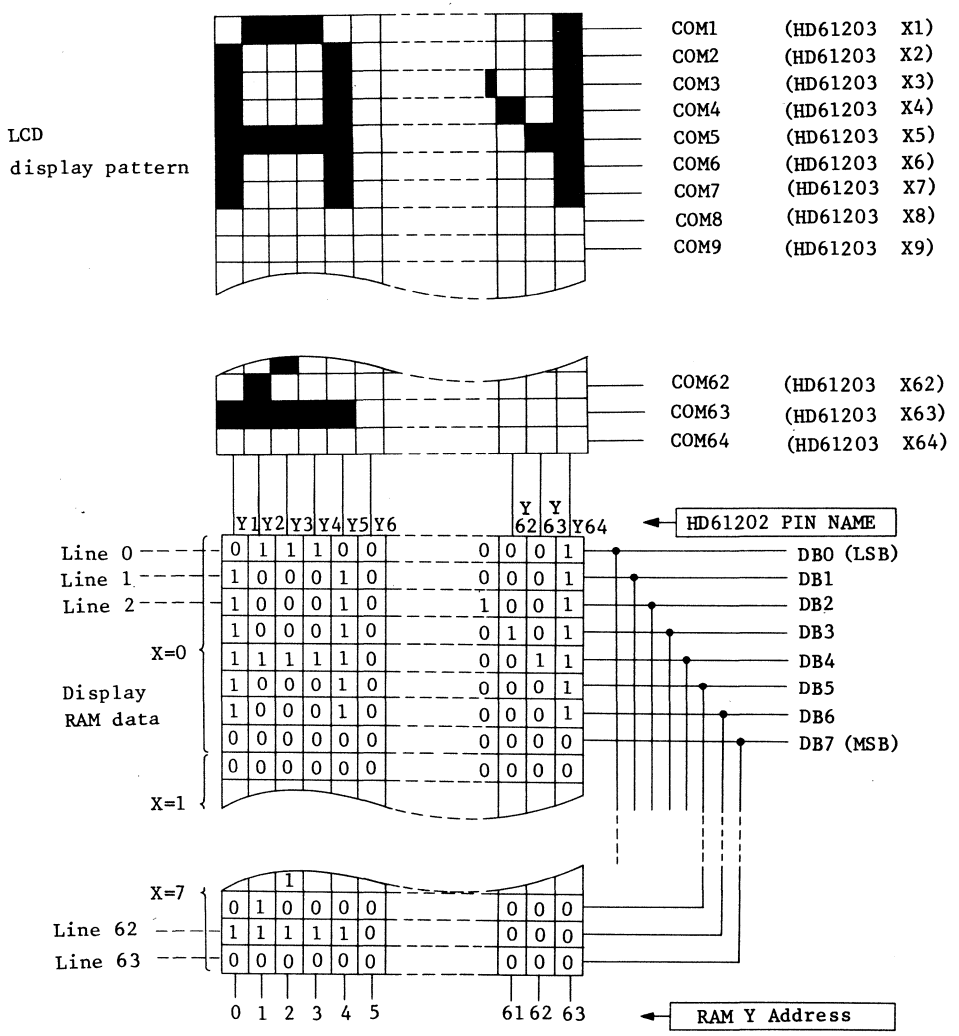
An address is set in by instruction and it is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

- Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light ON (data=1) and light OFF (data=0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

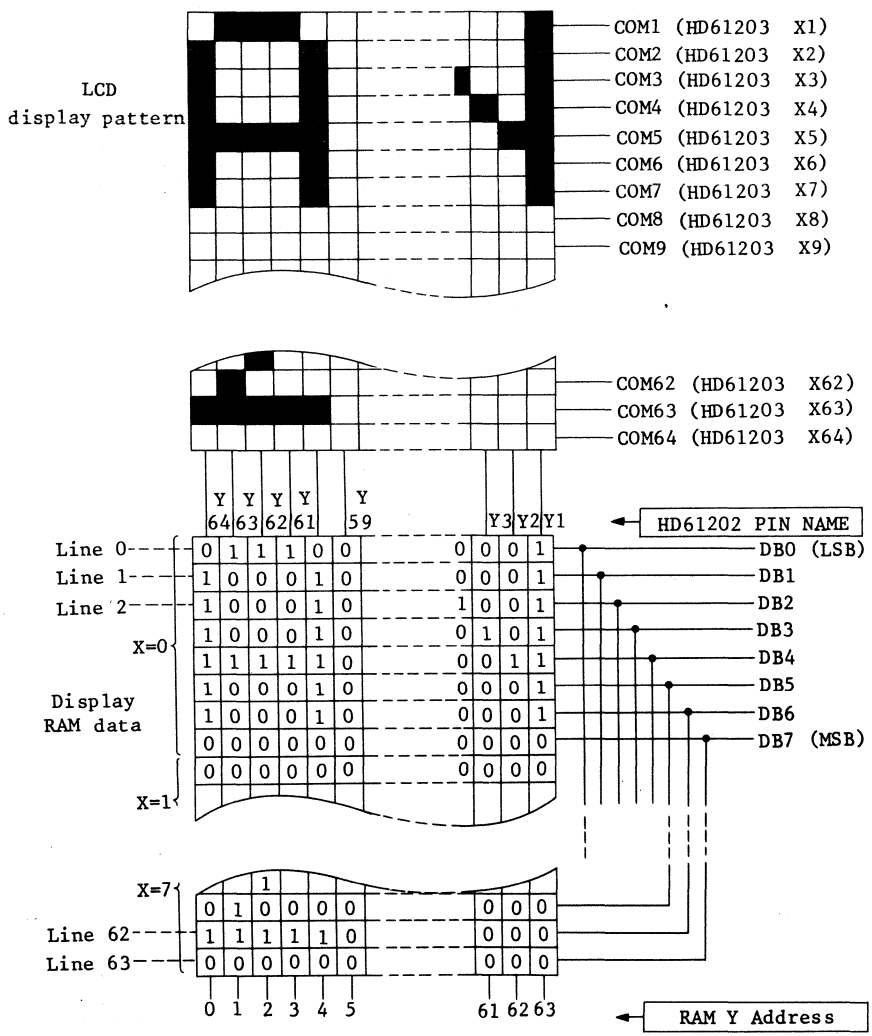
As ADC signal controls Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Fig. 6 shows the relations between Y address of RAM and segment pins in the cases of ADC=1 and ADC=0. (display start line=0, 1/64 duty).



(a) ADC="1" (Connected to Vcc)

Fig. 6 Relation between RAM Data and Display



(b) ADC="0" (Connected to GND)

Fig. 6 Relation Between RAM Data and Display

- Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6-bit and counts up at the fall of CL signal. With "H" level of FRM, the contents of the display start line register is preset at the Z counter.

- Display data Latch

The display data latch stores the display data temporarily which is output from display data RAM to liquid crystal driving circuit. Data is latched at the rise of CL signal. Display ON/OFF instruction controls the data in this latch and does not influence data in display data RAM.

- Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

- Reset

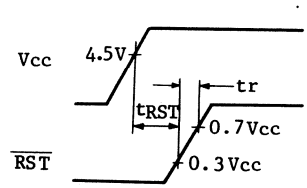
The system can be initialized by setting $\overline{RST}$ terminal at "Low" level when turning power ON.

1) Display-OFF
2) Set display start line register 0 line.

While $\overline{RST}$ is in Low level, any instruction except Status Read cannot be accepted. Therefore, Carry out other instructions after making sure that DB4=0 (clear RESET) and DB7=0 (Ready) by Status Read instruction. The conditions of Power Supply at initial power up are as follows.

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	t_{RST}	1.0	-	_	μs
Rise time	t_r	-	-	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the register except ON/OFF register and in RAM.



Display Control Instructions

Outline

Table 2 shows the instructions. Read/Write (R/W) signal, Data/Instruction (D/I) signal and Data bus signal (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.
These explanations are detailed from the following page. Generally, there are following three kinds of instructions.

(1) Instruction to give addresses in the internal RAM
(2) Instruction to transfer data from/to the internal RAM
(3) Other instructions

In general use, the instruction (2) are used most frequently. But, since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be lessened. During the execution of an instruction, the system cannot accept other instructions than Status Read instruction. Send instructions from MPU after making sure if the busy flag is "0", which is the proof an instruction is not being excuted.

Table 2. Instructions

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1 Display ON/OFF	0	0	0	0	1	1	1	1	1	1/0	Controls the ON/OFF of display. RAM data and internal status are not affected. 1:ON, 0:OFF.	
2 Display start line	0	0	1	1	display start line (0∿63)						Specifies a RAM line displayed at the top of the screen.	
3 Set page (X address)	0	0	1	0	1	1	1	Page (0∿7)			Sets the page (X address) of RAM at the page (X address) register.	
4 Set Address	0	0	0	1	Y address (0∿63)						Sets the Y address at the Y address counter	
5 Status Read	1	0	Busy	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: reset 0:normal ON/OFF 1: display OFF 0:display ON Busy 1: on the internal operation 0: Ready	
6 Write deisplay data	0	1	Write Data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
7 Read display data	1	1	Read Data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note 1) Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.

$(1/f_{CLK} \leqq T_{BUSY} \leqq 3/f_{CLK})$

● Detailed Explanation

(1) Display ON/OFF

	R/W	D/I	DB7						DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order-bit low-order-bit →

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen width D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

(2) Display start line

	R/W	D/I	DB7						DB0
Code	0	0	1	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Z address AAAAAA (binary) of the display data RAM is set at the display start line register and displayed at the top of the screen. Fig. 7 are the examples of display (1/64 duty) when the start line=0 ∿ 3. When the display duty is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

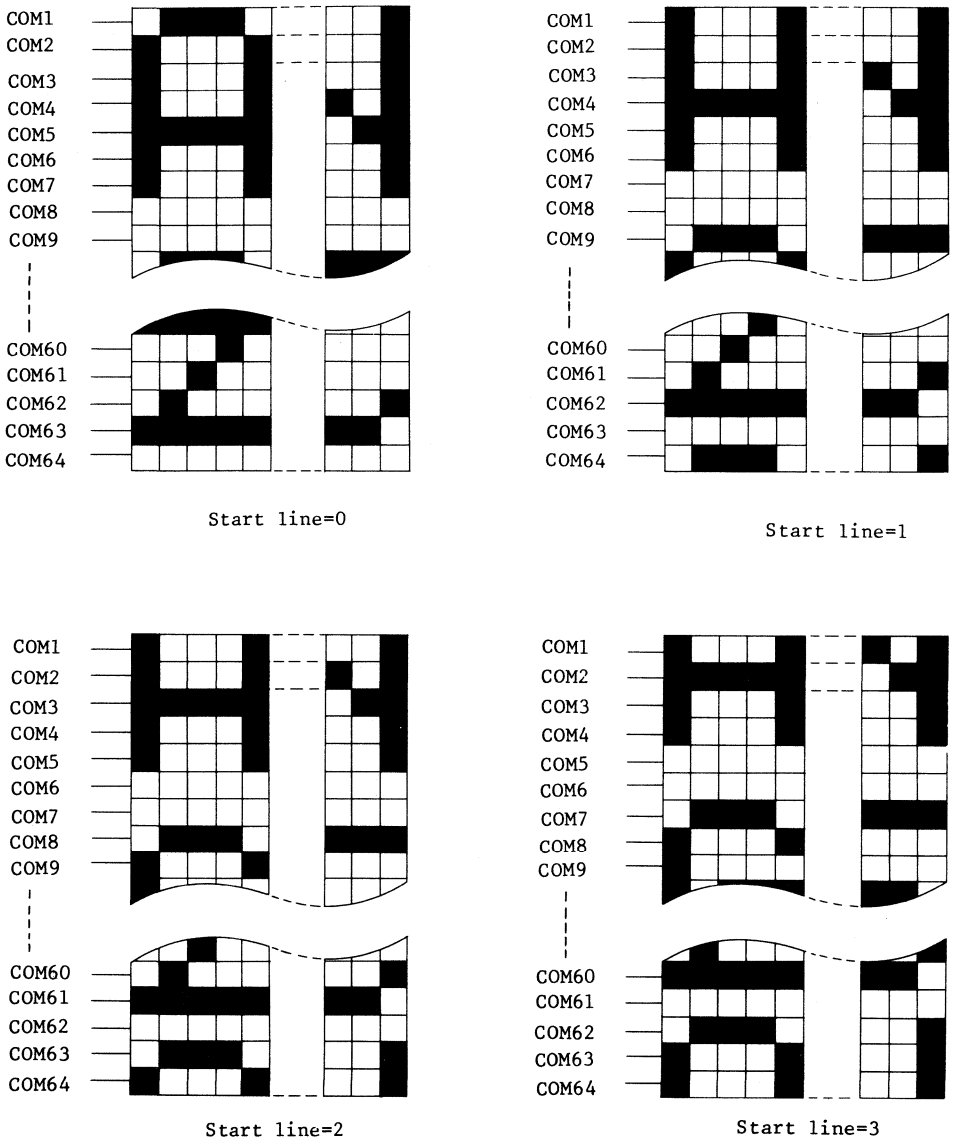


Fig. 7 Relation Between Start Line and Display

(3) Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order-bit low-order-bit →

X address AAA (binary) of the display data RAM is set at the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

(4) Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Y address AAAAAA (binary) of the display data RAM is set at the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

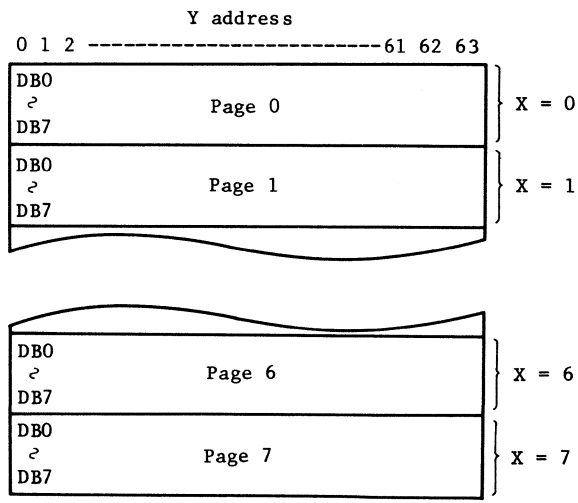


Fig. 8 Address Configuration of Display Data RAM

(5) Status Read

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/ OFF	RESET	0	0	0	0
	← high-order-bit									low-order-bit →

BUSY: When BUSY is 1, the LSI is in internal operation. No instructions are accepted while BUSY is 1, so you should make sure that BUSY is 0 before writing the next instruction.

ON/OFF: This bit shows the liquid crystal display conditions - ON condition or OFF condition.
When ON/OFF is 1, the display is in OFF condition.
When ON/OFF is 0, the display is in ON condition.

RESET: RESET=1 shows that the system is being initialized. In this condition, any instructions except Status Read instruction cannot be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation.

(6) Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D
	← high-order-bit									low-order-bit →

Writes 8-bit data DDDDDDDD (binary) into the display data RAM.
Then Y address is increased by 1 automatically.

(7) Read Display Data

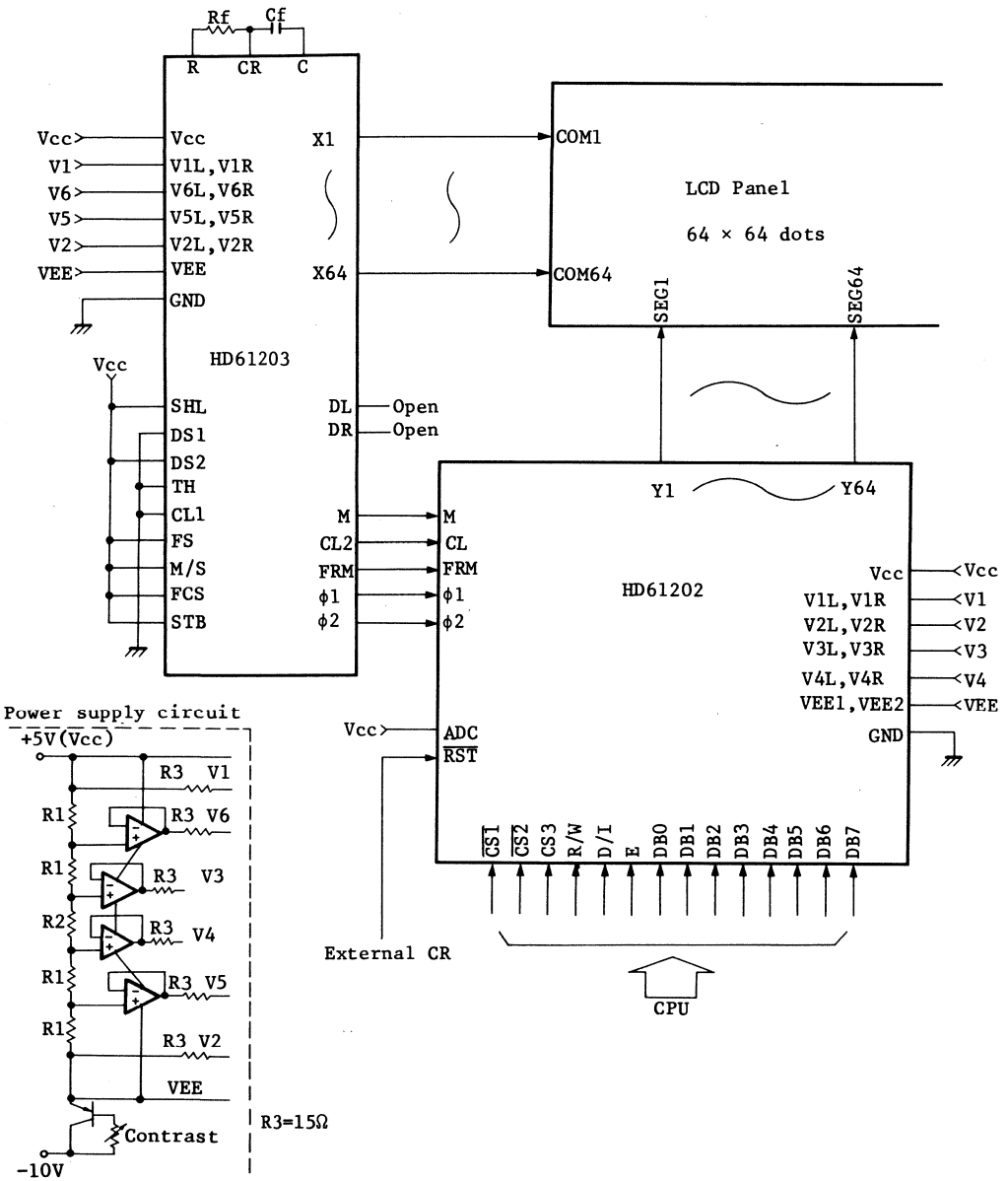
	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D
	← high-order-bit									low-order-bit →

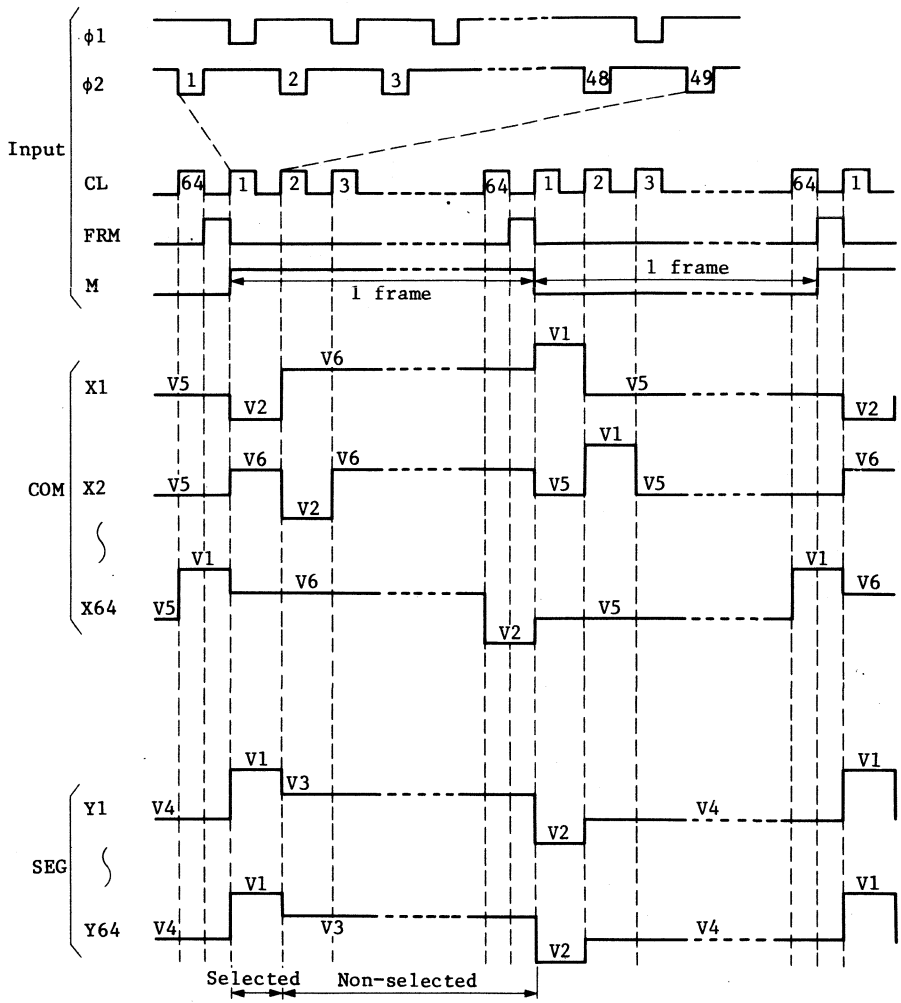
Read out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary soon after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

The Usage of HD61202

- Interface with HD61203 (1/64 duty)



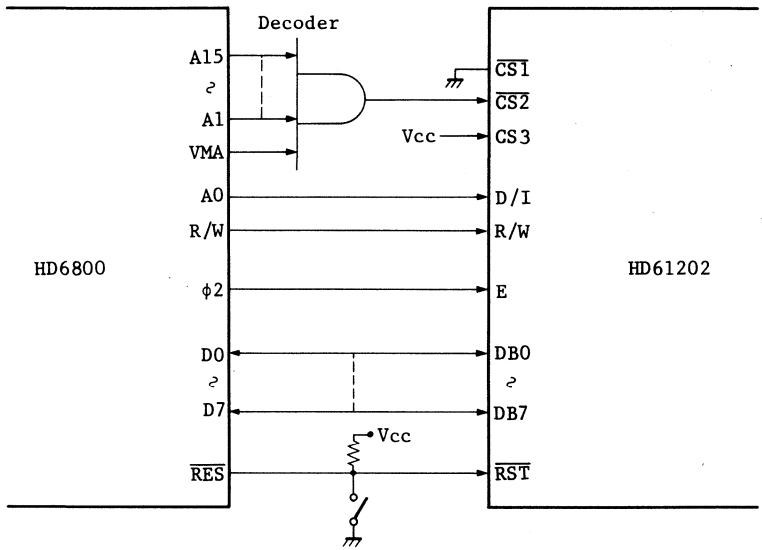


The wave forms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Fig. 9 LCD Driver Timing Chart (1/64 duty)

Interface with CPU

a) Example of connection with HD6800



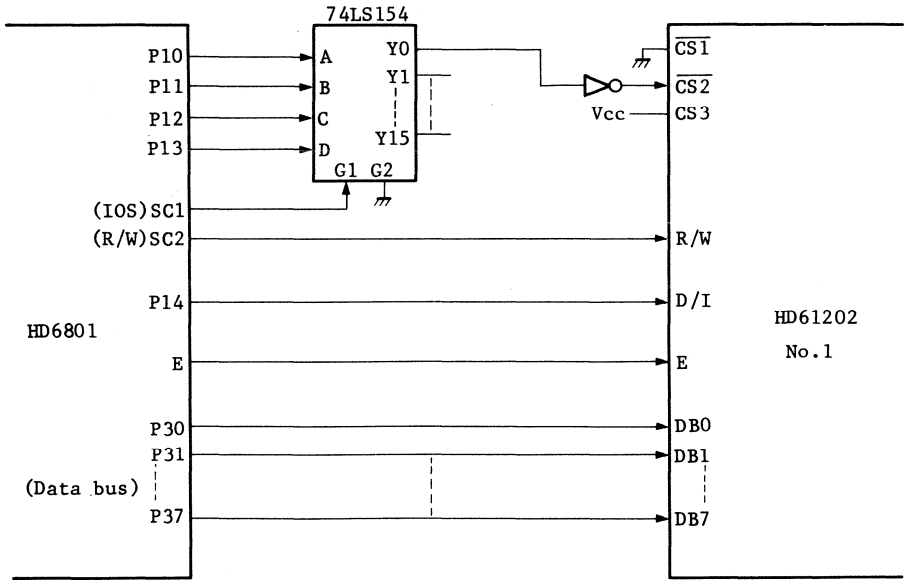
The example of connection with HD6800 series

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/Write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

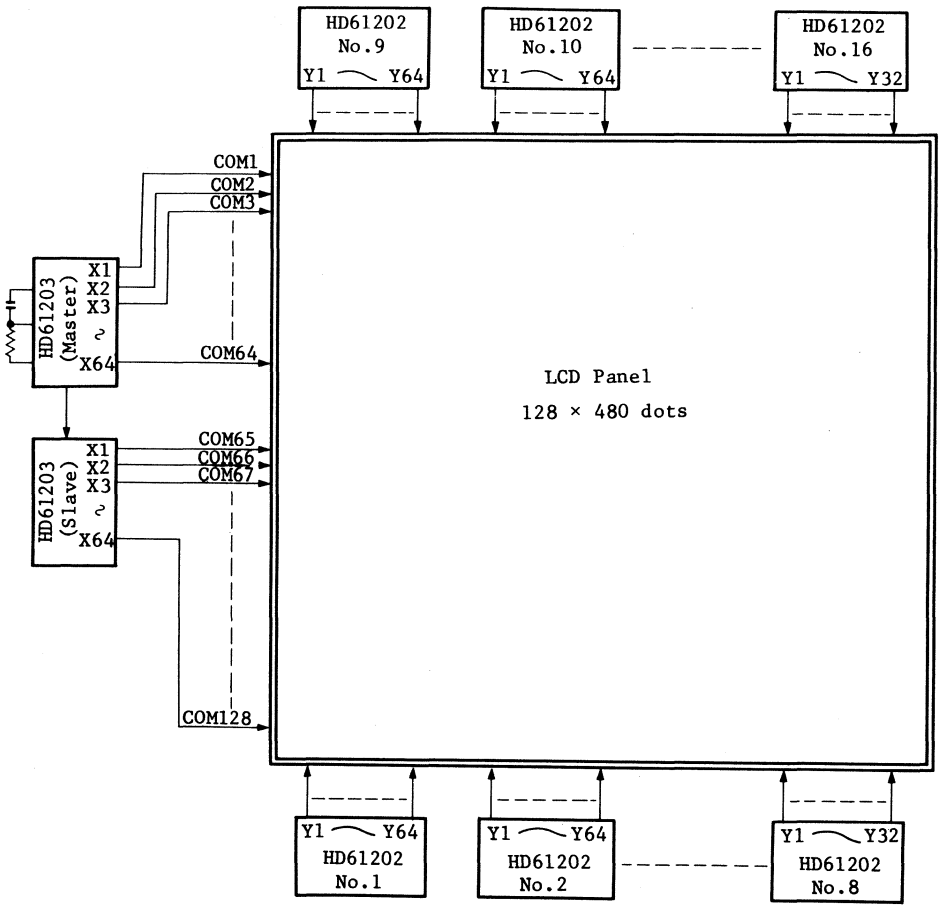
Therefore, you can control HD61202 by reading/writing the data at these addresses.

b) Example of connection with HD6801



- Set HD6801 in Mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 is 4 to 16 decoder and generate chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after making the operation possible by P10 to P13 and specifying D/I signal by P14, read/write from/to. the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to the each manual.

● Example of Application



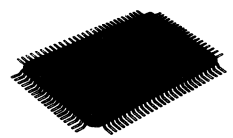
Note) In this example, two HD61203 's output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, you had better drive in 2 rows as this example to guarantee the display quality.

HD61203

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

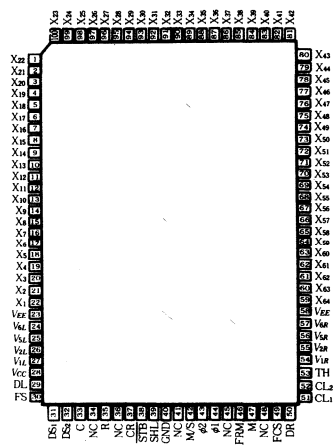
The HD61203 is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61203 is produced in a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61203 and the column (segment) driver HD61202.



(FP-100)

PIN ARRANGEMENT



(Top View)

FEATURES

- Dot matrix liquid crystal graphic display common driver with low impedance.
- Low impedance -- 1.5kΩ max.
- Internal liquid crystal display driver circuit -- 64 circuits
- Internal dynamic display timing generator circuit
- Display duty
  When used with the column driver HD61202
  1/48, 1/64, 1/96, 1/128
  When used with the column driver HD61200
  Selectable out of 1/32 to 1/128

- Low power dissipation
  - during display 5mW
- Power supplies : V_{CC} 5V ± 10%
- Power supply voltage for liquid crystal display drive ..... 8V ∿ 17V
- CMOS process
- 100-pin flat plastic package (FP-100)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	2
Power Supply Voltage (2)	V_{EE}	V_{CC}-19.0 ∿ V_{CC} +0.3	V	5
Terminal Voltage (1)	V_{T1}	-0.3 ∿ V_{CC} +0.3	V	2, 3
Terminal Voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC} +0.3	V	4, 5
Operating Temperature	Topr	-20 ∿ +75	°C	
Storage Temperature	Tstg	-55 ∿ +125	°C	

Note 1) If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

Note 2) Based on GND=0V

Note 3) Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) and I/O terminals at high impedance.

Note 4) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R.

Note 5) Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V_{5R}, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.
Maintain $V_{CC} \geq V1L=V1R \geq V6L=V6R \geq V5L=V5R \geq V2L=V2R \geq V_{EE}$

ELECTRICAL CHARACTERISTICS

- DC Characteristics (V_{CC}=5V ± 10%, GND=0V, VCC-VEE=8.0∿17.0V Ta= -20 ∿ +75°C)

Test Item	Symbol	Test conditions	Specifications Min	Typ.	Max	Unit	Note
Input "High" voltage	V_{IH}		0.7×Vcc	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		GND	-	0.3×Vcc	V	1
Output "High" voltage	V_{OH}	I_{OH}=-0.4mA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V	2
Vi-Xj ON resistance	R_{ON}	V_{CC}-V_{EE}=17V Load current ±150μA	-	-	1.5	kΩ	13
Input Leakage Current	I_{IL1}	Vin=0∿V_{CC}	-1.0	-	1.0	μA	3
Input Leakage Current	I_{IL2}	Vin=V_{EE}∿V_{CC}	-2.0	-	2.0	μA	4
Operating Frequency	f_{opr1}	In master mode External clock operation	50	-	600	kHz	5
Operating Frequency	f_{opr2}	In slave mode Shift register	0.5	-	1500	kHz	6
Oscillation Frequency	fosc	Cf=20pF±5% Rf=47KΩ±2%	315	450	585	kHz	7,12
Dissipation Current (1)	I_{GG1}	In master mode 1/128 duty Cf=20pF Rf=47kΩ	-	-	1.0	mA	8,9
Dissipation Current (2)	I_{GG2}	In slave mode 1/128 duty	-	-	200	μA	8,10
Dissipation Current	I_{EE}	In master mode 1/128 duty	-	-	100	μA	8,11

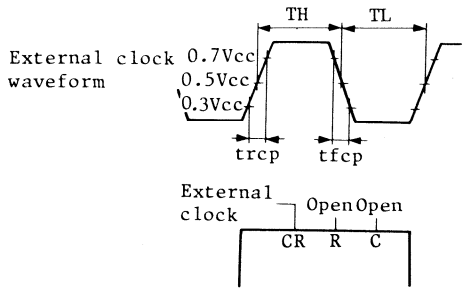
Note 1) Applies to input terminals FS, DS1, DS2, CR, SHL, M/S and FCS and I/O terminals DL, M, DR and CL2 in the input status.

Note 2) Applies to output terminals, φ1, φ2 and FRM and I/O common terminals DL, M, DR and CL2 in the output status.

Note 3) Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1 and TH, I/O terminals DL, M, DR and CL2 in the input status and NC terminals.

Note 4) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R. Don't connect any lines to X1 to X64.

Note 5) External clock is as follows.

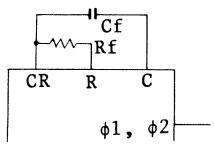


$$\text{Duty} = \frac{TH}{TH+TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty	45	50	55	%
trcp	-	-	50	ns
tfcp	-	-	50	ns

Note 6) Applies to the shift register in the slave mode. For details, refer to AC Characteristics.

Note 7) Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency ($f\phi$) at $\phi 1$ or $\phi 2$.



Cf=20pF
Rf=47kΩ fosc=2 × fφ

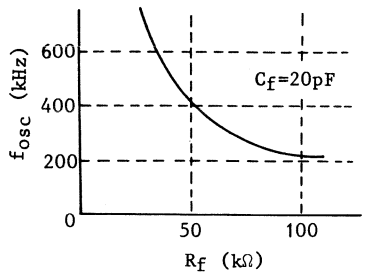
Note 8) No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH}=V_{CC}$ and $V_{IL}=GND$.

Note 9) This value is specified about current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$ and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in Note 7.

Note 10) This value is specified about current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH and M/S to GND and the terminals CL2, M and DL are respectively connected to terminals CL2, M and DL of the HD61203 under the condition described in Note 9.

Note 11) This value is specified about current flowing through V_{EE} under the condition described in Note 9. Don't connect any lines to terminal V.

Note 12) This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting condition.

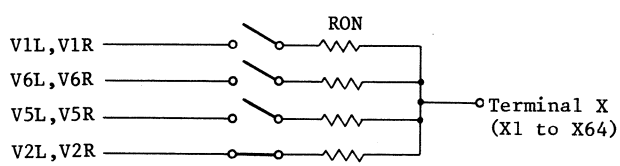


Note 13) Resistance between terminal X and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following condition.

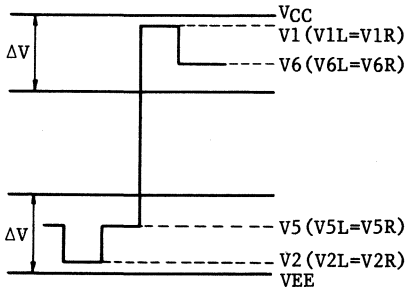
VCC - VEE = 17V

V1L=V1R, V6L=V6R = VCC-1/7(VCC-VEE)

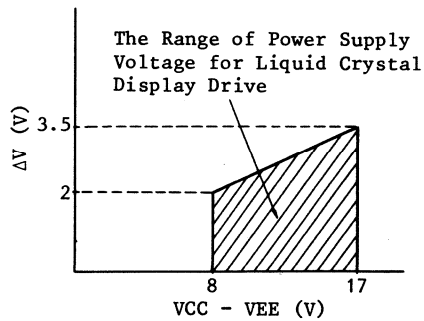
V2L=V2R, V5L=V5R = VEE+1/7(VCC-VEE)



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V6L=V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage VCC-VEE.



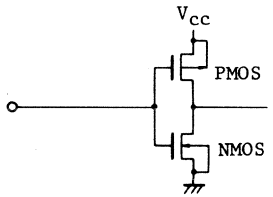
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage VCC-VEE and ΔV

Terminal Configuration

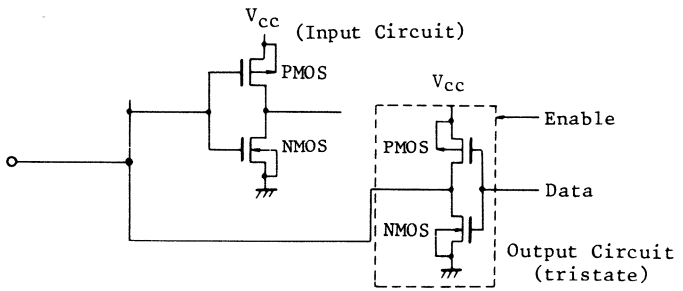
● Input Terminal



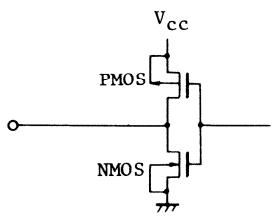
Applicable terminals :
CR, M/S, SHL, FCS, DS1, DS2, FS

● I/O Terminal

Applicable terminal : DL, DR, CL2, M

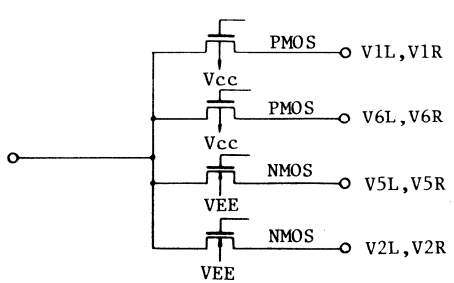


● Output Terminal



Applicable terminal : $\phi 1$, $\phi 2$, FRM

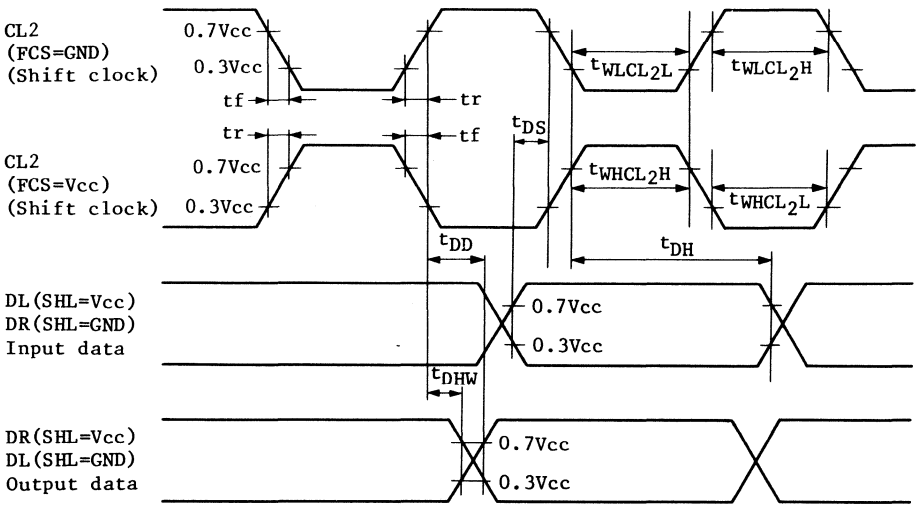
● Output Terminal



Applicable terminals:
X1 to X64

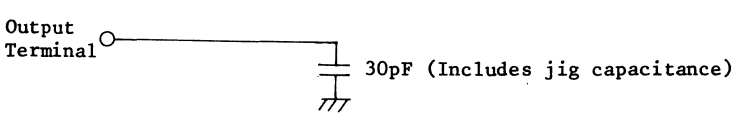
● AC Characteristics (V_{CC}=5V±10% GND=0V, Ta=-20∿+75°C)

(1) In the slave mode (M/S=GND)



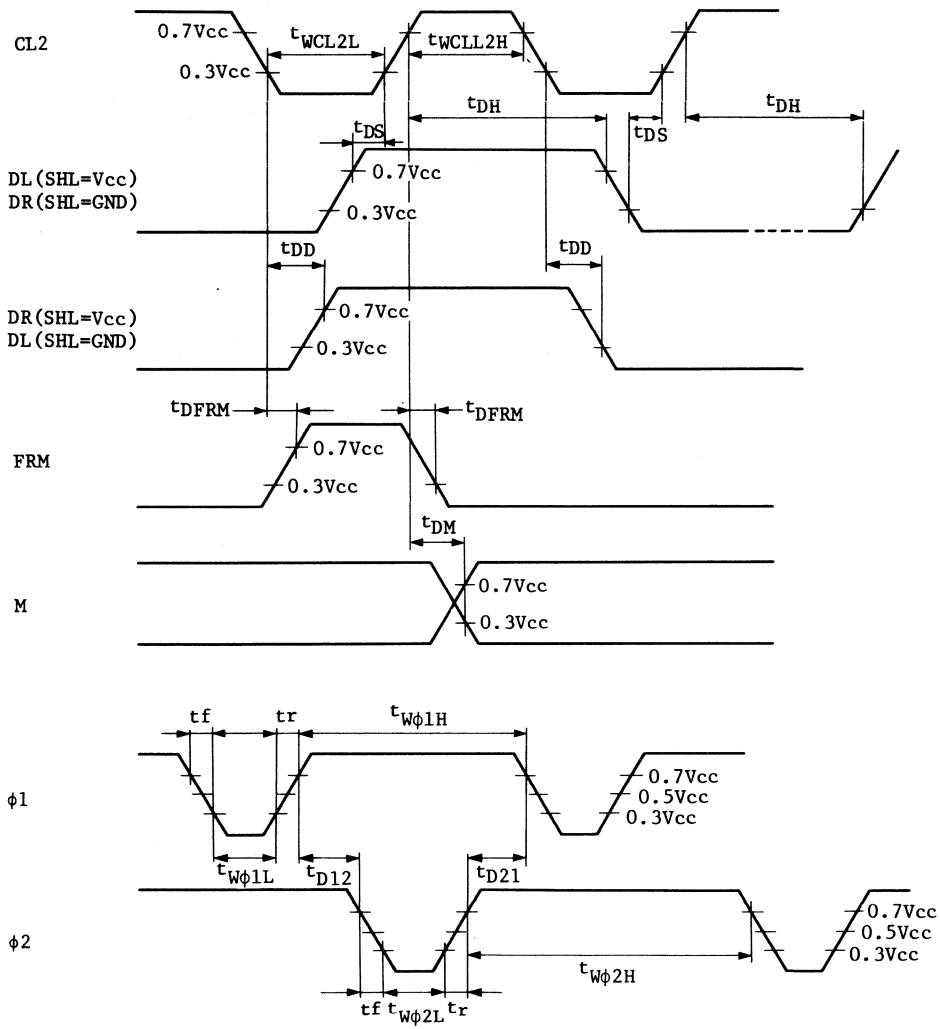
Item	Symbol	Min.	Typ.	Max	Unit	Note
CL2 "Low" level width (FCS=GND)	t_{WLCL2L}	450	-	-	ns	
CL2 "High" level width (FCS=GND)	t_{WLCL2H}	150	-	-	ns	
CL2 "Low" level width (FCS=V_{CC})	t_{WHCL2L}	150	-	-	ns	
CL2 "High" level width (FCS=V_{CC})	t_{WHCL2H}	450	-	-	ns	
Data setup time	t_{DS}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_{DD}	-	-	200	ns	1
Output data hold time	t_{DHW}	10	-	-	ns	
CL2 rise time	tr	-	-	30	ns	
CL2 fall time	t_f	-	-	30	ns	

Note 1) The following load circuit is connected for specification.



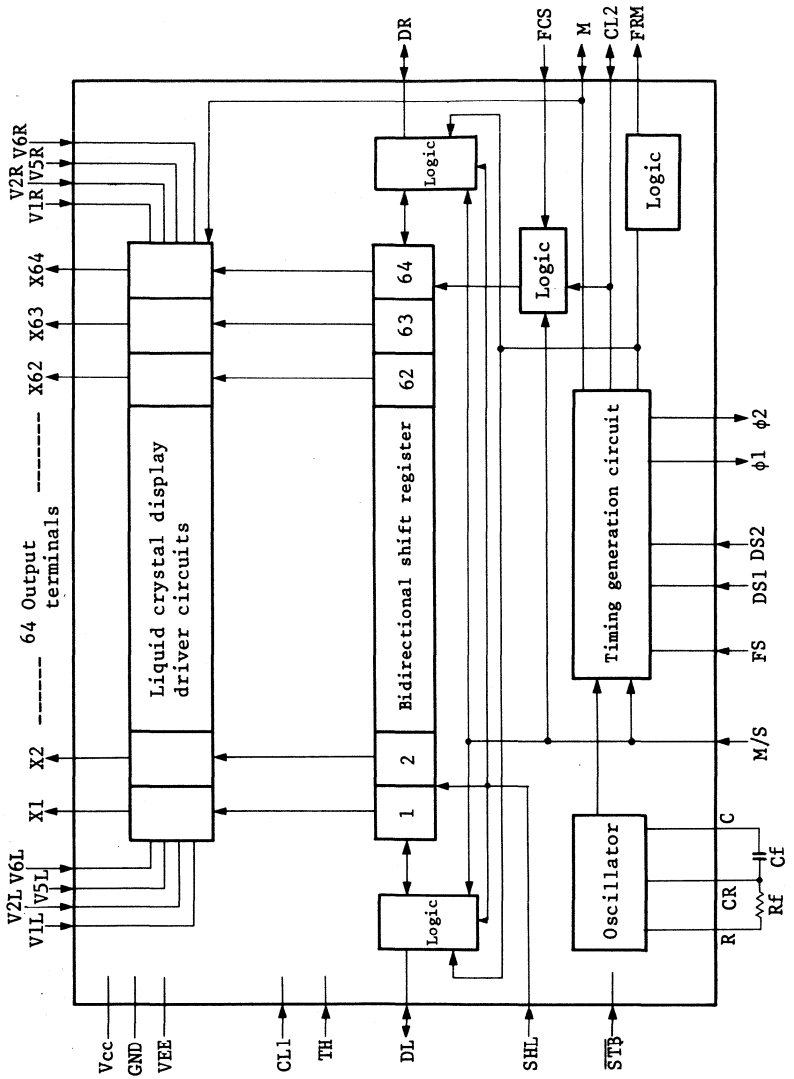
(2) In the master mode

($M/S=V_{CC}$, $FCS=V_{CC}$, Cf=20pF, Rf=47KΩ)



Item	Symbol	Min.	Typ.	Max.	Unit
Data setup time	t_{DS}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	μs
Data delay time	t_{DD}	5	-	-	μs
FRM delay time	t_{DFRM}	-2	-	2	μs
M delay time	t_{DM}	-2	-	2	μs
CL_2 "Low" level width	t_{WCL2L}	35	-	-	μs
CL_2 "High" level width	t_{WCL2H}	35	-	-	μs
$\phi 1$ "Low" level width	$t_{W\phi 1L}$	700	-	-	ns
$\phi 2$ "Low" level width	$t_{W\phi 2L}$	700	-	-	ns
$\phi 1$ "High" level width	$t_{W\phi 1H}$	2100	-	-	ns
$\phi 2$ "High" level width	$t_{W\phi 2H}$	2100	-	-	ns
$\phi 1$-$\phi 2$ phase difference	t_{D12}	700	-	-	ns
$\phi 2$-$\phi 1$ phase difference	t_{D21}	700	-	-	ns
$\phi 1$, $\phi 2$ rise time	tr	-	-	150	ns
$\phi 1$, $\phi 2$ fall time	tf	-	-	150	ns

■ Block Diagram

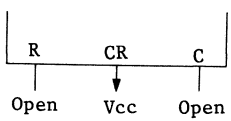


Block Functions

- Oscillator

The oscillator is a CR oscillator that generates display timing signals and operating clocks for the HD61202. It is required when the HD61203 is used with the HD61202. It attaches an oscillation resistor Rf and an oscillation capacity Cf as shown in the following figure and terminal $\overline{STB}$ is connected to "high" level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminal R and C.

Oscillator is not required when the HD61203 is used with the HD61830. Then, connect terminal CR to "high" level and don't connect any lines to terminals R and C.



- Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61202. This circuit is required when the HD61203 is used with the HD61202. Then connect terminal M/S to "high" level. (master mode). It is not necessary when display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals FS, DS1 and DS2 to "high" level and M/S to "low" level. (Slave mode)

- Bidirectional Shift Register

This is a 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the side of DL, corresponds to X1 and the highest order bit on the side of DR corresponds to X64.

- Liquid Crystal Display Driver Circuit

  The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

Data from the shift register	M	Output level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

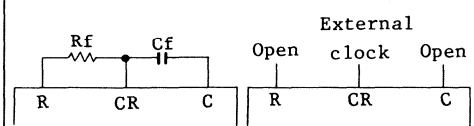
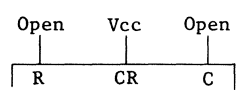
HD61203 Terminal Functions

Terminal name	Number of terminals	I/O	Connected to	Function
VCC GND VEE	1 1 2		Power supply	V_{CC}-GND: Power supply for internal logic. V_{CC}-V_{EE}: Power supply for driver circuit logic.
V1L,V2L, V5L,V6L V1R,V2R V5R,V6R	8		Power supply	Liquid crystal display driver level power supply. V1L(V1R), V2L(V2R): Selected level V5L(V5R), V6L(V6R): Non-selected level voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects Master/Slave M/S=V_{CC}: In master mode When the HD61203 is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61202. Each of I/O common terminals DL, DR, CL2 and M is in the output state. M/S=GND: In slave mode The timing operation circuit stops operating. The HD61203 is used in this mode when combined with the HD61830. Even if combined with the HD61202, this mode is used when display timing signals (M, data, CL2 etc.) are supplied by another HD61203 in the master mode. Terminals M and CL2 are in the input state.

(to be continued)

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>* M/S</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>When SHL is V_{CC}, DL is in the input state and DR is in the output state.
When SHL is GND, DL is in the output state and DR is in the input state.</td></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift clock phase
FCS=V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61203 is used with HD61202 or when MA of the HD61830 connects to CL2 in the combination with the HD61830.
FCS=GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in the combination with the HD61830.</td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects frequency
When the frame frequency is 70Hz, the oscillation frequency should be:
fosc=430kHz at FCS=V_{CC}
fosc=215kHz at FCS=GND
This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.</td></tr>
<tr><td>DS1,DS2</td><td>2</td><td>I</td><td>V_{CC} or GND</td><td>Selects display duty factor
<table><tr><th>Display Duty</th><th>1/48</th><th>1/64</th><th>1/96</th><th>1/128</th></tr><tr><td>DS1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr><tr><td>DS2</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr></table>This terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.</td></tr>
</table>

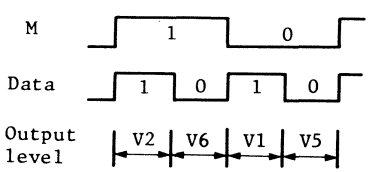
(to be continued)

Terminal name	Number of terminals	I/O	Connected to	Function
$\overline{STB}$ TH CL1	1 1 1	I	V_{CC} or GND	Input terminal for testing Connect $\overline{STB}$ to V_{CC}. Connect TH and CL1 to GND.
CR,R,C	3			Oscillator. In the master mode, use these terminals as shown below. Usage of these terminal in the master mode Internal oscillation External clock  In the slave mode, stop the oscillator as shown below. 
$\phi 1$, $\phi 2$	2	O	HD61202	Operating clock output terminals for the HD61202. Master mode: Connect these terminals to terminals $\phi 1$ and $\phi 2$ of the HD61202 respectively. Slave mode : Don't connect any lines to these terminals.
FRM	1	O	HD61202	Frame signal Master mode: Connect this terminal to terminals FRM of the HD61202. Slave mode : Don't connect any lines to this terminal.

(to be continued)

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61202</td><td>Signal to convert LCD driver signal into AC.
Master mode: Output terminal. Connect this terminal to terminal M of the HD61202.
Slave mode : Input terminal. Connect this terminal to terminal MB of the HD61830.</td></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61202</td><td>Shift clock
Master mode: Output terminal Connect this terminal to terminal CL of the HD61202.
Slave mode : Input terminal Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register.
DL corresponds to X1's side and DR to X64's side.
Master mode: Output common scanning signal. Don't connect any lines to these terminals normally.
Slave mode : Connect terminal FLM of the HD61830 to DL (when SHL=V_{CC}) or DR (when SHL=GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
</table>

(to be continued)

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don't connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table><tr><th>SHL</th><th>Shift direction</th><th>Common scanning direction</th></tr><tr><td>V_{CC}</td><td>DL ⟶ DR</td><td>X1 ⟶ X64</td></tr><tr><td>GND</td><td>DL ⟵ DR</td><td>X1 ⟵ X64</td></tr></table></td></tr>
<tr><td>X1~X64</td><td>64</td><td>O</td><td>Liquid crystal display</td><td>Liquid crystal display driver output.
Output one of the four liquid crystal display driver levels V1, V2, V5 and V6 with the combination of the data from the shift register and M signal.
 
Data "1" — Selected level
"0" — Non-selected level
When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64.
When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.</td></tr>
</table>

HD61203 Connection List

H...V_{CC} } Fixed
L...GND }

"-" means "open".

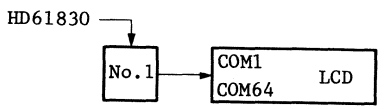
Rf...Oscillation resistor
Cf...Oscillation capacity

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	ϕ1	ϕ2	FRM	M	CL2	SHL	DL	DR	X1 ∿ X64
A	L	L	L	L	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	-	COM1 ∿COM64
																	L	-	from FLM of HD61830	COM64 ∿COM1
B	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61203 No.2	COM1 ∿COM64
																	L	to DL/DR of HD61203 No.2	from FLM of HD61830	COM64 ∿COM1
C	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61203 No.1	-	COM65 ∿COM128
																	L	-	from DL/DR of HD61203 No.1	COM128∿COM65
D	H	L	L	H	H	L L or L H		H	Rf Cf	Rf	Cf	to ϕ1 of HD61202	to ϕ2 of HD61202	to FRM of HD61202	to M of HD61202	to CL of HD61202	H	-	-	COM1 ∿COM64
																	L	-	-	COM64 ∿COM1
E	H	L	L	H	H	L L or L H		H	Rf Cf	Rf	Cf	to ϕ1 of HD61202	to ϕ2 of HD61202	to FRM of HD61202	to M of HD61202 HD61203	to CL of HD61202 to CL2 of HD61203	H	-	to DL/DR of HD61203 No.2	COM1 ∿COM64
																	L	to DL/DR of HD61203 No.2	-	COM64 ∿COM1
F	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from M of HD61203 No.1	from CL2 of HD61203 No.1	H	from DL/DR of HD61203 No.1	-	COM1 ∿COM64
																	L	-	from DL/DR of HD61203 No.1	COM64 ∿COM1

Outline of HD61203 System Configuration

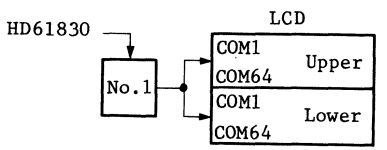
1) Use with HD61830

a) When display duty ratio of LCD is 1/64



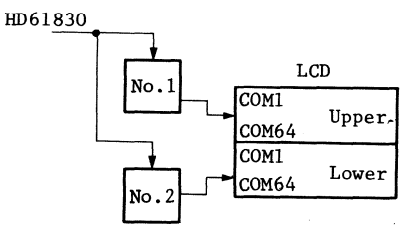
One HD61203 drives common signals.

Refer to Connection list 'A'



One HD61203 drives common signals for upper and lower panels.

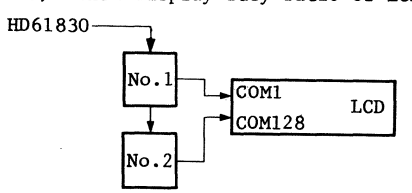
Refer to Connection list 'A'



Two HD61203's drive upper and lower panel separately to ensure the quality of display. No.1 and No.2 operate in parallel.

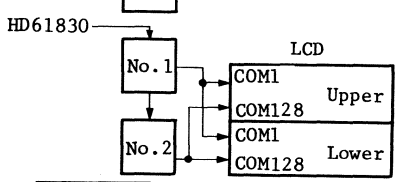
For both of No.1 and No.2, refer to Connection list 'A'

b) When display duty ratio of LCD is from 1/65 to 1/128



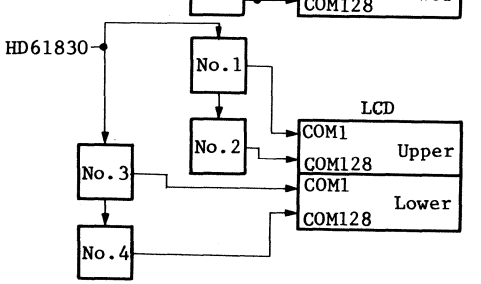
Two HD61203's connected serially drive common signals.

Refer to Connection list 'B' for No.1. Refer to Connection list 'C' for No.2.



Two HD61203 's connected serially drive upper and lower panels in parallel.

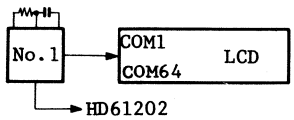
Refer to Connection list 'B' for No.1. Refer to Connection list 'C' for No.2.



Two sets of HD61203 's connected serially drive upper and lower panels in parallel to ensure the quality of display.

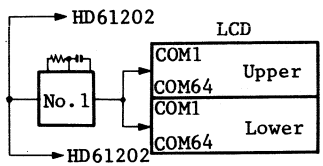
Refer to Connection list 'B' for No.1 and 3. Refer to Connection list 'C' for No.2 and 4.

2) Use with HD61202 (1/64 duty)



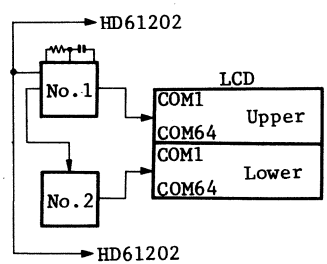
One HD61203 drives common signals and supplies timing signals to the HD61202's.

Refer to Connection list 'D'



One HD61203 drives upper and lower panels and supplies timing signals to the HD61202's.

Refer to Connection list 'D'



Two HD61203 's drive upper and lower panels in parallel to ensure the quality of display. No.1 supplies timing signals to No.2 and the HD61202's.

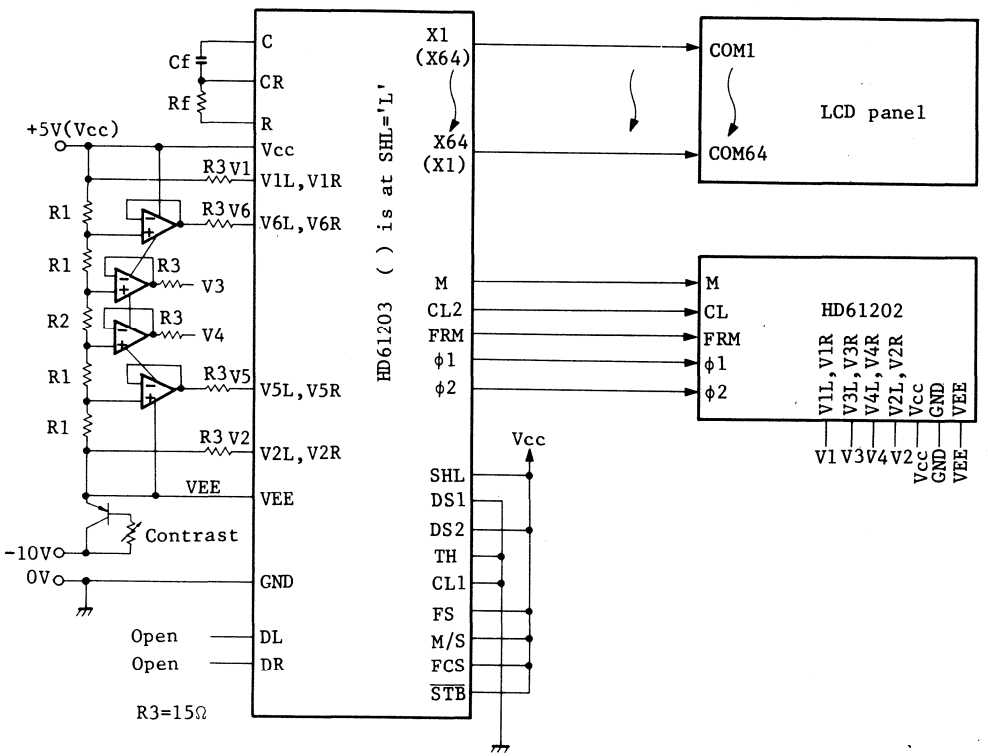
Refer to Connection list 'E' for No.1

Refer to Connection list 'F' for No.2

● Example of Connection 1)

(1) Use with HD61202 (RAM type segment driver)

a) 1/64 duty ratio (See Connection List "D")



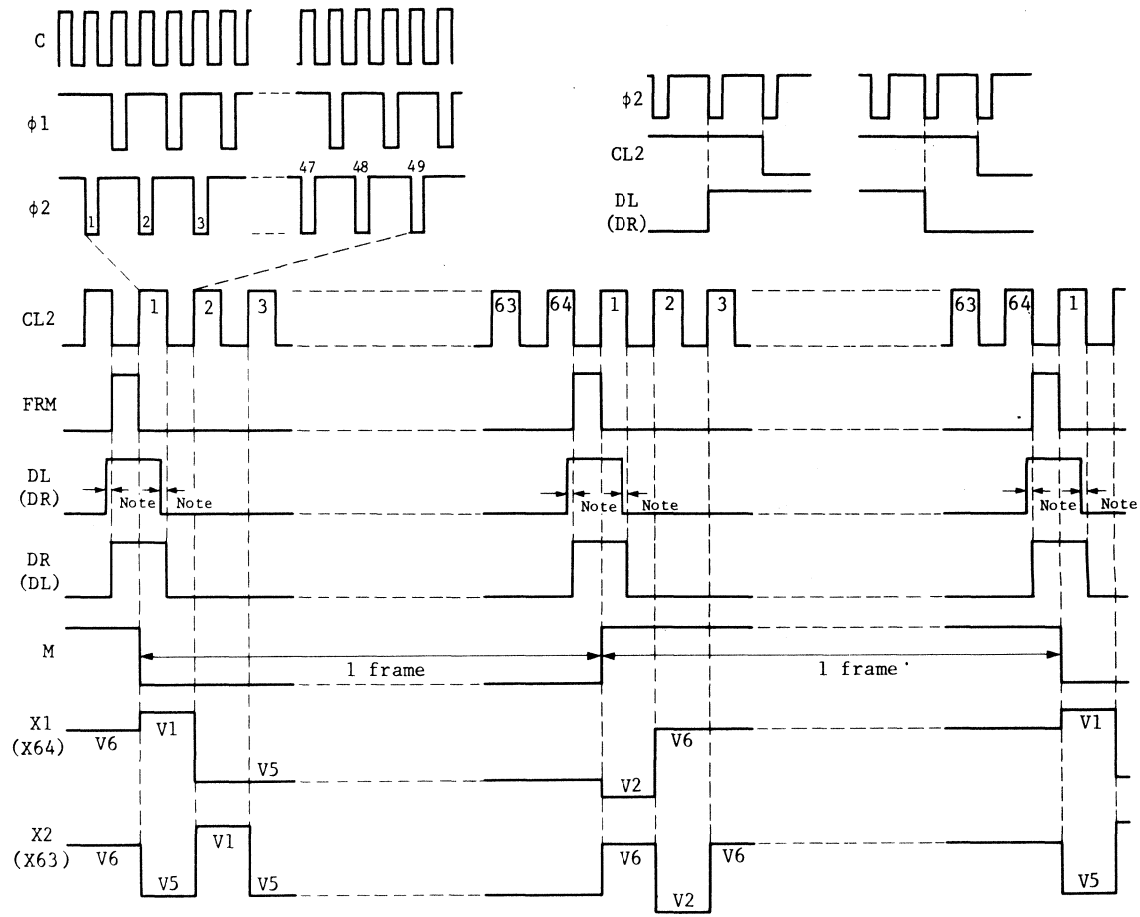
Note 1) The values of R1 and R2 vary with the LCD panel used. When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1=3kΩ, R2=15kΩ

Example of Waveform (RAM type, 1/64 duty)



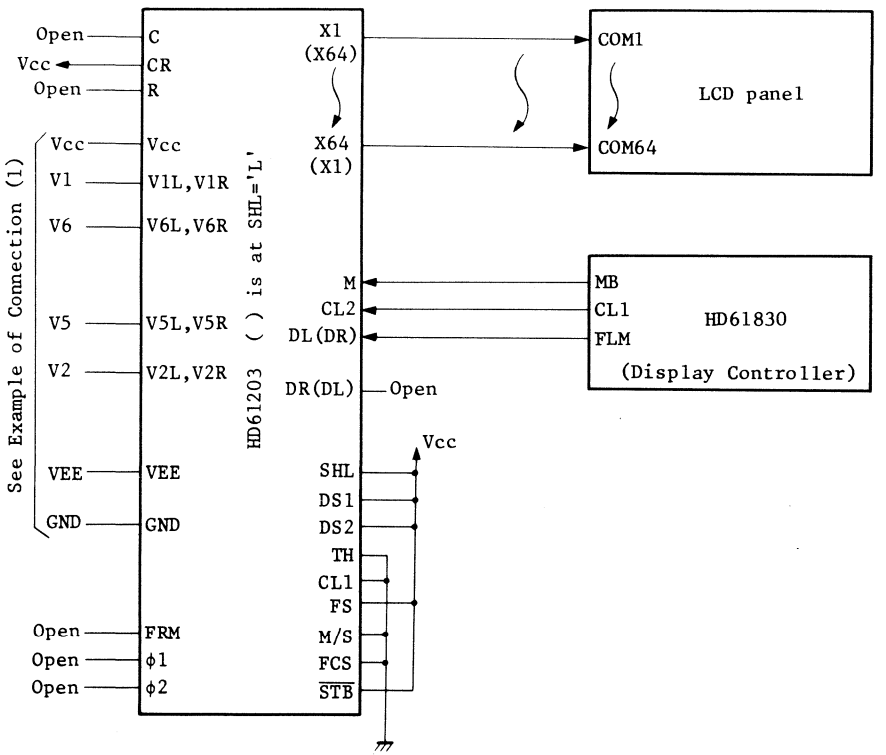
( ) ... at SHL='L'

Note) Phase difference between DL(DR) and CL2

Example of Connection 2)

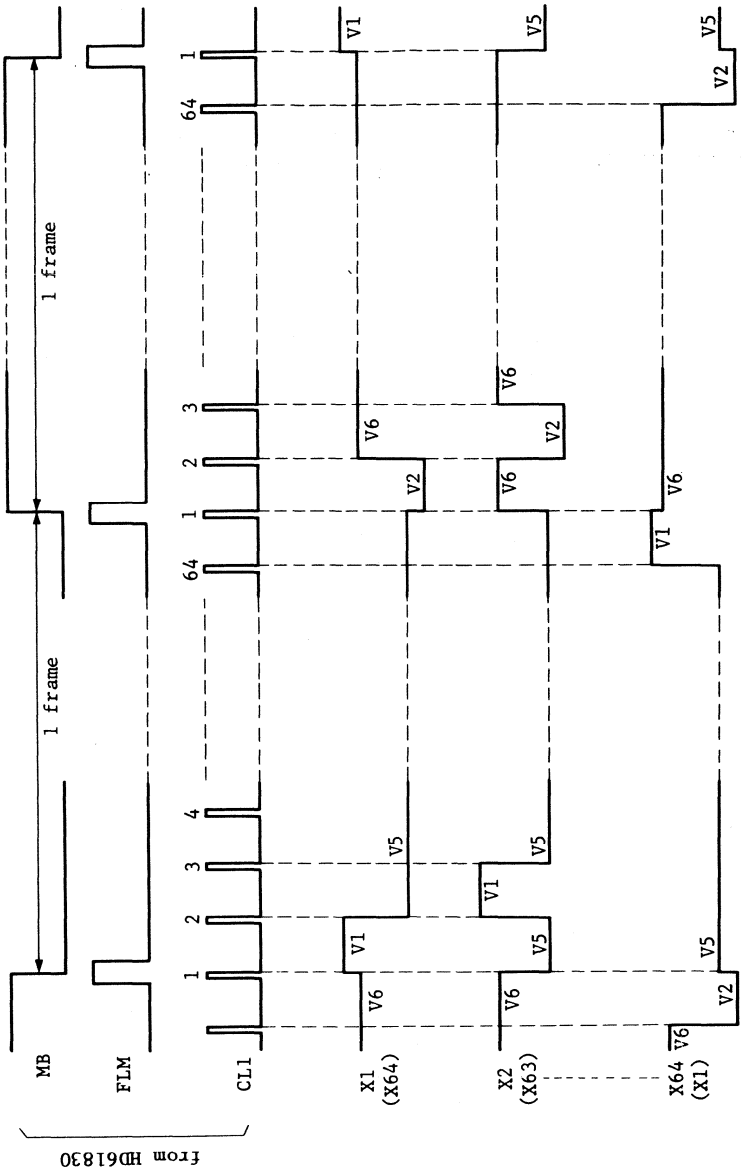
(2) Use with HD61830 (Display controller)

a) 1/64 duty ratio (See Connection List "A")

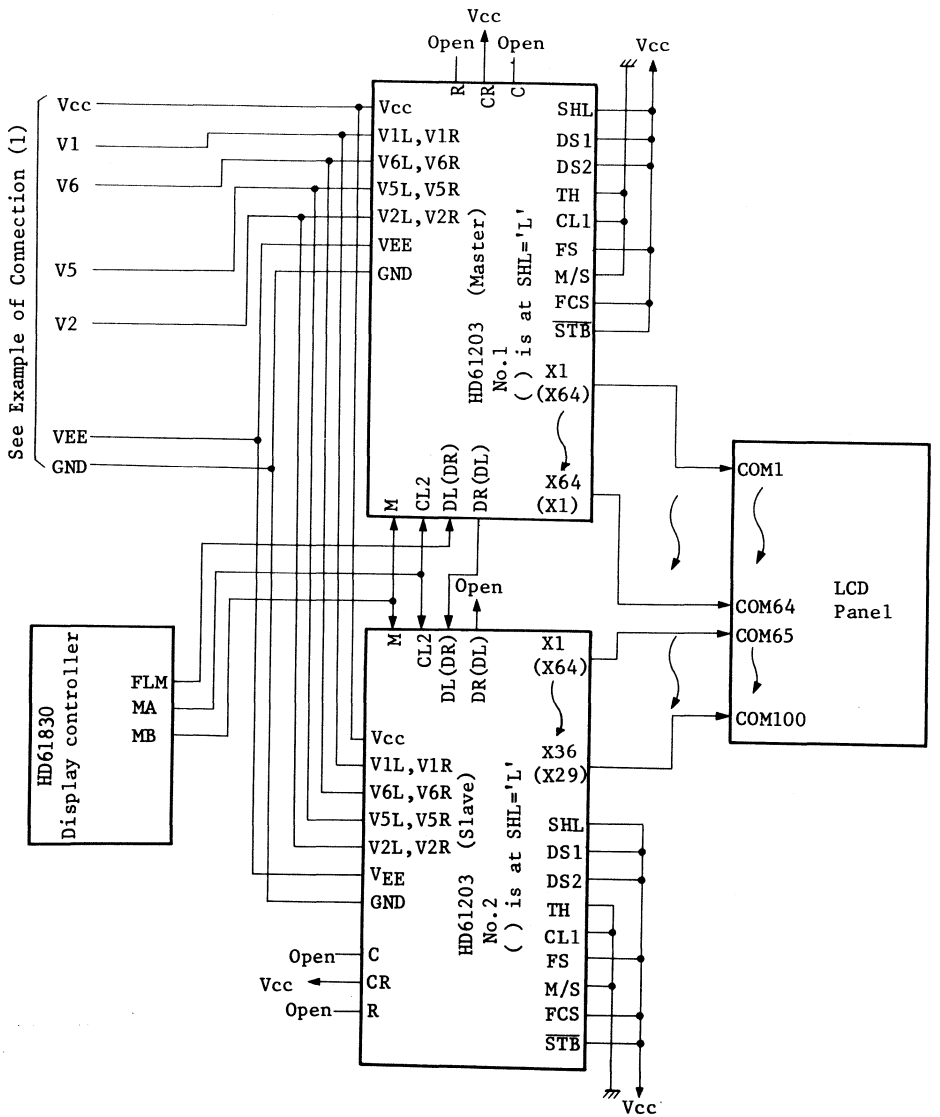


Example of Waveform

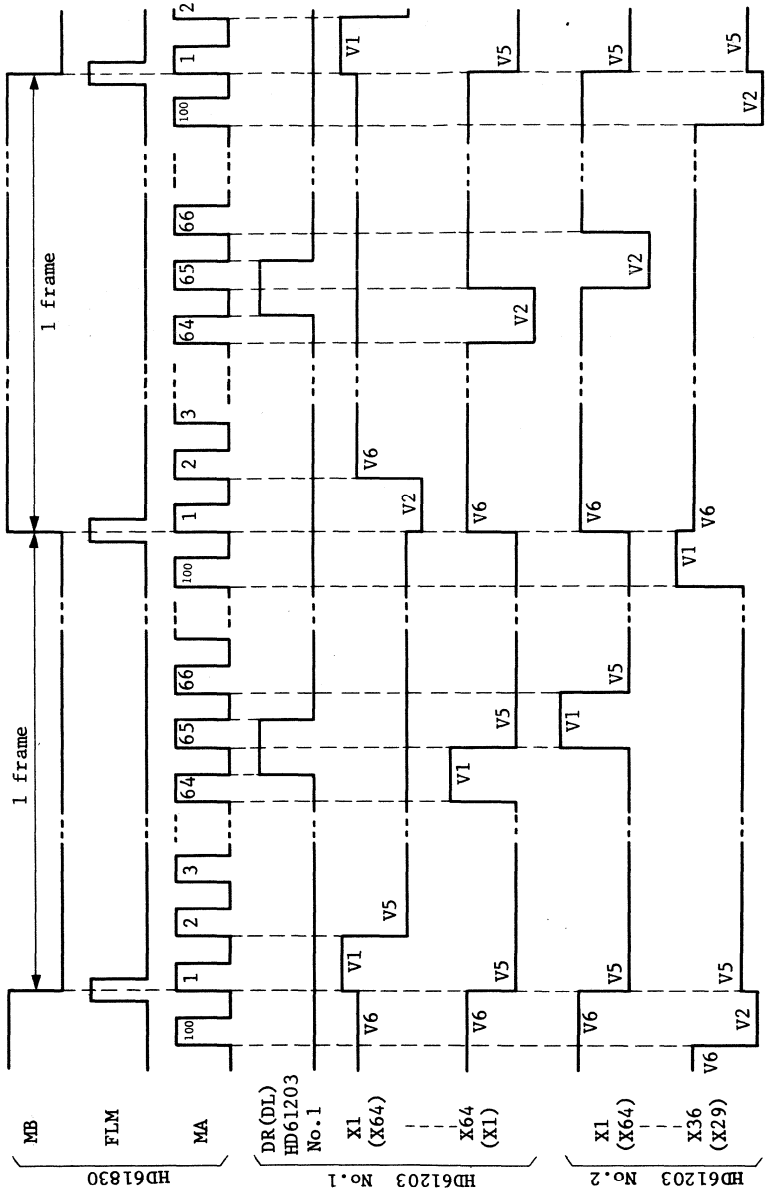
a) 1/64 duty ratio



b). 1/100 duty ratio (See Connection List 'B' 'C')

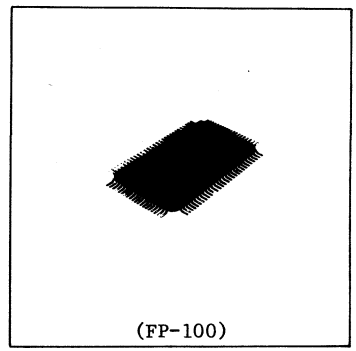


Example of Waveform b) 1/100 duty



HD61104, HD61104A
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

HD61104, HD61104A is a column (segment) driver for large-area dot matrix liquid crystal graphic display systems.



(FP-100)

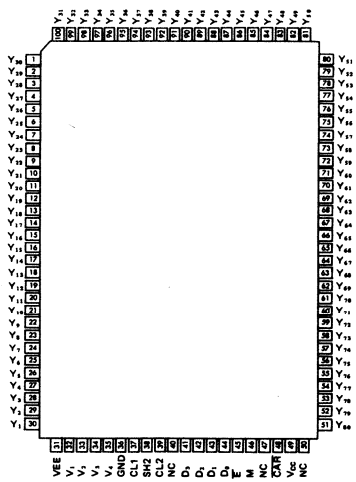
■ FEATURES

- Display duty 1/64 ∿ 1/200
- Internal liquid crystal display driver 80 drivers
- 4-bit bus, bi-directional shift data transfer
- Cascade connection with enable format
- Data transfer rate 3.5 MHz
- Power supply for logic circuit 5V ± 10%
- Power supply for LCD drive circuits:
  10 to 26V (HD61104)
  10 to 28V (HD61104A)
- Stand-by function
- CMOS process
- 100-pin flat plastic package

■ ORDERING INFORMATION

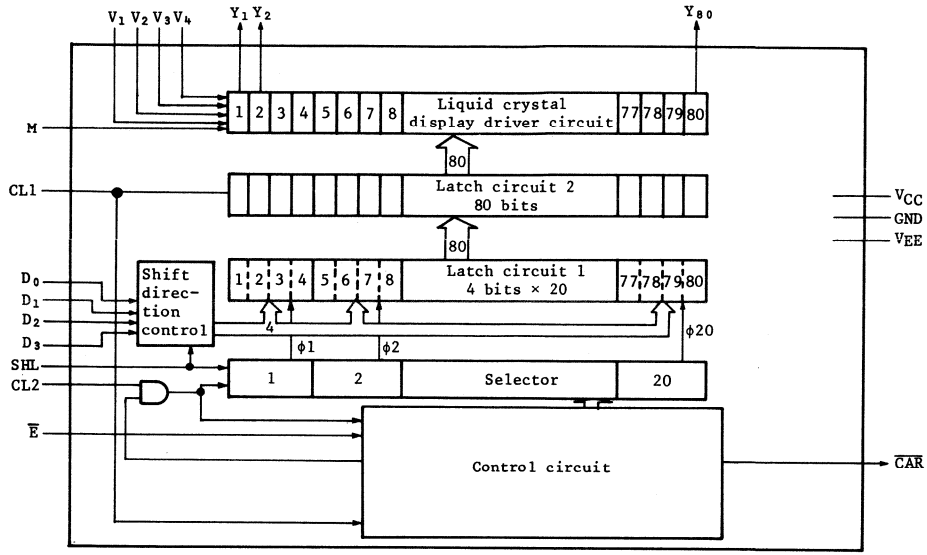
Type No.	LCD driving Level (V)	Package
HD61104	+10 to +26	100 pin plastic QFP (FP-100)
HD61104A	+10 to +28 V	

■ Pin Arrangement



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2)	HD61104	V_{EE}	V_{CC} - 28.0 to V_{CC} + 0.3	V	
	HD61104A	V_{EE}	V_{CC} - 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	-0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} - 0.3 to V_{CC} + 0.3	V	4
Operating temperature		Topr	-20 to +75	°C	
Storage temperature		Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND = 0V.

(Note 3) Applies to input terminals, SHL, CL1, CL2, D0 - D3, $\overline{E}$ and M.

(Note 4) Applies to V1, V2, V3 and V4. Must maintain

$$V_{CC} \geq V1 \geq V3 \geq V4 \geq V2 \geq V_{EE}$$

Connect a protection resistor of 15Ω ± 10% to each terminals in series.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, V_{CC} - V_{EE} = 10 to 26V (HD61104), V_{CC} - V_{EE} = 10 to 28 (HD61104A), Ta = -20 to +75°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input "High" voltage	V_{IH}		0.7×V_{CC}		V_{CC}	V	1
Input "Low" voltage	V_{IL}		0		0.3×V_{CC}	V	1
Output "High" Voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4			V	2
Output "Low" voltage	V_{OL}	I_{OL}=400μA			0.4	V	2
Driver ON Resistance	R_{ON}	V_{EE}=-10V, Load current= 100μA			7.5	kΩ	5
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1		1	μA	1
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-25		25	μA	3
Dissipation Current (1)	I_{GND}				2.0	mA	4
Dissipation Current (2)	I_{EE}	HD61104			0.2	mA	4
		HD61104A			0.4		
Dissipation Current (3)	I_{ST}				100	μA	4 5

(Note 1) Applies to CL1, CL2, SHL, $\overline{E}$, M, and D0 - D3.

(Note 2) Applies to $\overline{CAR}$.

(Note 3) Applies to V1, V2, V3 and V4.

(Note 4) Specified when display data is transferred under following conditions.

CL2 frequency fcp2 = 2.5 MHz (data transfer rate)

CL1 frequency fcp1 = 14.0 kHz (data latch frequency)

M frequency f_M = 35 Hz (frame frequency / 2)

Display duty ratio 1/200

Specified when V_{IH} = V_{CC}, V_{IL} = GND and no load on outputs.

I_{GND}: currents between V_{CC} and GND

IEE : currents between V_{CC} and V_{EE}

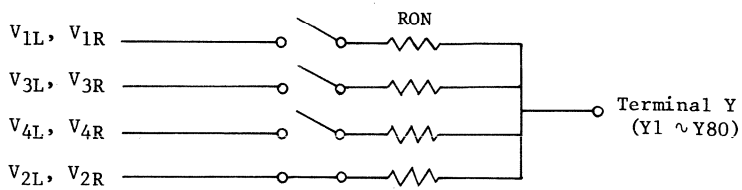
(Note 5) Currents between V_{CC} and GND at stand-by ($\overline{E}$ input = "H").

(Note 6) Resistance between terminal Y (one of Y1 to Y80) and terminal V (one of V1, V2, V3, and V4) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition.

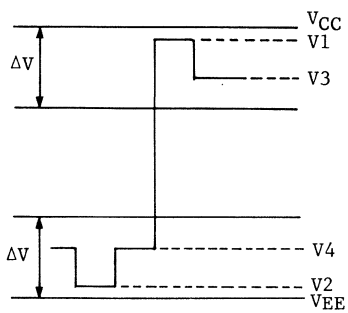
$V_{CC} - V_{EE} = 26V$

$V1, V3 = V_{CC} - 2/10\ (V_{CC} - V_{EE})$

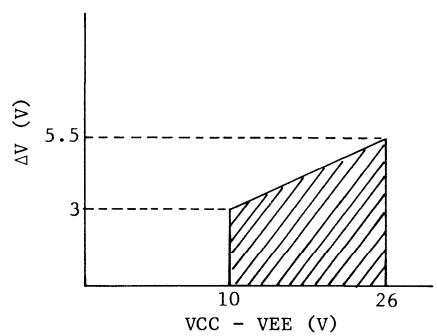
$V2, V4 = V_{EE} + 2/10\ (V_{CC} - V_{EE})$



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1, and V3, and negative voltage to V2 and V4, within the ΔV range respectively. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

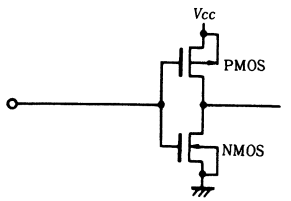


Correlation between Power Supply Voltage V_{CC}-V_{EE} and ΔV

■ Terminal Configuration

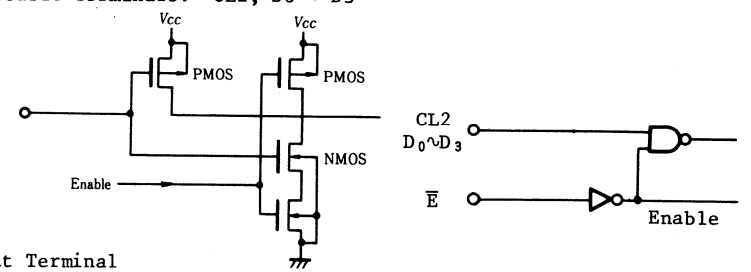
● Input Terminal

Applicable Terminals: CL1, SHL, $\overline{E}$, M



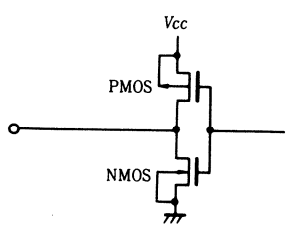
● Input Terminal (controlled by Enable signal)

Applicable Terminals: CL2, D0 ∿ D3



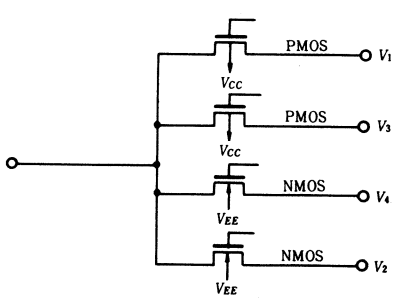
● Output Terminal

Applicable Terminal: $\overline{CAR}$



● Output Terminal

Applicable Terminals: Y1 ∿ Y80

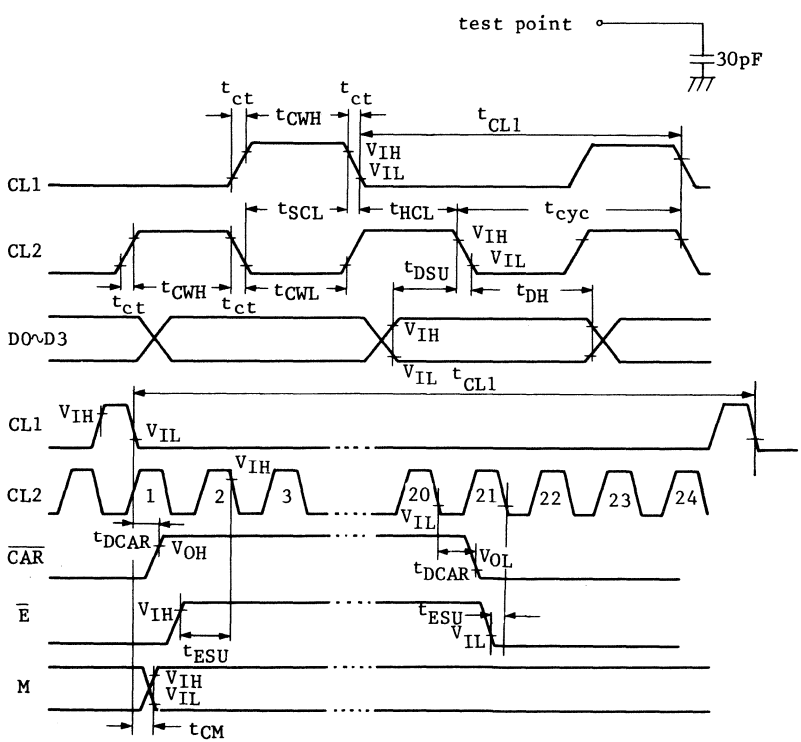


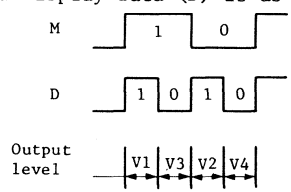
- AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, Ta = -20 to +75°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Clock cycle time	tCYC		285			ns	
Clock high level width	tCWH		110			ns	
Clock low level width	tCWL		110			ns	
Clock setup time	tSCL		80			ns	
Clock hold time	tHCL		80			ns	
Clock rise/fall time	tCT				30	ns	
Data setup time	tDSU		80			ns	
Data hold time	tDH		80			ns	
E setup time	tESU		75			ns	
Output delay time	tDCAR				180	ns	1
M phase difference time	tCM				300	ns	
CL1 cycle time	tCL1		tCYC × 10			ns	

Note 1) The following load circuits are connected for specification:



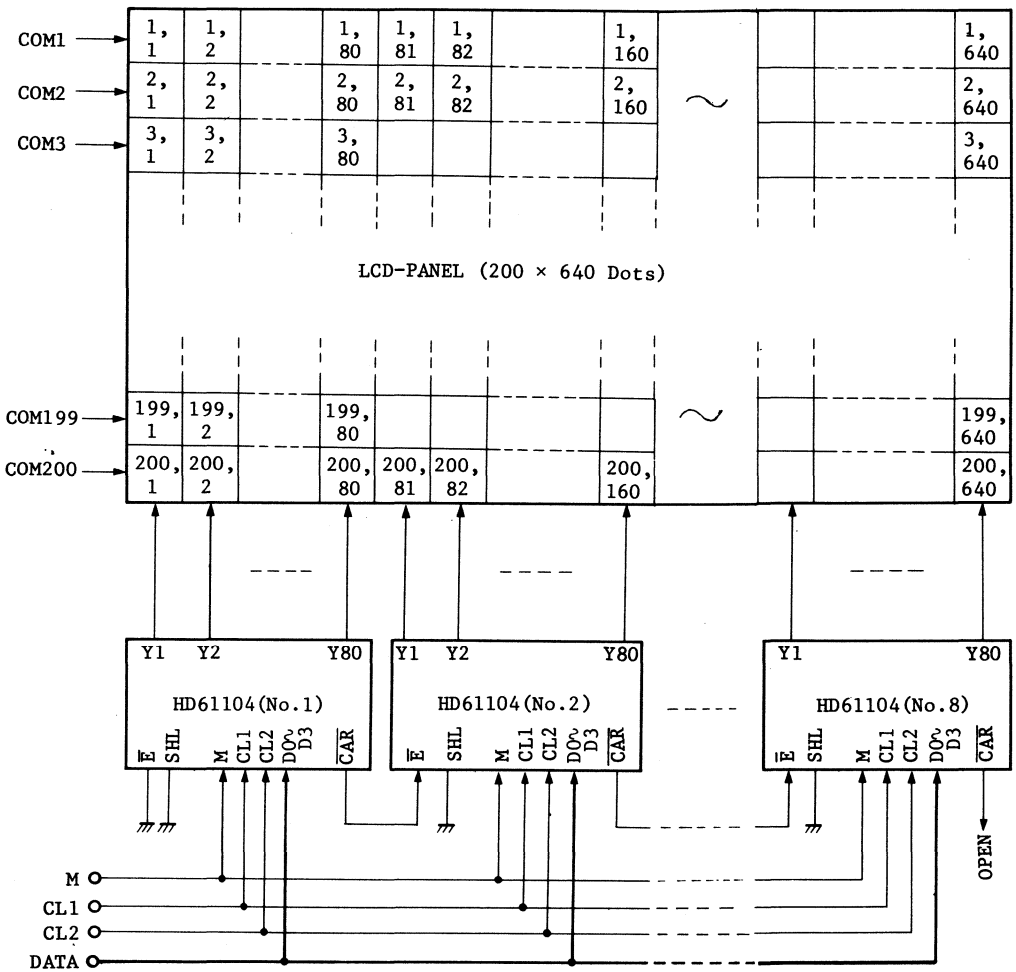
Terminal name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} - GND: Power supply for internal logic V_{CC} - V_{EE}: Power supply for LCD drive circuit
V1 V2 V3 V4	4		Power supply	Power supply for liquid crystal drive V1, V2 --- selection level V3, V4 --- non-selection level
Y1∿Y80	80	O	LCD	Liquid crystal driver outputs Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M, and display data (D) is as follows. 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger) Synchronizing with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D) Fall edge trigger

-to be continued

<table>
<tr><th>Terminal name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>D0∿D3</td><td>4</td><td>I</td><td>Controller</td><td>Input of 4-bit display data (D)
<table>
<tr><td colspan="2">(D)</td><td>Liquid Crystal driver output</td><td>Liquid crystal display</td></tr>
<tr><td colspan="2">1 ("H" level)</td><td>Selection level</td><td>ON</td></tr>
<tr><td colspan="2">0 ("L" level)</td><td>Non-selection level</td><td>OFF</td></tr>
<tr><td colspan="4">Truth table Positive logic</td></tr>
<tr><td>SHL</td><td colspan="3">Input data and latch circuit 1</td></tr>
<tr><td rowspan="4">0</td><td colspan="3">D3 → 1 → 5 → 9 --- → 73 → 77</td></tr>
<tr><td colspan="3">D2 → 2 → 6 → 10 --- → 74 → 78</td></tr>
<tr><td colspan="3">D1 → 3 → 7 → 11 --- → 75 → 79</td></tr>
<tr><td colspan="3">D0 → 4 → 8 → 12 --- → 76 → 80</td></tr>
<tr><td rowspan="4">1</td><td colspan="3">D3 → 80 → 76 → 72 --- → 8 → 4</td></tr>
<tr><td colspan="3">D2 → 79 → 75 → 71 --- → 7 → 3</td></tr>
<tr><td colspan="3">D1 → 78 → 74 → 70 --- → 6 → 2</td></tr>
<tr><td colspan="3">D0 → 77 → 73 → 69 --- → 5 → 1</td></tr>
<tr><td colspan="4">ex.) When SHL="0", the data which is input to D3 is latched to each bit of the latch circuit 1 in order of 1 → 5 → 9 --- → 77.</td></tr>
</table></td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of display data.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61104</td><td>Enable input
The operation stops with "H" level, and enables at "L" level.</td></tr>
<tr><td>$\overline{CAR}$</td><td>1</td><td>0</td><td>the input terminal $\overline{E}$ of the HD61104</td><td>Enable output
Used for cascade connection.</td></tr>
<tr><td>NC</td><td>3</td><td></td><td></td><td>Unused. No wire is to be connected.</td></tr>
</table>

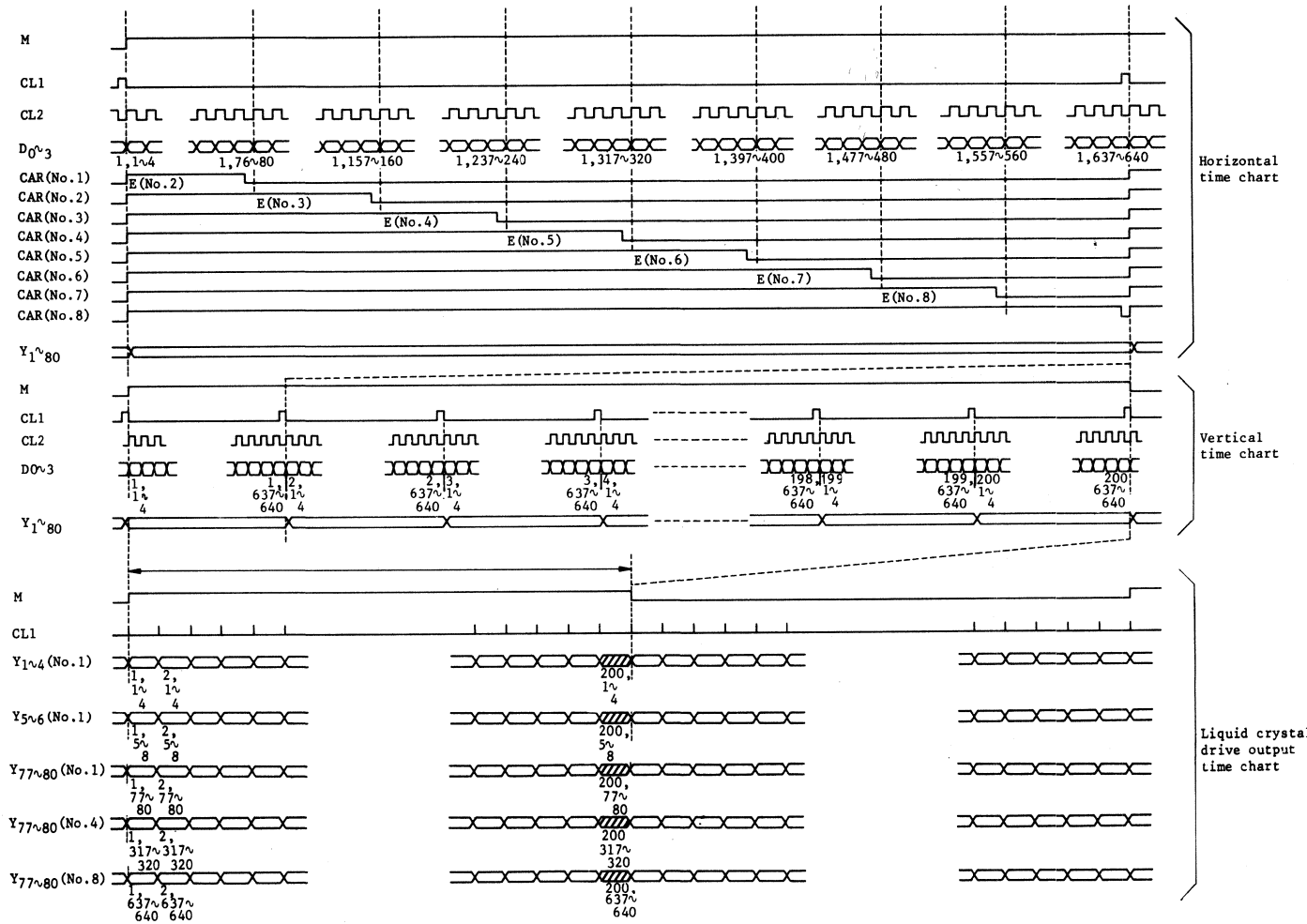
■TYPICAL APPLICATION

The following is the LCD panel with 200 × 640 dots on which characters are displayed with 1/200 duty dynamic drive.



Cascade eight HD61104's. Input data to the terminal D0∿D3 of No.1∿No.8. Connect $\overline{E}$ of No.1 to GND. No lines to be connected to $\overline{CAR}$ of No.8 Connect common signal terminals (COM1∿COM200) to the common driver HD61105. (m,n) of LCD panel is the address corresponding to each dot.

Example of Waveform



HD66106F

(LCD Driver for High Voltage)

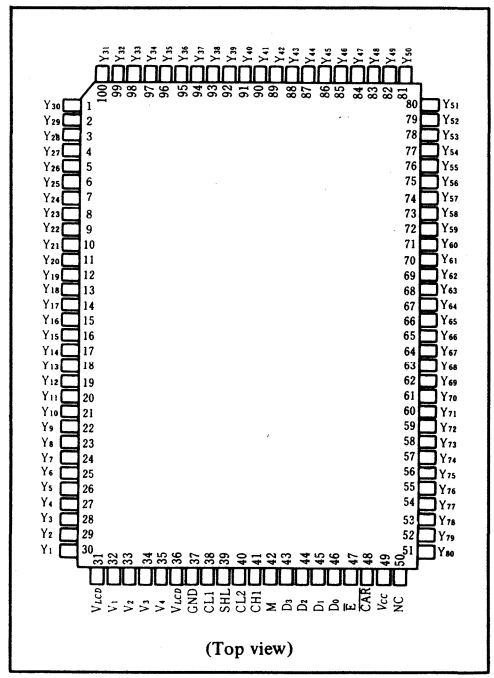
Description

The HD66106F LCD driver has a high duty ratio and many outputs for driving a large capacity dot matrix LCD panel.
It includes 80 LCD drive circuits and can drive up to 1/480 duty. For example, only 14 drivers are enough to drive an LCD panel of 640 × 480 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator.
Using this LSI sharply lowers the cost of an LCD system.

Features

- Column and row driver
- 80 LCD drive circuits
- Multiplexing duty ratio: 1/100 to 1/480
- 4-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby function
- Recommended LCD controller LSI's: HD63645 and HD64645 (LCTC)
- Power supply: +5 V ± 10% for the internal logic, and 14.0 V to 37.0 V for LCD drive circuits
- Operation frequency: 6.0 MHz (max.)
- CMOS process
- 100-pin flat plastic package (FP-100)

Pin Arrangement



(Top view)

Pin Description

Power supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1-V_4 supply power for driving LCD (figure 1).

Control signals

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_3: D_0-D_3 input display data for the column driver (table 2).

Table 1. Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	49	V_{CC}	I
GND	37	Ground	I
V_{LCD}	31, 36	V_{LCD}	I
V_1	32	LCD voltage 1	I
V_2	33	V_2 LCD voltage 2	I
V_3	34	V_3 LCD voltage 3	I
V_4	35	V_4 LCD voltage 4	I
CL1	38	Clock 1	I
CL2	40	Clock 2	I
M	42	M	I
D_0-D_3	46-43	Data 0 to data 3	I
SHL	39	Shift left	I
$\overline{E}$	47	Enable	I
$\overline{CAR}$	48	Carry	O
CH1	41	Channel 1	I
Y_1-Y_{80}	30-1, 100-51	Drive outputs 1-80	O
NC	50	No connection	–

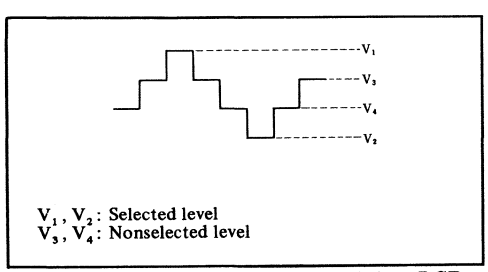


Figure 1. Power Supply for Driving LCD

Table 2. Relation between Display Data and LCD State

Display Data	LCD Outputs	LCD
1 (= high level)	Selected level	On
0 (= low level)	Nonselected level	Off

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, E connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). $\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip drives columns when CH1 = V_{CC}, and rows when CH1 = GND.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 3).

NC: NC is not used. Do not connect any wire.

Table 3. Relation between SHL and Scan Direction of Selected Line (When LSI is Used as a Row Driver)

SHL	Shift Direction of Shift Register				Scan Direction of Selected Line				
V_{CC}	$\overline{E}$	→ 1	→ 2	→ 3 ----------→ 80	Y_1	→ Y_2	→ Y_3	----------→	Y_{80}
GND	$\overline{E}$	→ 80	→ 79	→ 78 ----------→ 1	Y_{80}	→ Y_{79}	→ Y_{78}	----------→	Y_1

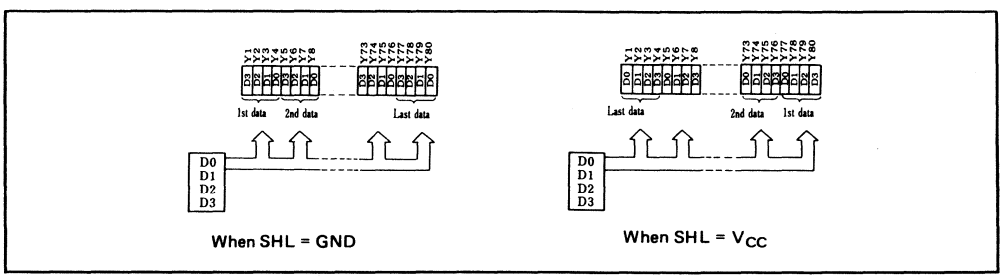


Figure 2. Relation between SHL and Data Output (When LSI is Used as a Column Driver)

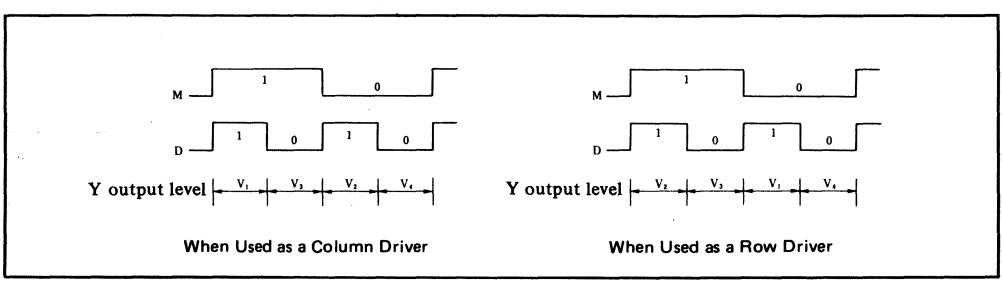


Figure 3. Selection of LCD Drive Output Level

Internal Block Diagram

LCD Drive Circuits

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Latch Circuit 2

When the LSI is used as a column driver, latch circuit 2 functions as an 80-bit latch circuit. It latches the data sent from latch circuit 1 at the fall of CL1 and transfers its outputs to the LCD drive circuits.
When the LSI is used as a row driver, this circuit functions as an 80-bit bidirectional shift register. The data sent from the $\overline{E}$ pin shifts at the fall of CL2. When SHL = V_{CC}, the data shifts from bit 1 to bit 80 in order of entry. When SHL = GND, the data shifts from bit 80 to bit 1.

Latch Circuit 1

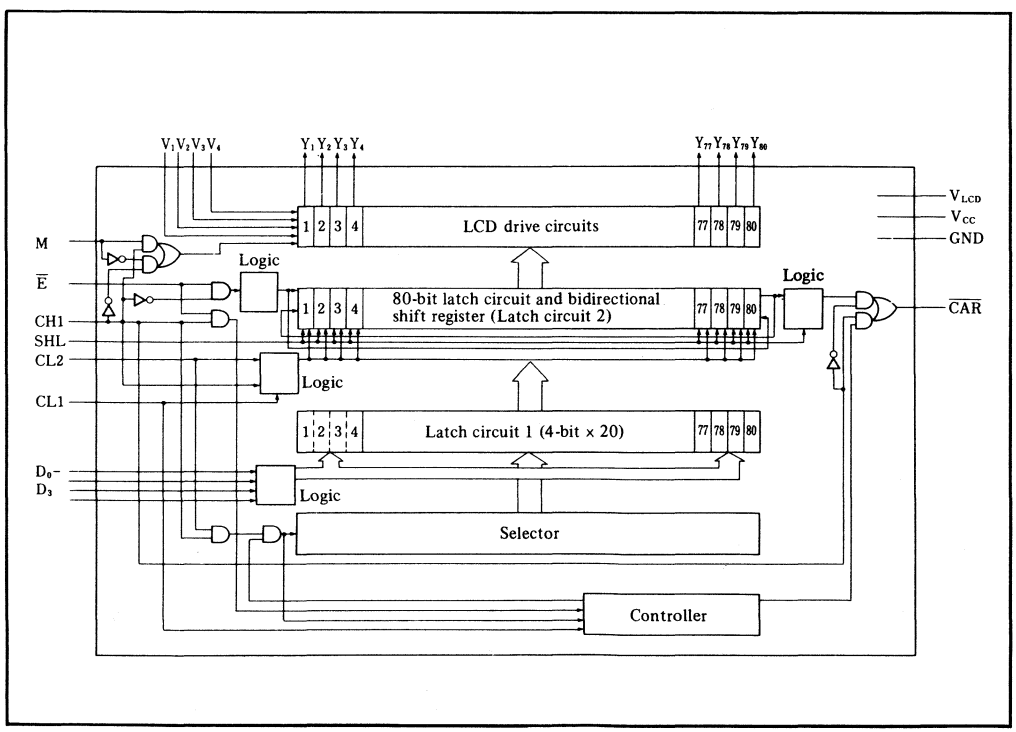
Latch circuit 1 is composed of twenty 4-bit parallel data latches. It latches the display data D_0-D_3 at the fall of CL2 when the LSI is used as a column driver. The signals sent from the selector determine which 4-bit latch should latch the data.

Selector

The selector is composed of a 5-bit up and down counter and a decoder. When the LSI is used as a column driver, it generates the latch signal to be sent to latch circuit 1, incrementing the counter at the negative edge of CL2.

Controller

The controller operates when the LSI is used as a column driver. It stops data latching when twenty pulses of CL2 have been input (= power-down function) and automatically generates the chip enable signal announcing the start of data latching into the next LSI.



Functional Description

When Used as a Column Driver

The HD66106F begins latching data when E goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (standby state) when it has latched 80 bits.

Data outputs change at the fall of CL1. Latched data d_1 is transferred to the output pin Y_1 and d_{80} to Y_{80} when SHL = GND. Conversely, d_{80} is transferred to Y_1 and d_1 to Y_{80} when SHL = V_{CC}. The output level is selected out of V_1-V_4 according to the combination of display data and the alternating signal M (figure 4).

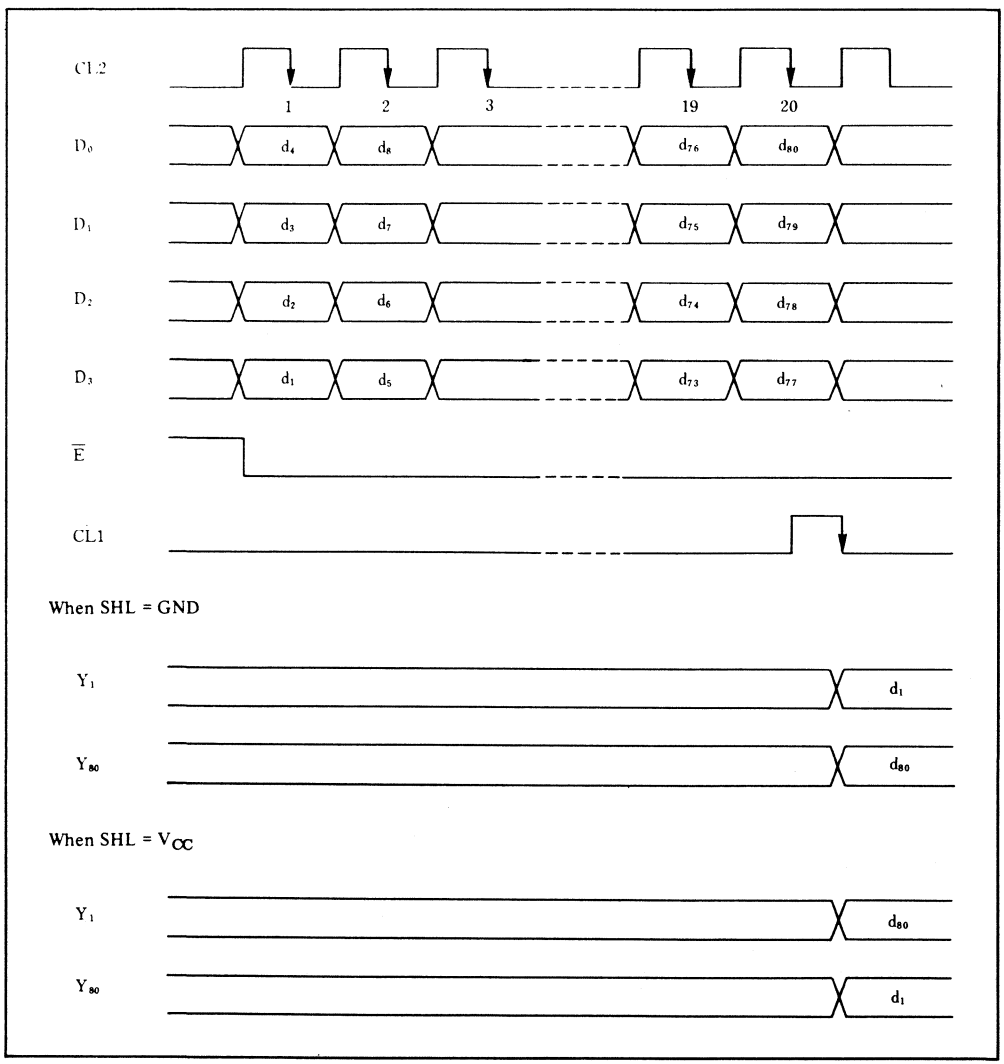


Figure 4. Column Driver Timing Chart

When Used as a Row Driver

The HD66106F shifts the line scan data sent from the pin $\overline{E}$ in order at the fall of CL2. When SHL = V_{CC}, data is shifted from Y_1 to Y_{80} and Y_{80} to Y_1 when SHL = GND.
In both cases, the data delayed for 80 bits by the shift register is output from the $\overline{CAR}$ pin to become the line scan data for the next LSI.

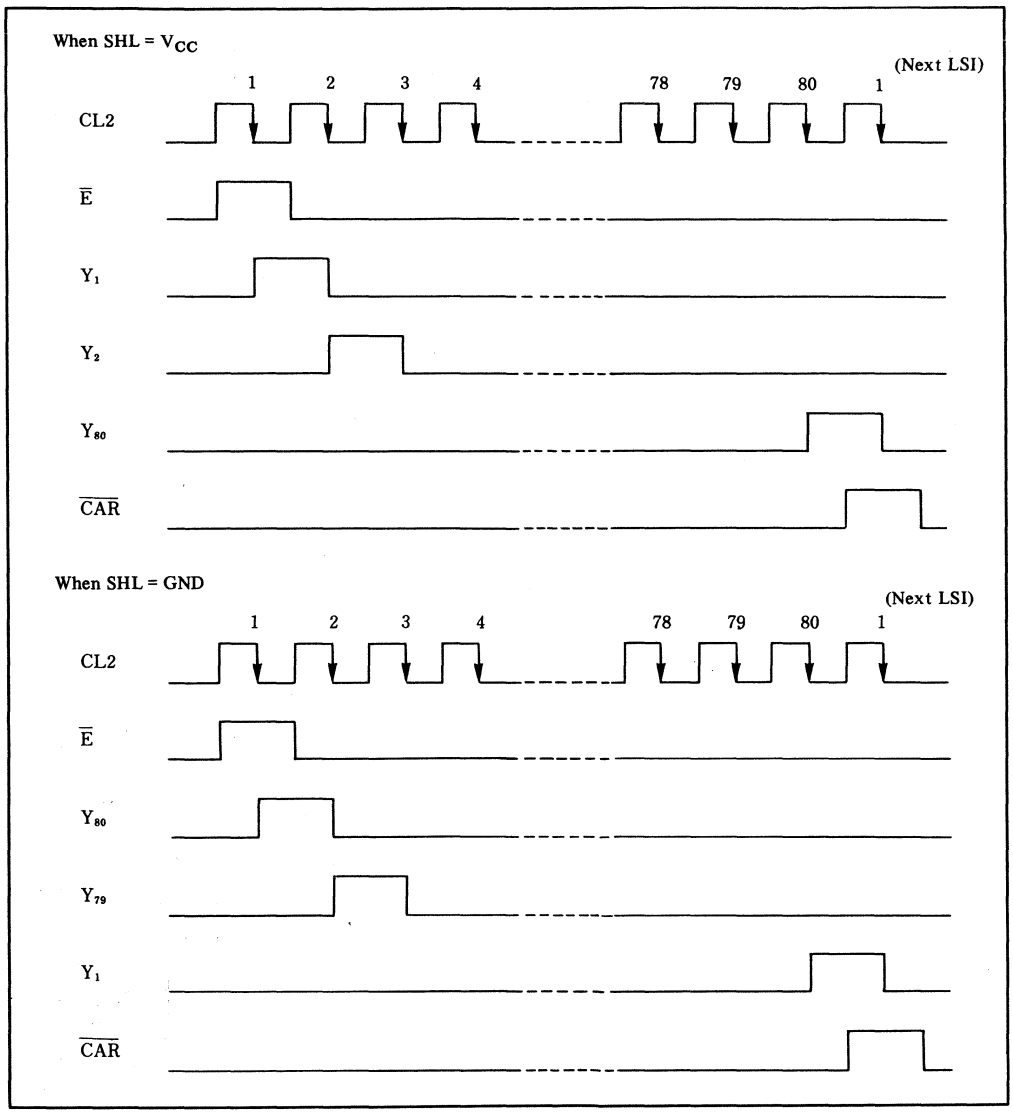


Figure 5. Row Driver Timing Chart

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 6). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 7).

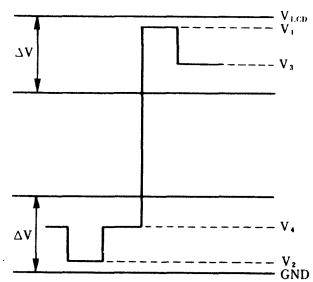


Figure 6. Driver's Output Waveform and Each Level of Voltage

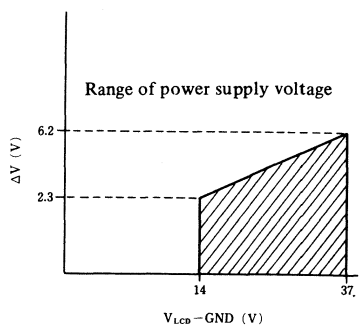
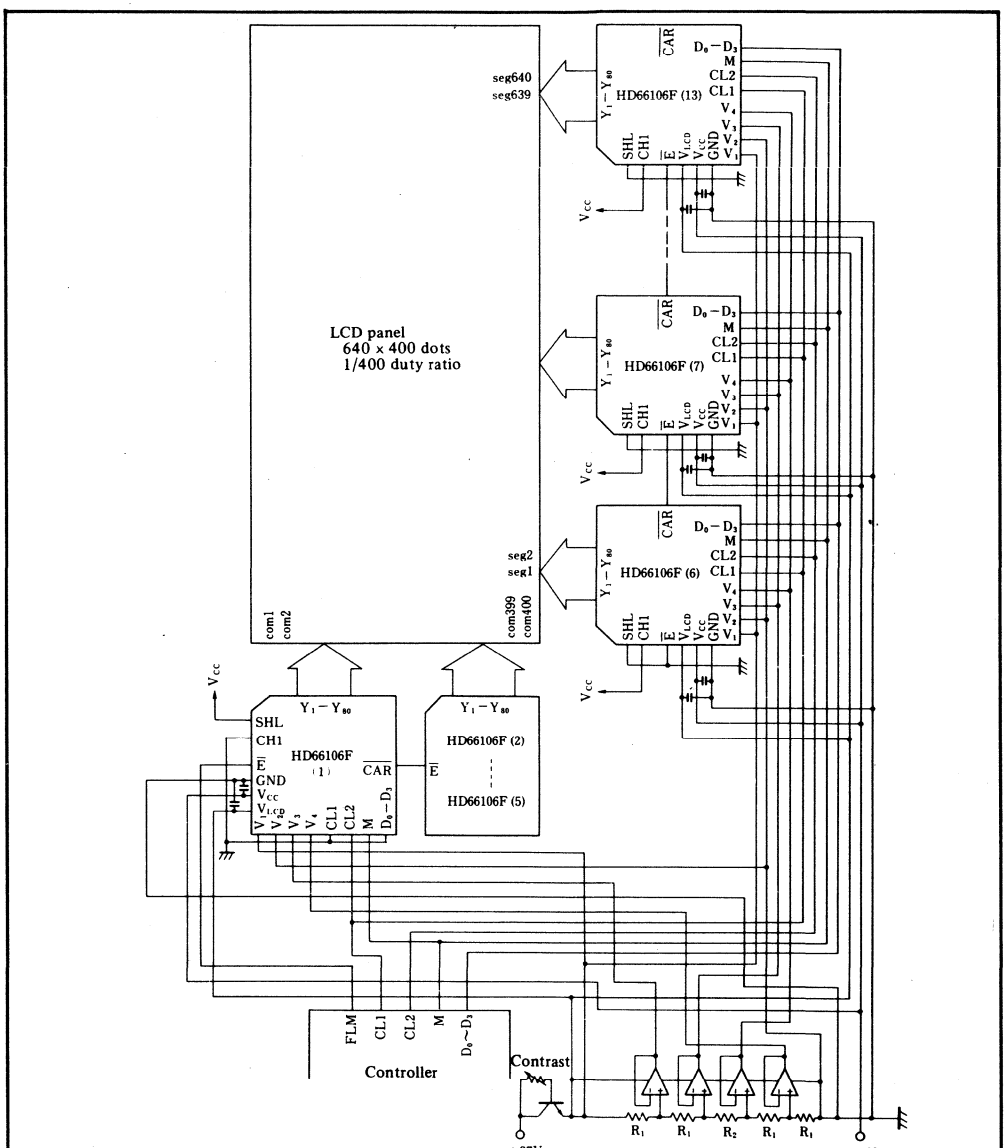


Figure 7. Power Supply Voltage V_{LCD}-GND and ΔV

Application Example

Application Diagram

Figure 8 shows an example of an LCD panel of 640 x 400 dots driven by HD66106Fs.



Notes:
1. R_1 and R_2 depend on the LCD panel in use. When using an LCD panel with 1/20 bias, $R_1/(4R_1 + R_2)$ should be 1/20. For example, R_1 -3 kΩ and R_2 -48 kΩ.
2. Use bypass capacitors to stabilize power supply when designing a board. It is desirable to use two capacitors with some 0.1 μF per LSI, putting one between V_{LCD} and GND, and the other between V_{CC} and GND.

Figure 8. Application Example

Timing waveform example

Figures 9 and 10 show the timing waveforms of the application example shown in figure 8.

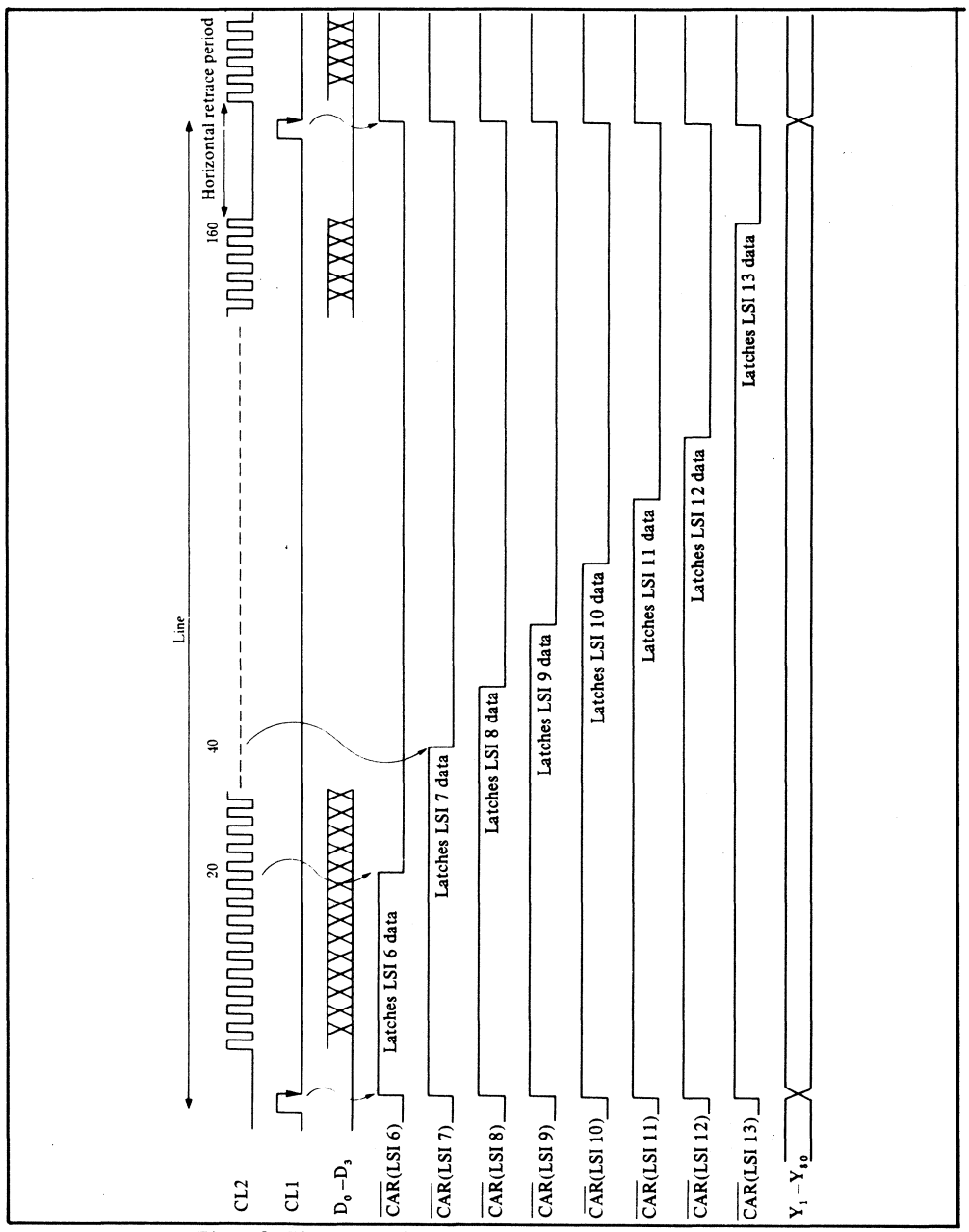


Figure 9. Timing Waveform for Column Drivers (LSI 6-LSI 13)

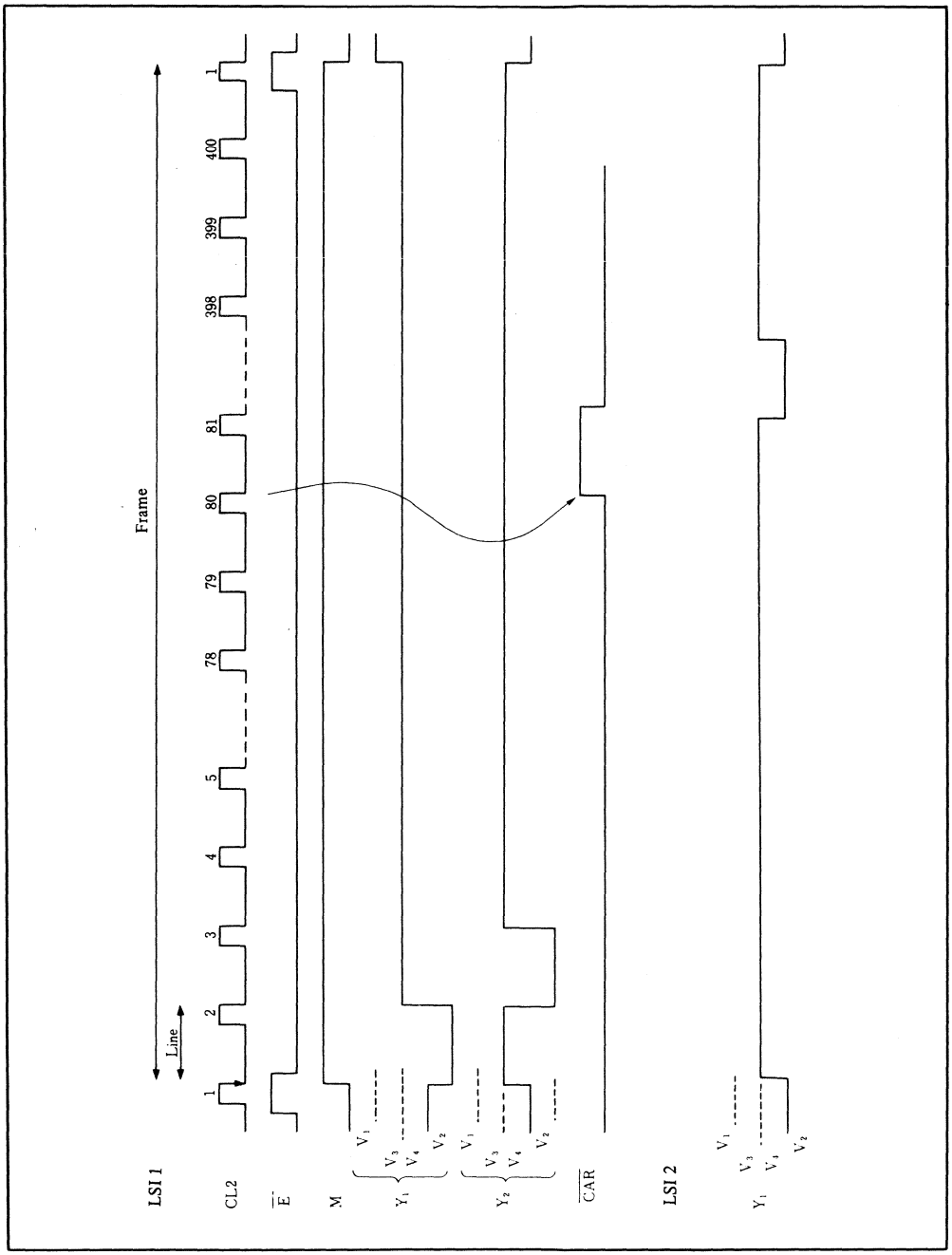


Figure 10. Timing Waveform for Row Drivers (LSI 1-LSI 5)

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Supply Voltage	Logic circuits	V_{CC}	−0.3 to +7.0	V	1
	LCD drive circuits	V_{LCD}	−0.3 to +38	V	1
Input voltage (Logic)		V_{T1}	−0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (LCD drive)		V_{T2}	−0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	−20 to +75	°C	
Storage temperature		T_{stg}	−55 to +125	°C	

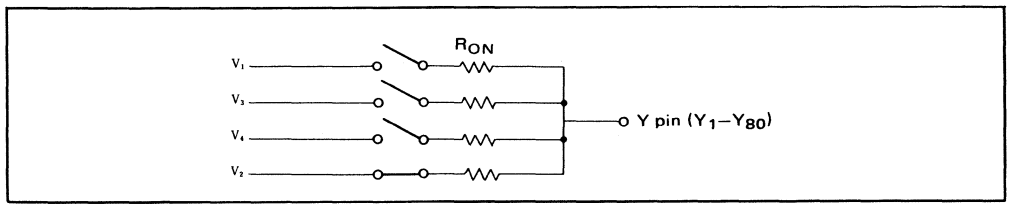
Notes: 1. Reference point is GND (= 0 V).
2. Applies to the input pins for logic circuits.
3. Applies to the input pins for LCD drive circuits.
4. Using an LSI beyond its maximum rating may result in its permanent destruction. LSIs should usually be used under electrical characteristics for normal operations. Exceeding any of these limits may adversely affect reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = −20°C to 75°C unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL,	0.8xVcc	–	Vcc	V		
Input low voltage	V_{IL}	D_0–D_3, $\overline{E}$, CH1	0	–	0.2xV_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC}−0.4	–	–	V	I_{OH}=−0.4 mA	
Output low voltage	V_{OL}		–	–	0.4	V	I_{OL}=0.4 mA	
Vi-Yj on resistance	R_{ON}	Y_1–Y_{80}, V_1–V_4	–	–	3.0	kΩ	I_{ON}=100 μA	4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	−5.0	–	5.0	μA	V_{IN}=V_{CC} to GND	
Input leakage current (2)	I_{IL2}	V_1–V_4	−50.0	–	50.0	μA	V_{IN}=V_{LCD} to GND	
Current consumption (1)	I_{CC1}		–	–	3.0	mA	f_{CL2}=6 MHz,	
(2)	I_{LCD1}		–	–	0.5	mA	f_{CL1}=28 kHz	1
(3)	I_{ST}		–	–	0.2	mA	At the standby state f_{CL2}=6 MHz, f_{CL1}=28 kHz	2
(4)	I_{CC2}		–	–	0.2	mA	f_{CL1}=28 kHz,	1
(5)	I_{LCD2}		–	–	0.1	mA	f_m=35 Hz	3

Notes: 1. Input and output current is excluded. When the input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit. V_{IH} and V_{IL} must be fixed at V_{CC} and GND respectively to avoid it.
2. Applies when the LSI is used as a column driver.
3. Applies when the LSI is used as a row driver.
4. Indicates the resistance between Y pin and V pin (one of V_1, V_2, V_3, and V_4) when it supplies load current to one of Y_1–Y_{80} pins.
Conditions: V_{LCD}–GND=37 V
V_1, V_3=V_{LCD}–2/20 (V_{LCD}–GND)
V_2, V_4=GND+2/20 (V_{LCD}–GND)



AC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to +75°C unless otherwise noted)

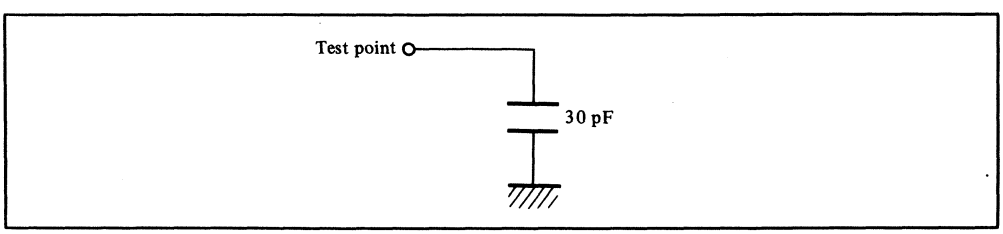
Column Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{cyc}	CL2	166	–	–	ns	
Clock high level width	t_{CWH}	CL2	50	–	–	ns	
Clock low level width	t_{CWL}	CL2	50	–	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	–	ns	
Clock rise/fall time	t_{ct}	CL1, CL2	–	–	30	ns	
Data setup time	t_{DSU}	D_0–D_3	30	–	–	ns	
Data hold time	t_{DH}	D_0–D_3	30	–	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	50	–	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	–	80	ns	1
M phase difference	t_{CM}	M, CL1	–	–	300	ns	

Row Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock low level width	t_{WL1}	CL2	5	–	–	μs	
Clock high level width	t_{WH1}	CL2	125	–	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	–	3	μs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	–	ns	1
Clock rise/fall time	t_{ct}	CL2	–	–	30	ns	

Note: 1. Values when the following load circuit is connected:



Column Driver

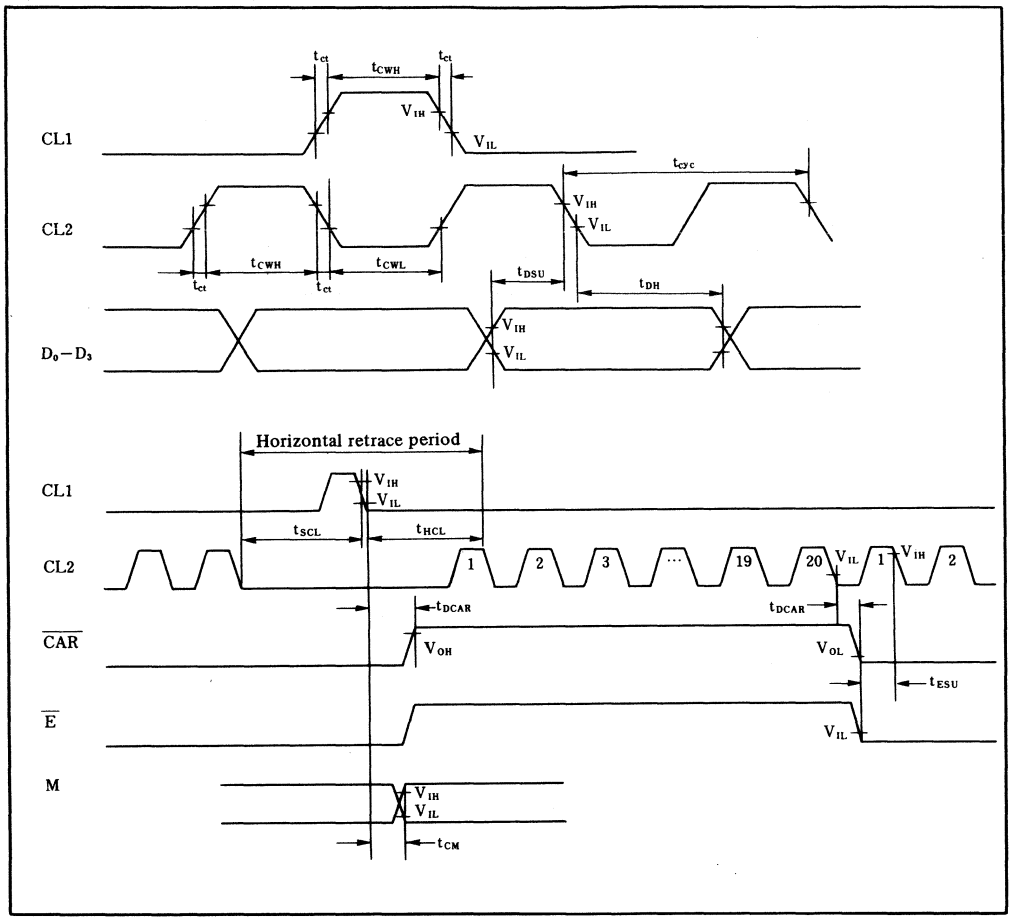


Figure 11. Controller Interface of Column Driver

Row Driver

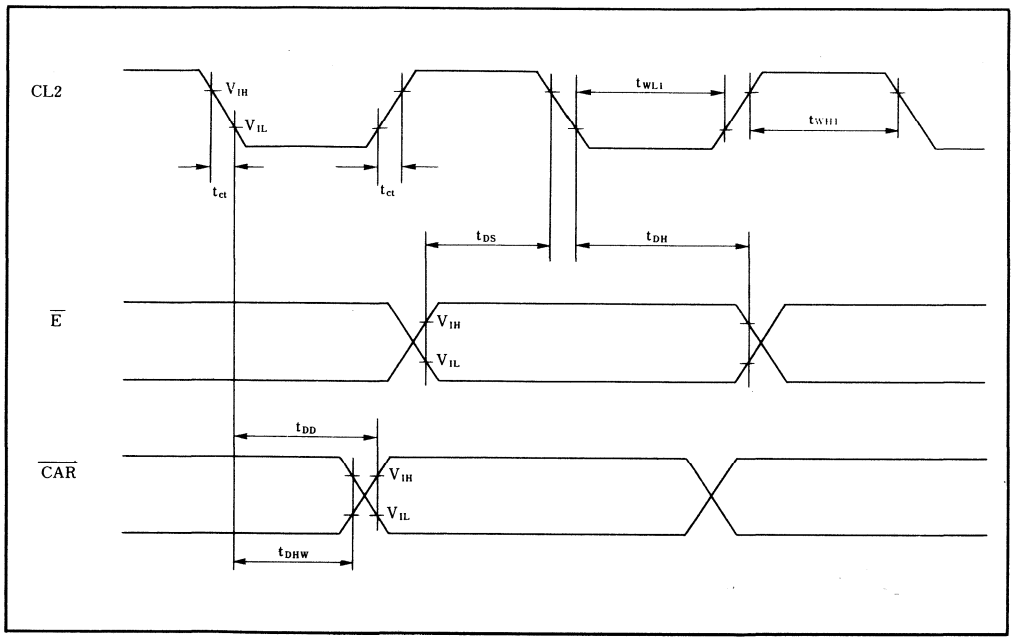


Figure 12. Controller Interface of Row Driver

HD66107T
(LCD Driver for High Voltage)

Description

The HD66107T is a multi-output, high duty ratio LCD driver used for large capacity dot matrix LCD panels. It consists of 160 LCD drive circuits with a display duty ratio up to 1/480: the seven HD66107Ts can drive a 640 × 480 dots LCD panel. Moreover, the LCD driver enables interfaces with various LCD controllers due to a built-in automatic generator of chip enable signals. Use of the HD66107T can help reduce the cost of an LCD-panel configuration, since it reduces the number of LCD drivers, compared with use of the HD61104 and HD61105.

Features

- Column and row driver
- 160 LCD drive circuits
- Multiplexing duty ratio :1/100 to 1/480
- 4-bit and 8-bit parallel data transfer
- Internal automatic chip enable signal generatator
- Internal standby mode
- Recommended LCD controller LSIs: HD63645, HD64645, and HD64646 (LCTC), HD66840 (LVIC)
- Power supply voltage
  internal logic : +5 V ± 10%
  LCD drive circuit : 14.0 to 37.0 V
- Operation frequency: 8.0 MHz (max.)
- CMOS Process
- 192-pin TAB (Tape Automated Bonding) package

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuits. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

Table 1. Pin Function

Symbol	Pin No.	Pin name	Input/output
V_{CC}	167	V_{CC}	
GND	161, 186, 187	Ground	
V_{LCD}	166, 192	V_{LCD}	
V1L, R	191, 165	V1L, R	
V2L, R	188, 162	V2L, R	
V3L, R	190, 164	V3L, R	
V4L, R	189, 163	V4L, R	
CL1	183	Clock 1	Input
CL2	184	Clock 2	Input
M	182	M	Input
D_0-D_7	174-181	DATA0-DATA7	Input
SHL	172	Shift left	Input
CH2	171	Channel 2	Input
BS	173	Bus Select	Input
TEST	185	TEST	Input
Y1-Y160	1-160	Y1-Y160	Output
SHL	172	Shift left	Input
$\overline{E}$	169	Enable	Input
$\overline{CAR}$	168	Carry	Onput
CH1	170	Channel 1	Input

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}: V_1 to V_4 supply power for driving an LCD (figure 1).

Control Signal

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_7: D_0-D_7 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver ($CH1 = V_{CC}$).
The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: outputs the enable signal when the LSI is used as a column driver ($CH1 = V_{CC}$).

Table 2. Relation between Display data and LCD state

Display Data	LCD Output	LCD
1 (=high level)	V1L, R/V2L, R	On
0 (=low level)	Nonselected level	Off

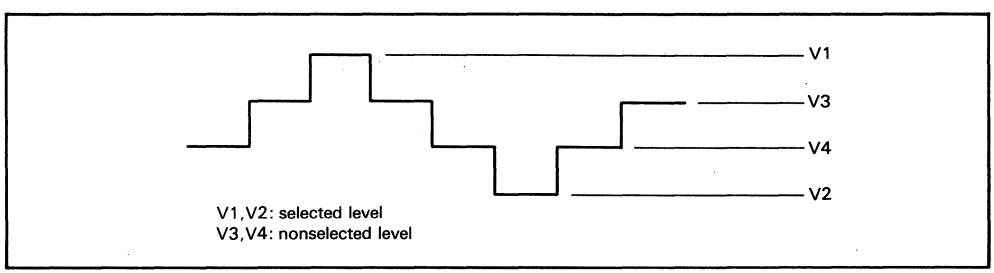


Figure 1. Power Supply for Driving an LCD

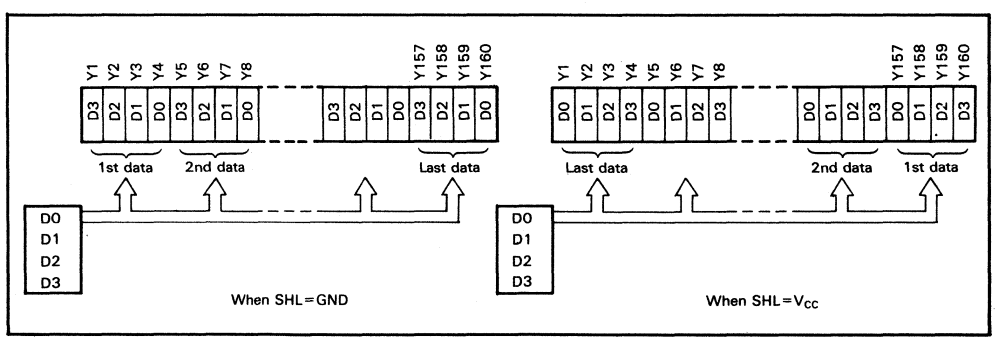


Figure 2. Relation between SHL and Data Output

$\overline{CAR}$ outputs acan data when the LSI is used as a row driver (CH1=GND). When HD66107Ts. are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip devices are columns when CH1=V_{CC}, and commons when CH1=GND.

CH2: CH2 selects the number of output data bits.

BS: BS selects the number of input data bits. When BS=V_{CC}, the chip latches 8-bits data. When BS=GND, the chip latches 4-bits data via D_0 to D_3. Fix D_4 through D_7 to GND.

TEST: Used for testing; fixed to GND, Other wise.

LCD drive interface

Y1-Y160: Each Y outputs one of the four voltage levels-V1, V2, V3, V4-according to the combination of M and display data (figure 3).

Table 3. Relation between SHL and Scan Direction of Selected Line (When LSI is Used as Common Driver)

SHL	Shift Direction of Shift Register					Scan Direction of Selected Line				
V_{CC}	E→	1→	2→	3→	4--------→160	Y1→	Y2→	Y3→	Y4--------→Y160	
GND	E→	160→	79→	78→	77--------→1	Y160→	Y79→	Y77→	Y76--------→160	

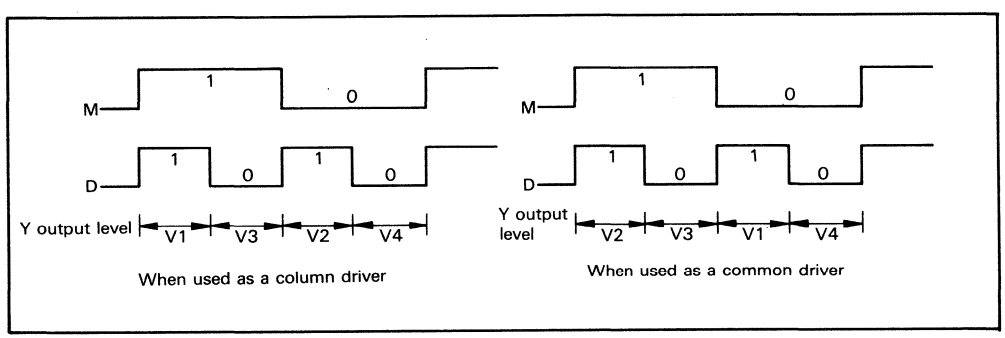
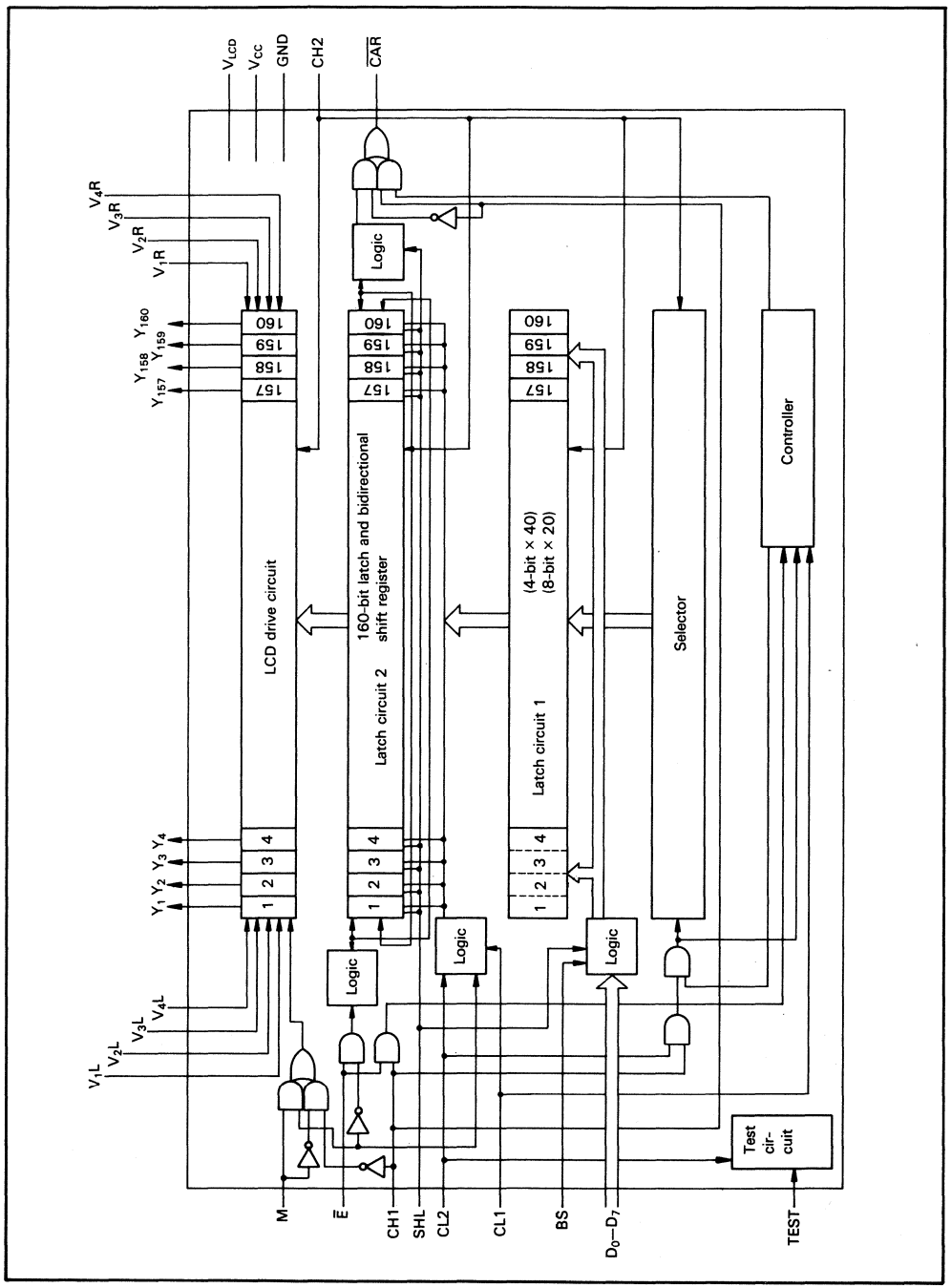


Figure 3. Selection of LCD Driver Output Level

Block Diagram



Function

LCD drive circuits

The LCD drive circuits generate four levels of voltages-V_1, V_2, V_3, and V_4-for driving an LCD. They select and transfer one of the four levels to the output circuit according to the combination of M and the data in the latch circuit 2.

Latch circuit 2

This circuit is used as a 160-bit latch circuit during column driving. Latch circuit 2 latches data input from latch circuit 1 at the falling edge of CL1 and outputs latched data to the drive circuits.

In the case of row driving latch circuit 2 is used as a 160-bit bidirectional shift register. Data input from $\overline{E}$ is shifted at the falling edge of CL2. When SHL=V_{CC}, data is shifted in input order from bit 1 to bit 160 of the shift register. When SHL=GND, data is shifted from bit 160 to bit 1 of the reister. Moreover, this latch circuit can be used as an 80-bit shift register. In this case, Y41 through Y120 are enabled, while the other bits remain unchanged.

Latch circuit 1

This circuit consists of twenty 8-bit parallel data latch circuits. It latches data D_0 through D_7 at the falling edge of CL2 during column driving. The selector signals specify which 8-bit circuit latches data. Moreover, this circuit can be used as forty 4-bit parallel data latch circuits by switching BS, in which case the circuit latches data D_0 through D_3. Moreover, this latch circuit can be used as an 80-bit shift register. In this case Y41 through Y120 are enabled, while the other bits remain unchanged.

Selector

The selector consists of a 6-bit up and down counter and a decoder. During column driving it generates a latch signal for latch circuit 1, incrementing the counter at the falling edge of CL2.

Controller

This controller is enabled during column driving. It provides a power-down function which detects completion of data latch and stops LSI operations.
Moreover, the controller automatically generates a chip enable signal ($\overline{CAR}$) which starts next-stage data latching.

Test circuit

This circuit divides the external clock and generates test signals.

Fundamental Operations

Column driving (1)

CH2 = GND (160-bit data output mode)
BS = Vcc (8-bit data latch mode)

The HD66107T starts data latch when $\overline{E}$ is at low level. In this case 8-bit parallel data is latched at the falling edge of CL2. When 160-bit data latch is completed, the HD66107T automatically stops and enters standby mode and $\overline{CAR}$ is goes to low level. If $\overline{CAR}$ is connected with $\overline{E}$ of the next-stage LSI, this next-stage LSI is activated when $\overline{CAR}$ of the previous LSI goes low.

Data is output at the falling edge of CL1. When SHL = GND, data dl is output to pin Y1 and dl60 to Y160. On the other hand, when SHL = Vcc, data d160 is output to pin Y1 and d1 to Y160. The output level is selected from among V1- V4 according to the combination of display data and alternating signal M.

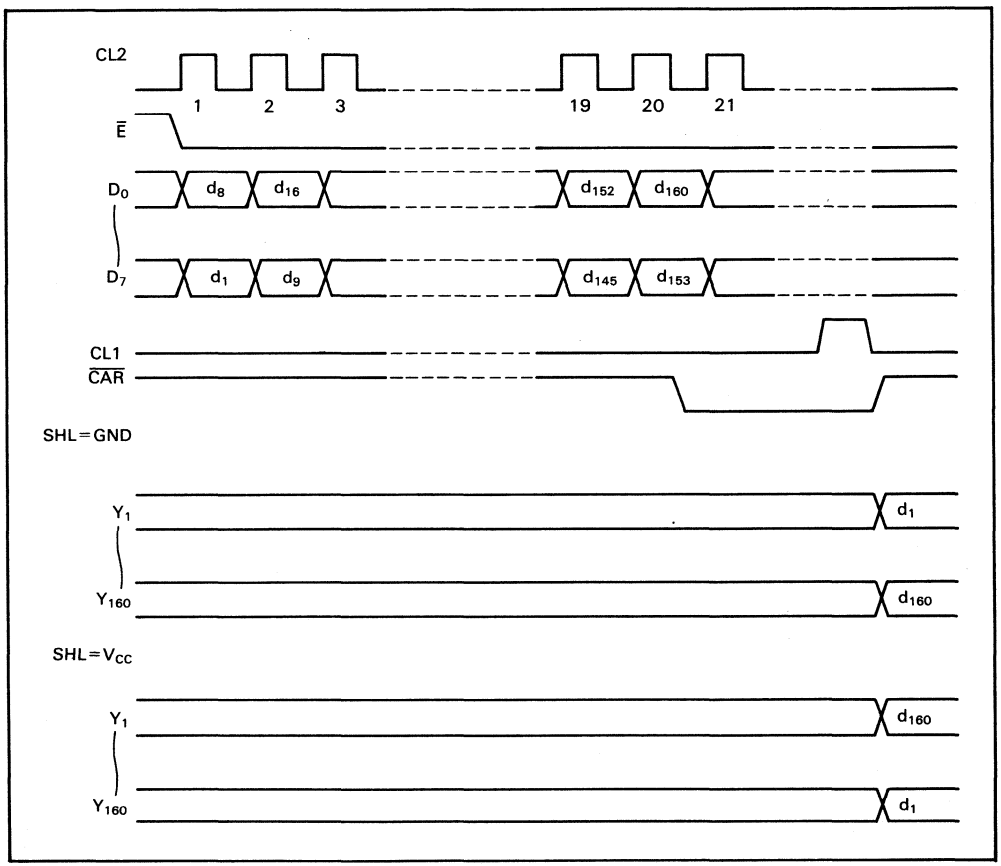


Figure 4. Column Driver Timing Chart (1)

Column driving (2)

CH2 = GND (160-bit data output mode)
BS = GND (4-bit data latch mode)

4-bit display data (D_0-D_3) is latched at the falling edge of CL2. Other operations are performed in the same way as described in "Column driving (1)".

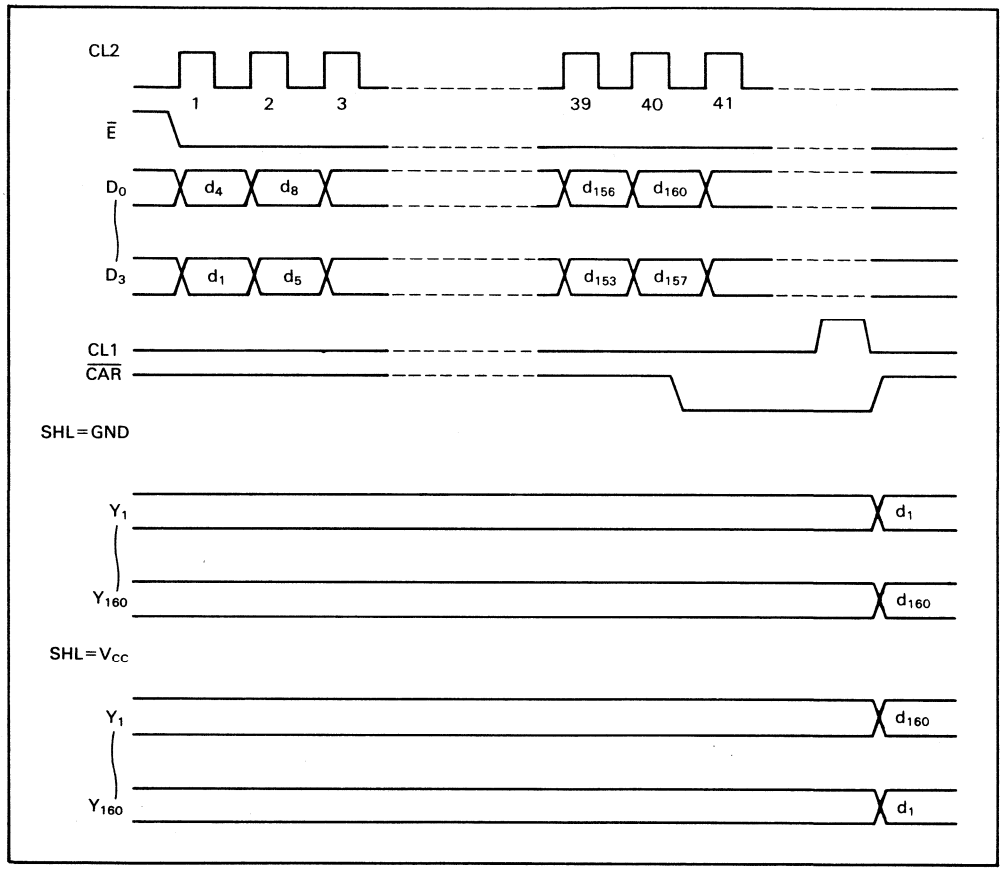


Figure 5. Column Driver Timing Chart (2)

Column driving (3)

CH2 V_{CC} (80-bit data output mode)
BS V_{CC} (8-bit data latch mode)

When CH2 is high (V_{CC}), the HD66107T can be used as an 80-bit column driver. In this case, Y41 through Y120 are enabled, the states of Y1 through Y40 and Y121 through Y160 remain unchanged.

When SHL = GND, data d1 is output to pin Y41 and d80 is output to Y120.
Conversely, when SHL = V_{CC}, data d80 is output to Y41 and d1 is output to Y120.

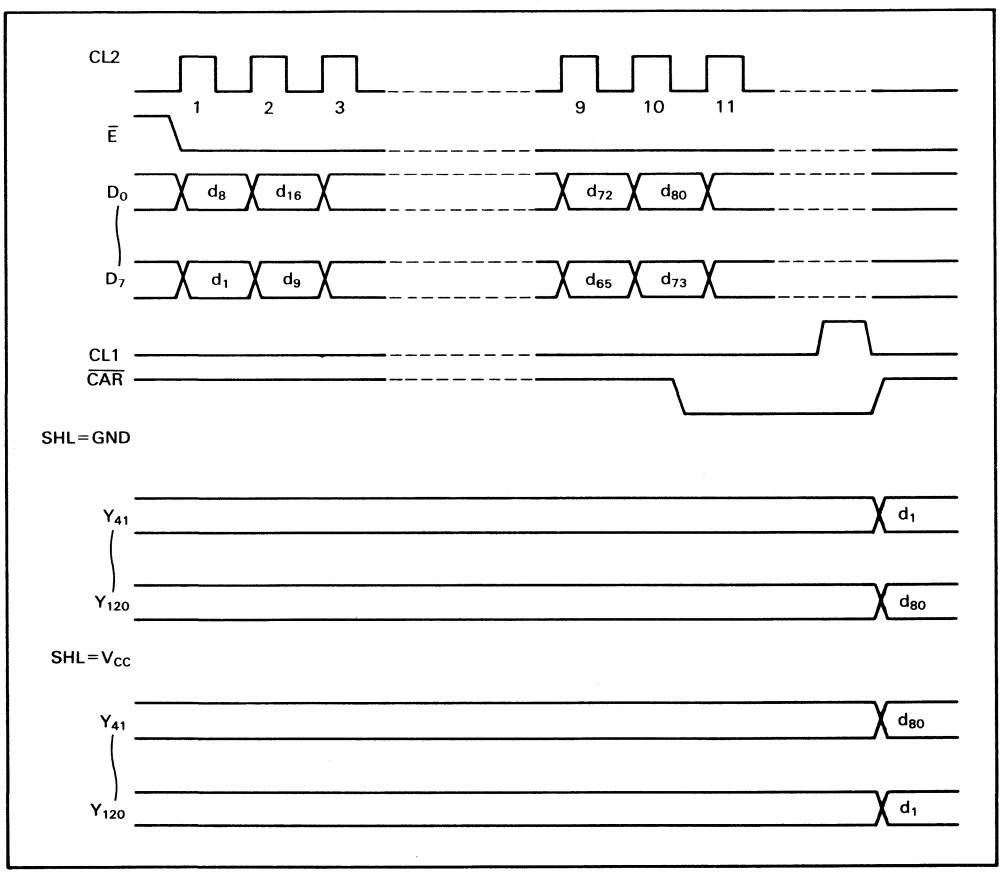


Figure 6. Column Driver Timing Chart (3)

Column driving (4)

CH2 = V_{cc} (80-bit data output mode)
BS = GND (4-bit data latch mode)

When CH2 = V_{cc} and BS = GND, 4-bit parallel data is latched, while 80-bit data is output. The output of latched data is performed in described at "Column driving (3)".

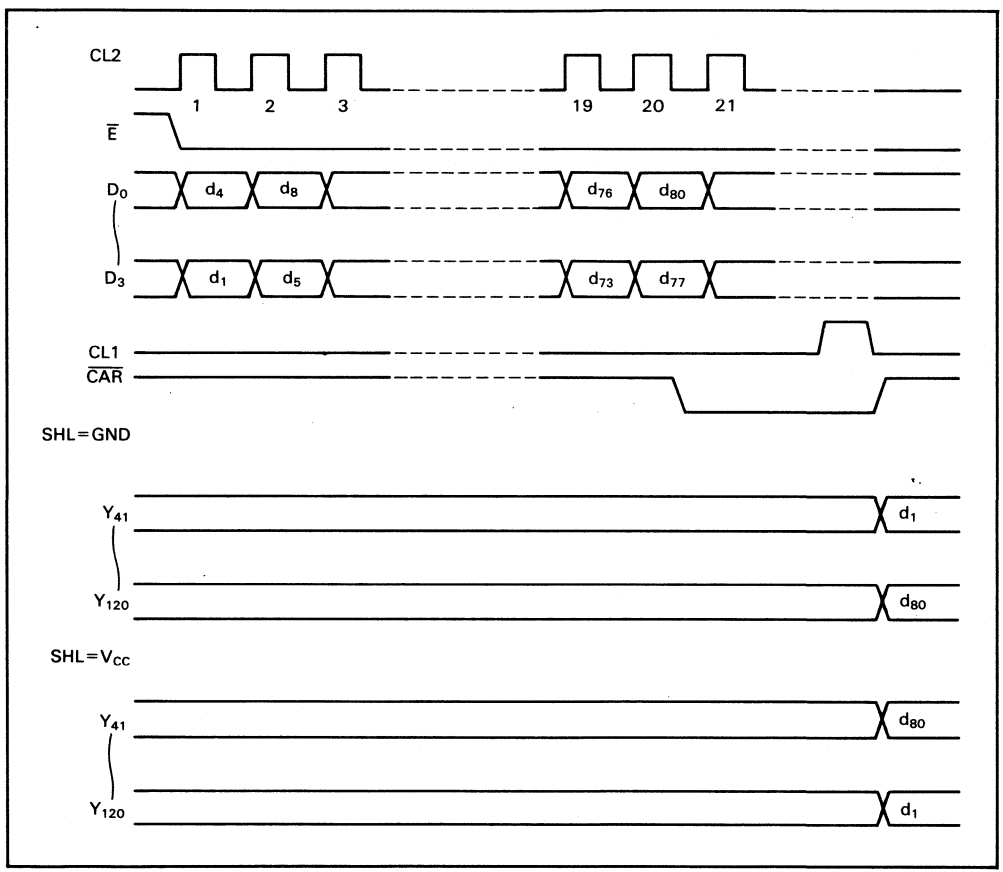


Figure 7. Column Driver Timing Chart (4)

Common driving (1)

CH2 = GND (160-bit data output mode)

The HD66107T shifts line scan data input through $\overline{E}$ at the falling edge of CL2.

When SHL=V_{cc}, 160-bit data is shifted from Y1 to Y160, whereas when SHL=GND, data is shifted from Y160 to Y1. In both cases the HD66107T outputs the data delayed for 160 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next IC driver.

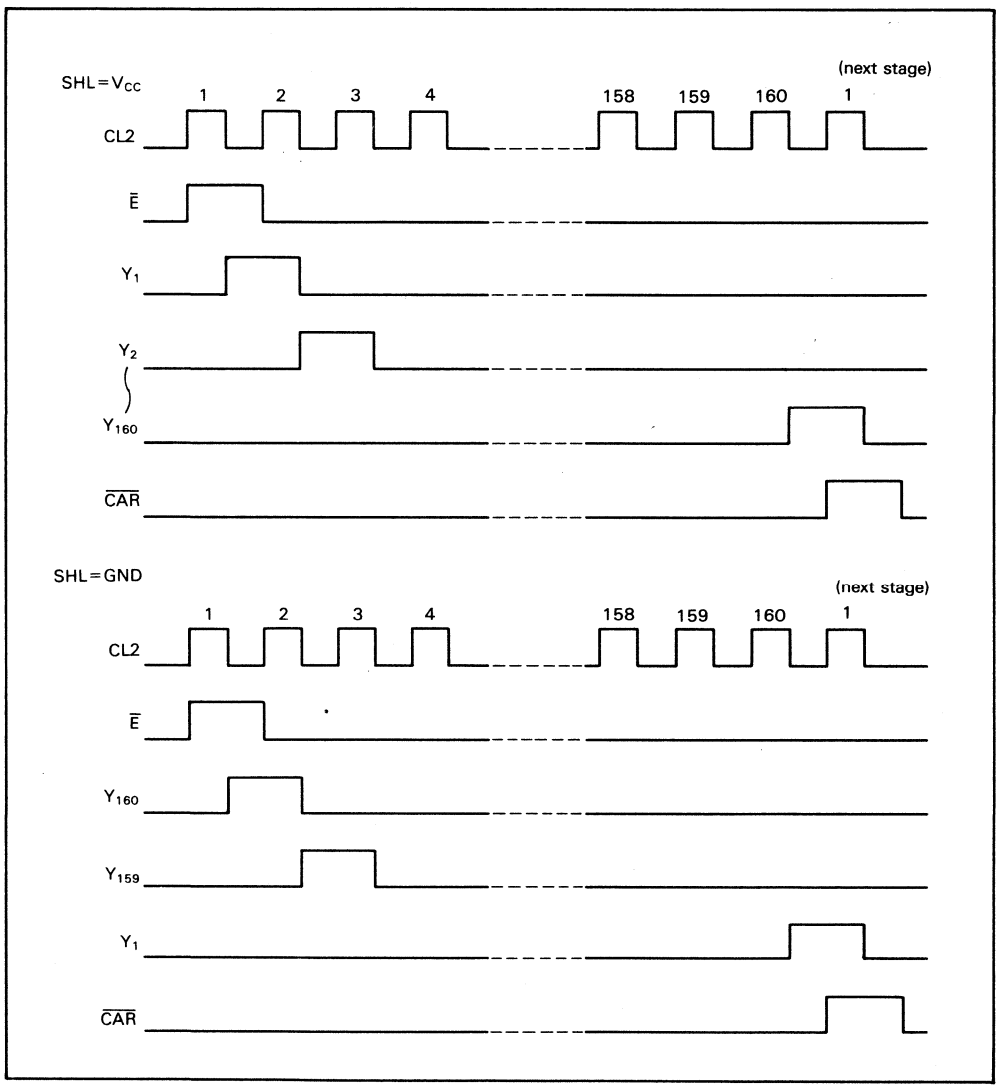


Figure 8. Common Driver Timing Chart (1)

Common driving (2)

CH2 = V_{CC} (80-bit data output mode)

When CH2 is high, the HD66107T can be used as an 80-bit row driver. In this case, Y41 to Y120 are enabled, while the other bits remain unchanged.

Line scan data input through $\overline{E}$ is shifted at the falling edge of CL2. When SHL=Vcc, data is shifted from Y41 to Y120. Conversely, when SHL=GND, data is shifted from Y120 to Y41. In both cases the HD66107T outputs the data delayed for 80 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next LSI.

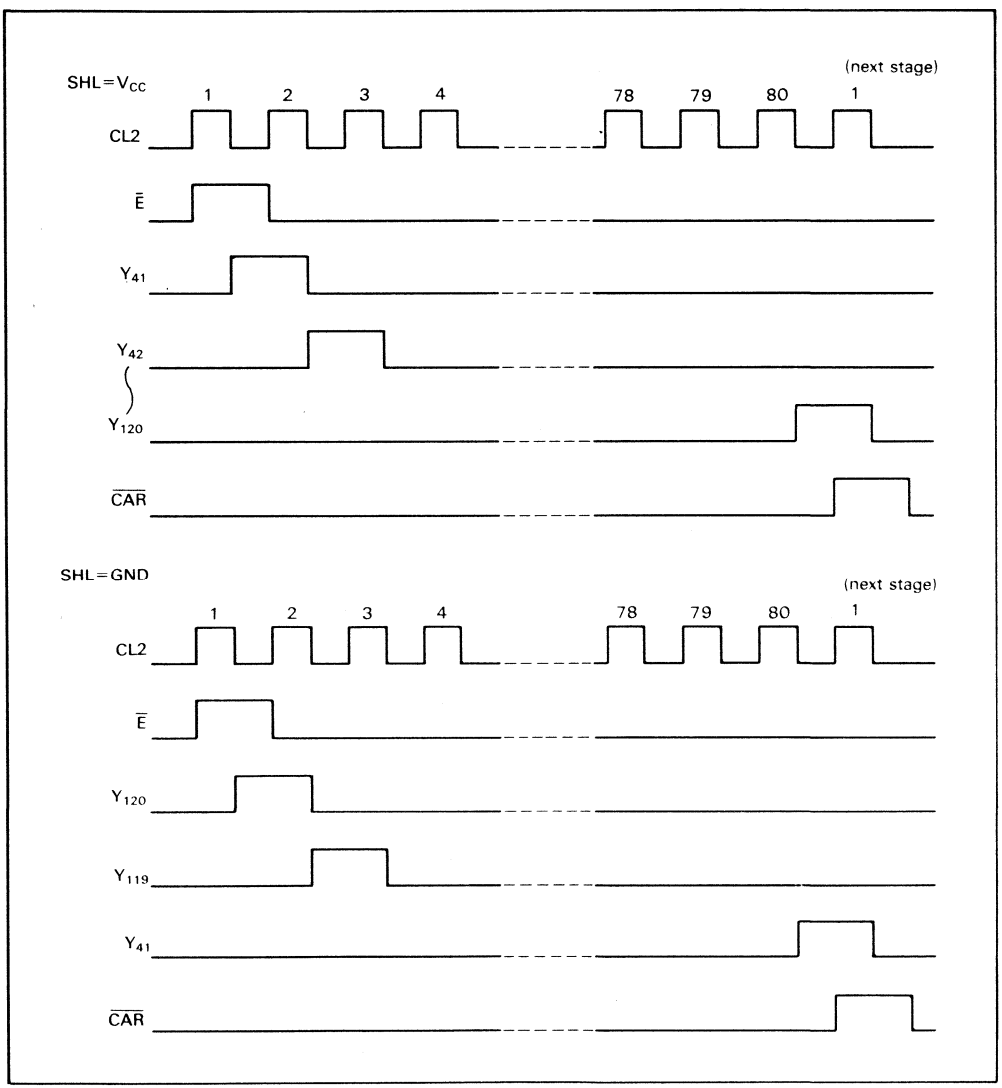


Figure 9. Common Driver Timing Chart (2)

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LDC}, and V_2 and V_4 should be near GND (figure 10). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 11).

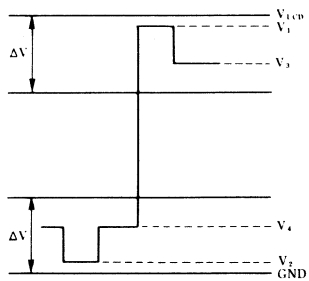


Figure 10. Driver's Output Waveform and Each Level of Voltage

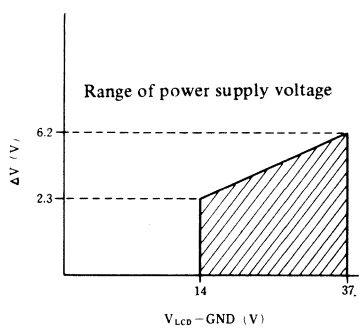
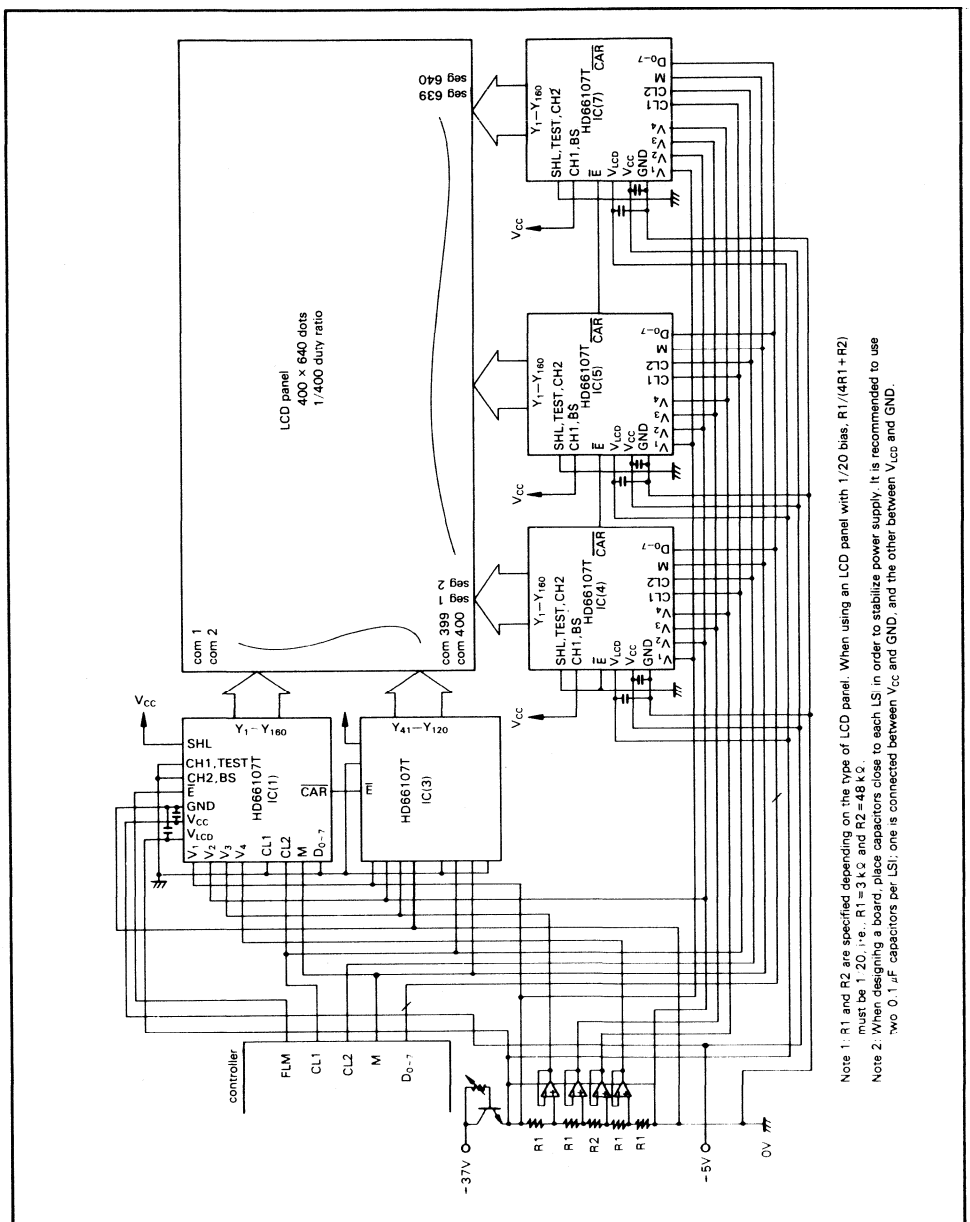


Figure 11. Power Supply Voltage V_{LCD}-GND and ΔV

Application

The following example shows a system configuration for driving a 640×400-dot LCD panel using the HD66107T.



Note 1: R1 and R2 are specified depending on the type of LCD panel. When using an LCD panel with 1/20 bias, R1/(4R1+R2) must be 1/20, i.e., R1=3 kΩ and R2=48 kΩ.

Note 2: When designing a board, place capacitors close to each LSI in order to stabilize power supply. It is recommended to use two 0.1 μF capacitors per LSI; one is connected between V_{CC} and GND, and the other between V_{LCD} and GND.

Figure 12. Application Example

Example of Waveform

In column driving

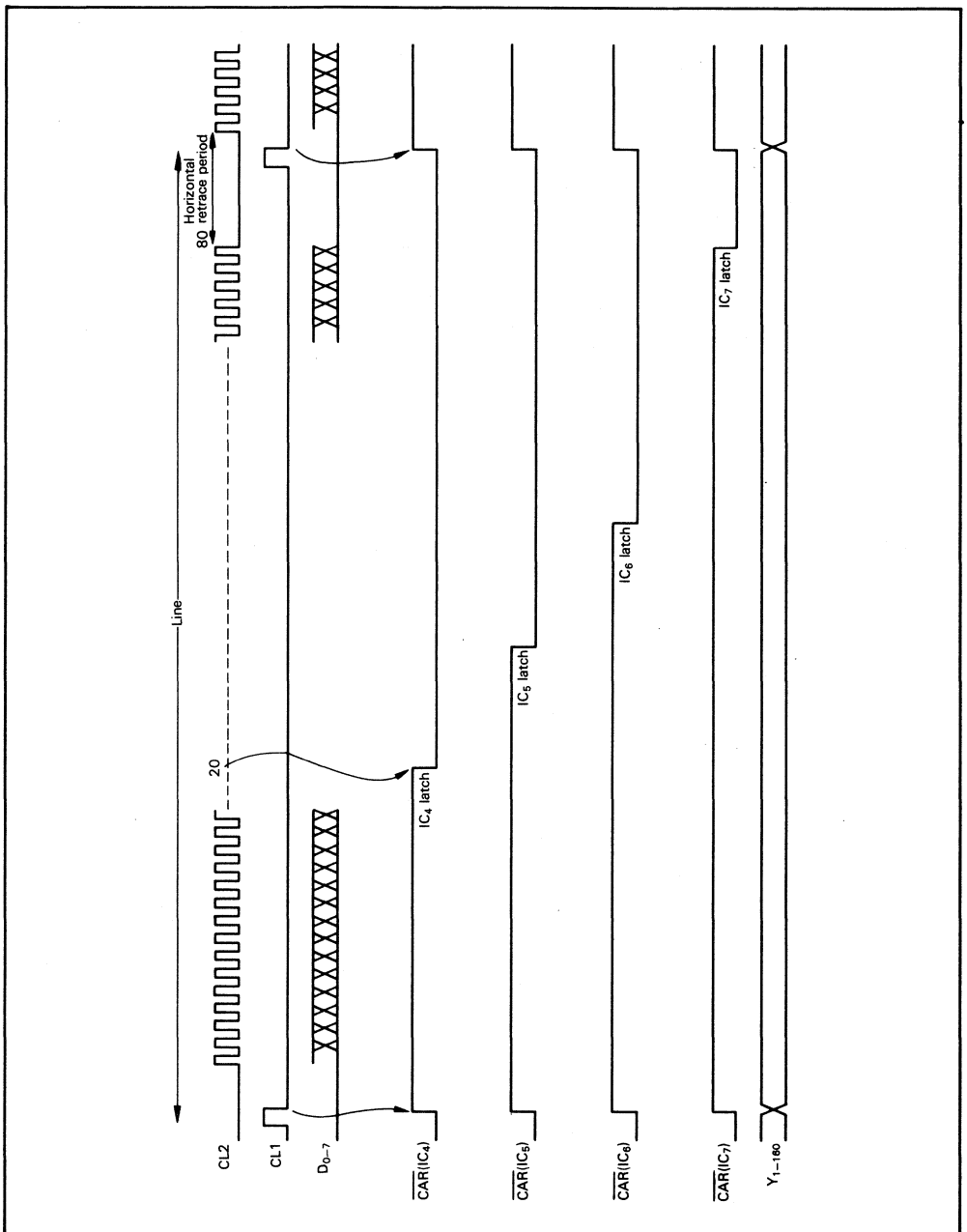


Figure 13. Column Driver Timing Chart (1)

In common driving

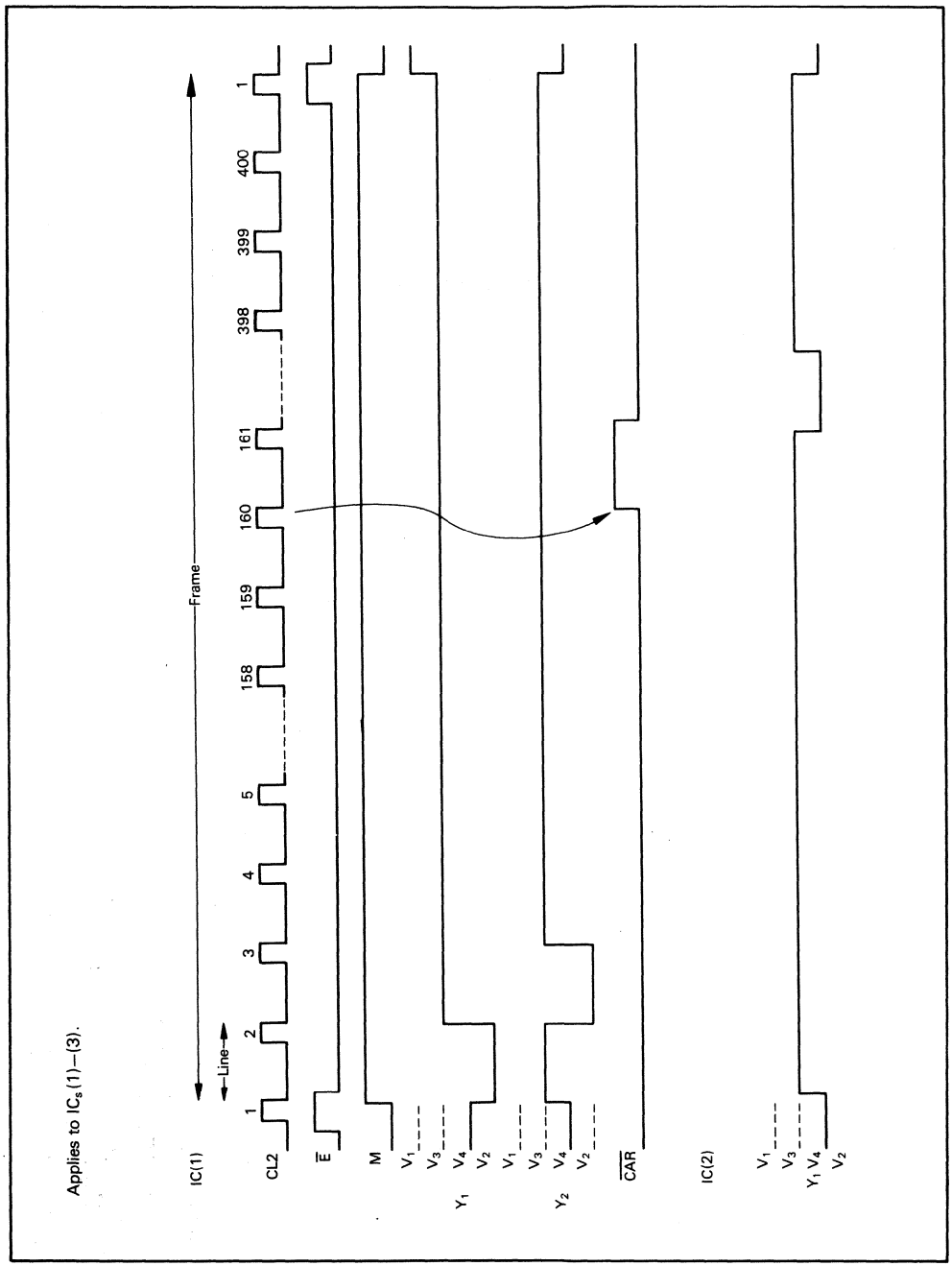


Figure 14. Common Driver Timing Chart

Absolute Maximum Rating

Item		Symbol	Rating	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	−0.3 − +7.0	V	1
	LCD drive circuit	V_{LCD}	−0.5 − +38	V	1
Input voltage (1)		V_{T1}	$-0.3-V_{CC}+0.3$	V	1, 2
Input voltage (2)		V_{T2}	$-0.3-V_{LCD}+0.3$	V	1, 3
Operation temperature		T_{opr}	−20 − +75	°C	
Storage temperature		T_{stg}	−55 − +125	°C	

Note 1. Reference point is GND (= 0V.)
2. Applies to input pins for logic circuit.
3. Applies to input pins for LCD drive circuits.
4. If the LSI is used beyond absolute maximum ratings, it may be permanently damaged. It should always be used within the above electrical characteristics to prevent malfunction or degradation of the LSI's reliability.

Electrical Characteristics

DC Characteristics (V_{CC}=5V±10%, V_{LCD}=14 to 37V, Ta=−20 to 75°C)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	CL1, CL2, M SHL, BS, CH2,	0.8×V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	TEST, D_0-D_7, E, CH1	0	0.2×V_{CC}	V		
Output high voltage	V_{OH}	CAR	V_{CC}−0.4	−	V	I_{OH}=−0.4mA	
Output low voltage	V_{OL}		−	0.4	V	I_{OL}=0.4mA	
Vi−Yj ON resistance	R_{ON}	Y1−Y160, V1−V4	−	3.0	kΩ	I_{ON}=150μA	
Input leak current (1)	I_{IL1}	CL1, CL2, M SHL, BS, CH2, TEST, D_0−D_7, E, CH1	−5.0	5.0	μA	V_{IN}=V_{CC}−GND	
Input leak current (2)	I_{IL2}	V1−V4	−100	100	μA	V_{IN}=V_{LCD}−GND	
Power dissipation (1)	I_{CC1}		−	5.0	mA	f_{CL2}=8MHz	1
Power dissipation (2)	I_{LCD1}		−	2.0	mA	f_{CL1}=28kHz	2
Power dissipation (3)	I_{ST}		−	0.5	mA	In standy mode: f_{CL2}=8MHz, f_{CL1}=28kHz	1 2
Power dissipation (4)	I_{CC2}		−	1.0	mA	f_{fcL1}=28kHz	1
Power dissipation (5)	I_{LCD2}		−	0.5	mA	fm=35Hz	3

Note 1. Input and output current is excluded. when an input is at the intermediate level is CMOS, the excessive current flows from the power supply though the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed to V_{CC} and GND respectively.
2. Applies to column driving.
3. Applies to row driving.

AC Characteristics (Vcc=5V±10%, V_{LCD}=14 to 37V, Ta=−20 to 75°C)

In column driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock cycle time	t_{cyc}	CL2	125	–	ns	
Clock high-level width	t_{CWH}	CL2	30	–	ns	
Clock low-level width	t_{CWL}	CL2	30	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	ns	
Clock rising/falling time	tct	CL1, CL2	–	30	ns	
Data setup time	t_{DSU}	D_0-D_7	30	–	ns	
Data hold time	t_{DH}	D_0-D_7	30	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	25	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	70	ns	1
M phase difference	t_{CM}	M, CL1	–	300	ns	

Note 1. Specified when connecting the load circuit shown to the right.

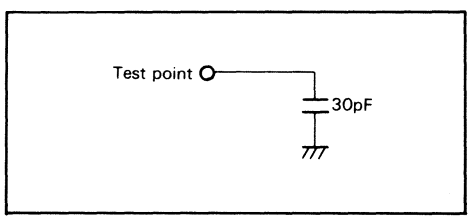


Figure 15. Test Circuit

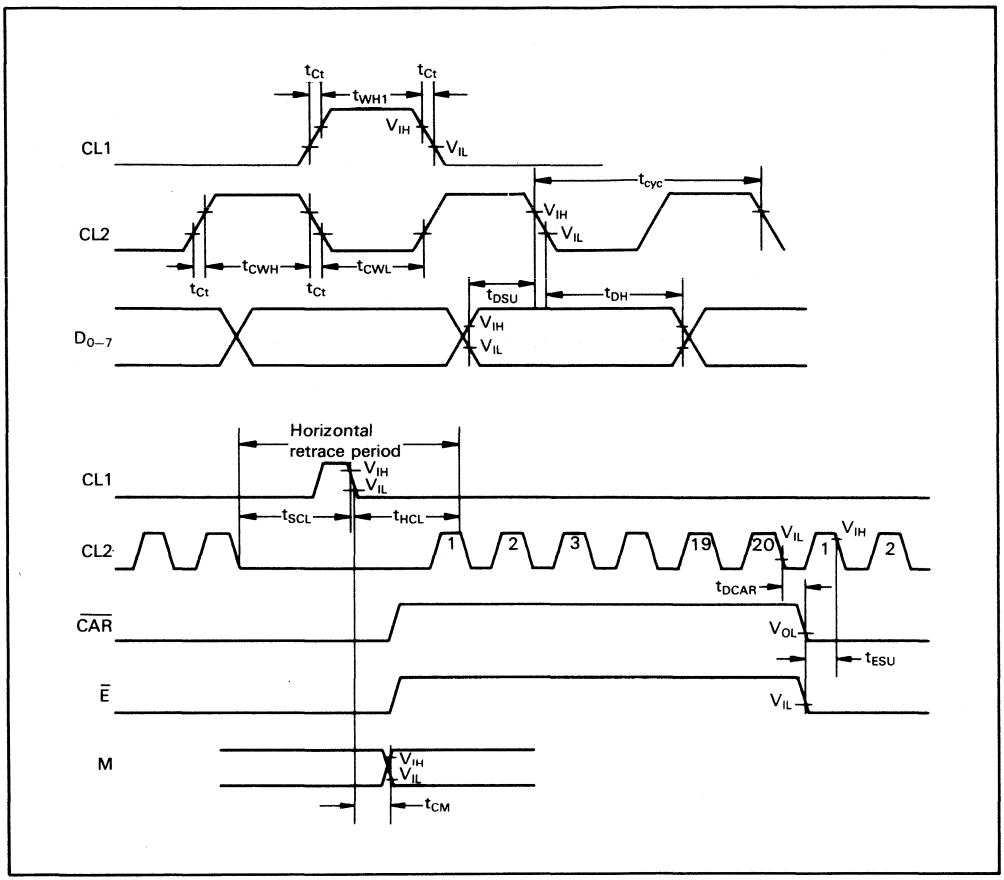


Figure 16. Controller Interface of column Driver

In common driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock low-level width	t_{WL1}	CL2	5	–	μs	
Clock high-level width	t_{WH1}	CL2	60	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	3	μs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	ns	1
Clock rising/falling time	t_{Ct}	CL2	–	30	ns	

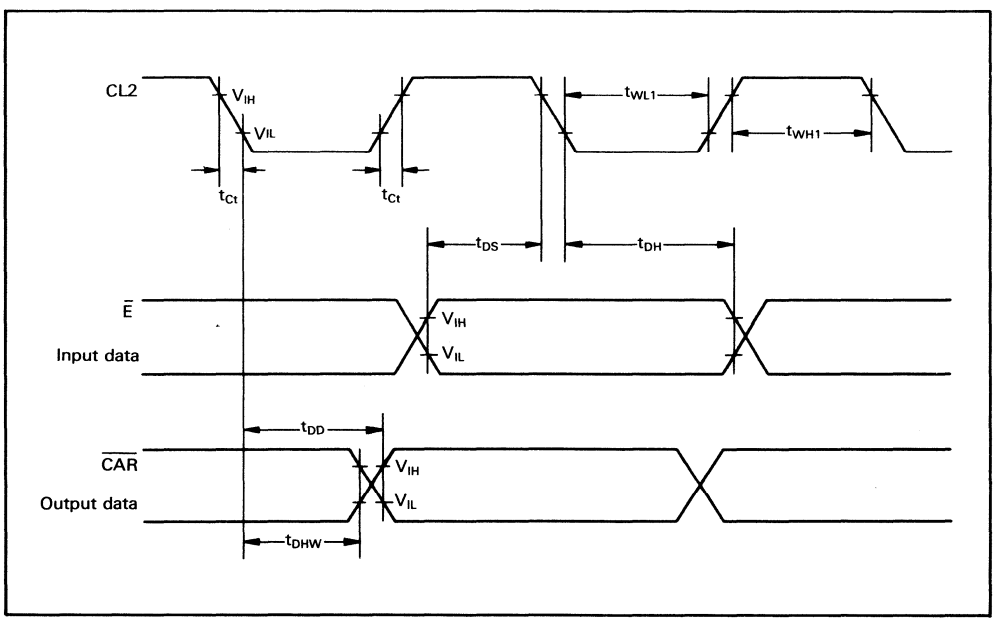
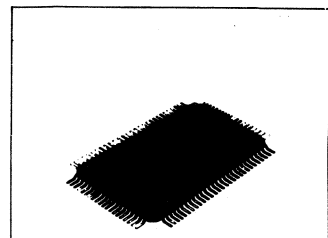


Figure 17. Controller Interface of common Driver

HD61105,HD61105A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

The HD61105, HD61105A is a common signal driver for dot matrix liquid crystal graphic display systems. It provides 80 driver output lines and the impedance is low enough to drive a large screen.

As the HD61105, HD61105A is produced in a CMOS process, it fits for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption.

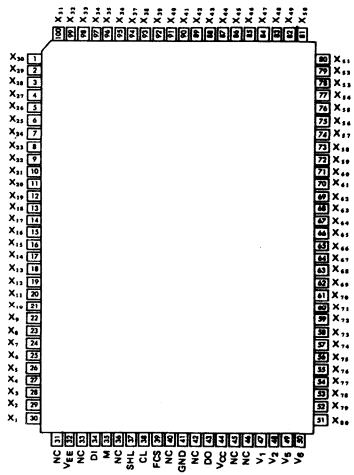


FP-100

FEATURES

- Dot matrix liquid crystal graphic display common driver with low impedance.
- Internal liquid crystal display driver circuit - 80 circuits
- Display duty ratio factor 1/64 ∿ 1/200
- Internal 80-bit shift register
- Power supply for logic circuit 5 ± 10%
- Power supply for LCD drive circuits;
  10 to 26V (HD61105)
  10 to 28V (HD61105A)
- CMOS process
- 100-pin plastic QFP (FP-100)

PIN ARRANGEMENT

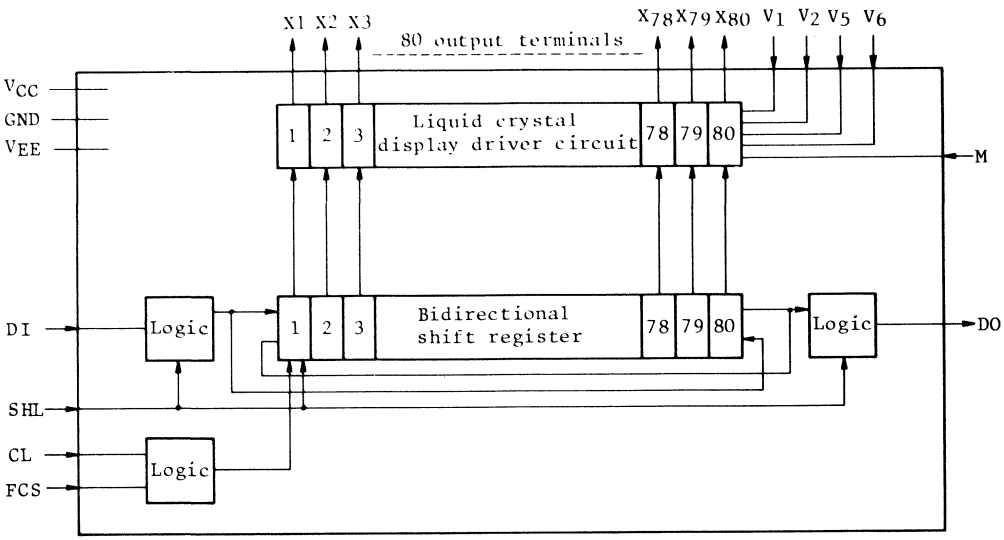


(Top View)

ORDERING INFORMATION

Type No.	LCD driving Level (V)	Package
HD61105	10 to 26	100 pin plastic QFP (FP-100)
HD61105A	10 to 28	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2) HD61105	V_{EE}	V_{CC} - 28.0 to V_{CC} + 0.3	V	5
Supply voltage (2) HD61105A	V_{EE}	V_{CC} - 28.5 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	-0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} - 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND = 0V.

(Note 3) Applies to input terminals except V1, V2, V5 and V6.

(Note 4) Applies to V1, V2, V5 and V6.

(Note 5) $V_{CC} \geqq V1 \geqq V6 \geqq V5 \geqq V2 \geqq V_{EE}$ must be maintained.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, V_{CC} - V_{EE} = 10 to 26V (HD61105), V_{CC} - V_{EE} = 10 to 28V (HD61105A), Ta = -20 to +75°C)

Test Item	Symbol	Test Condition	Specifications			Unit	Note
			Min.	Typ.	Max.		
Input "High" voltage	V_{IH}		0.7×V_{CC}	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		GND		0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-0.4mA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V	2
Vi-Xj ON Resistance	R_{ON}	V_{CC}-V_{EE}=10V Load current ± 150μA	-	-	2.0	kΩ	5
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1.0		1.0	μA	3
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-25		25	μA	4
Clock Frequency	fCL	Transfer clock CL	-	-	100	kHz	
Dissipation Current (1)	I_{GG1}	at 1/200 duty operation	-	-	200	μA	6
Dissipation Current (2)	I_{EE}	at 1/200 duty operation	-	-	100	μA	7

(Note 1) Applies to input terminals FCS, SHL, DI, M, and CL.

(Note 2) Applies to output terminal of DO.

(Note 3) Applies to the terminals NC, and the input terminals FCS, SHL, DI, M, and CL.

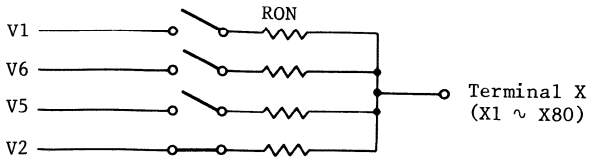
(Note 4) Applies to V1, V2, V5, and V6. No wire is to be connected to X1∿X80.

(Note 5) Resistance value between terminal X (one of X1 to X80) and terminal V (one of V1, V2, V5, and V6) when load current is applied to one of terminals X1 to X80. This value is specified under the following condition.

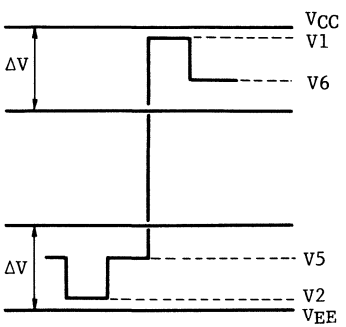
$V_{CC} - V_{EE} = 26V$

V1, V6 = $V_{CC} - 1/10\ (V_{CC} - V_{EE})$

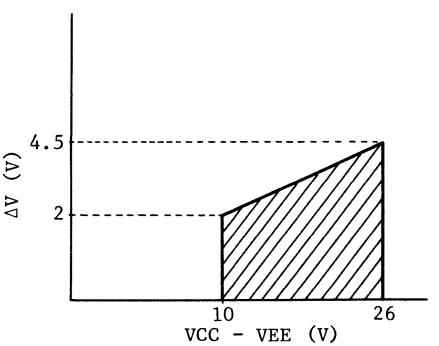
V2, V5 = $V_{EE} + 1/10\ (V_{CC} - V_{EE})$



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1, and V6, and negative voltage to V2 and V5, within the ΔV range respectively. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage V_{CC}-V_{EE} and ΔV

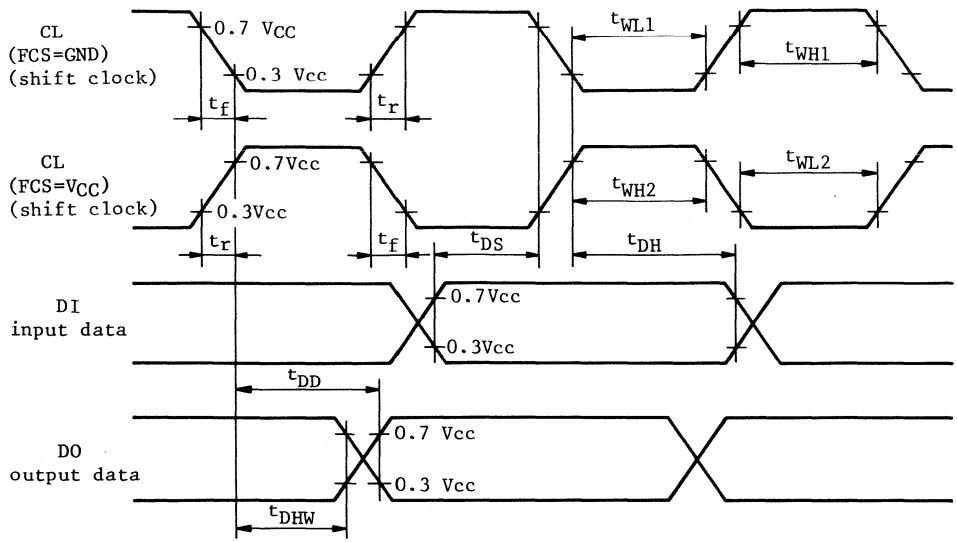
(Note 6) The currents flowing through the GND terminal. Specified when display data is transferred under following conditions.

CL frequency f_{CL} = 14 kHz (data transfer rate)
M frequency fM = 35 Hz (frame frequency / 2)
Display duty ratio 1/200
$V_{IH} = V_{CC}$, V_{IL} = GND
No load on outputs

(Note 7) The currents flowing through the V_{EE} terminal in the conditions of (Note 6). No line is to be connected to the V terminal.

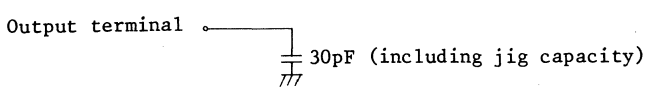
● AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, Ta = -20 to +75°C)



Item	Symbol	Min.	Typ.	Max.	Unit	Note
Clock low level width (FCS = GND)	tWL1	5.0			µs	
Clock high level width (FCS = GND)	tWH1	125			ns	
Clock low level width (FCS = Vcc)	tWL2	125			ns	
Clock high level width (FCS = Vcc)	tWH2	5.0			µs	
Data setup time	tDS	100			ns	
Data hold time	tDH	100			ns	
Output delay time	tDD			3.0	µs	1
Output hold time	tDHW	100			ns	
Clock rise time	tr			30	ns	
Clock fall time	tf			30	ns	

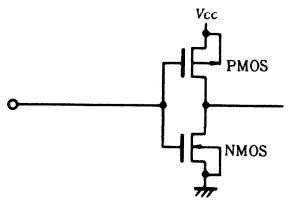
Note 1) The following load circuits are connected for specification:



TERMINAL CONFIGURATION

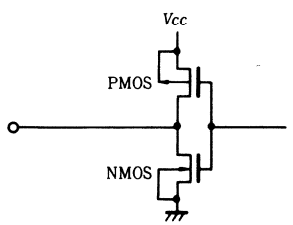
● Input Terminal

Applicable Terminals: DI, CL, SHL, FCS, M



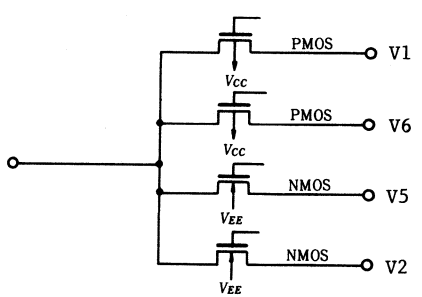
● Output Terminal

Applicable Terminal: DO

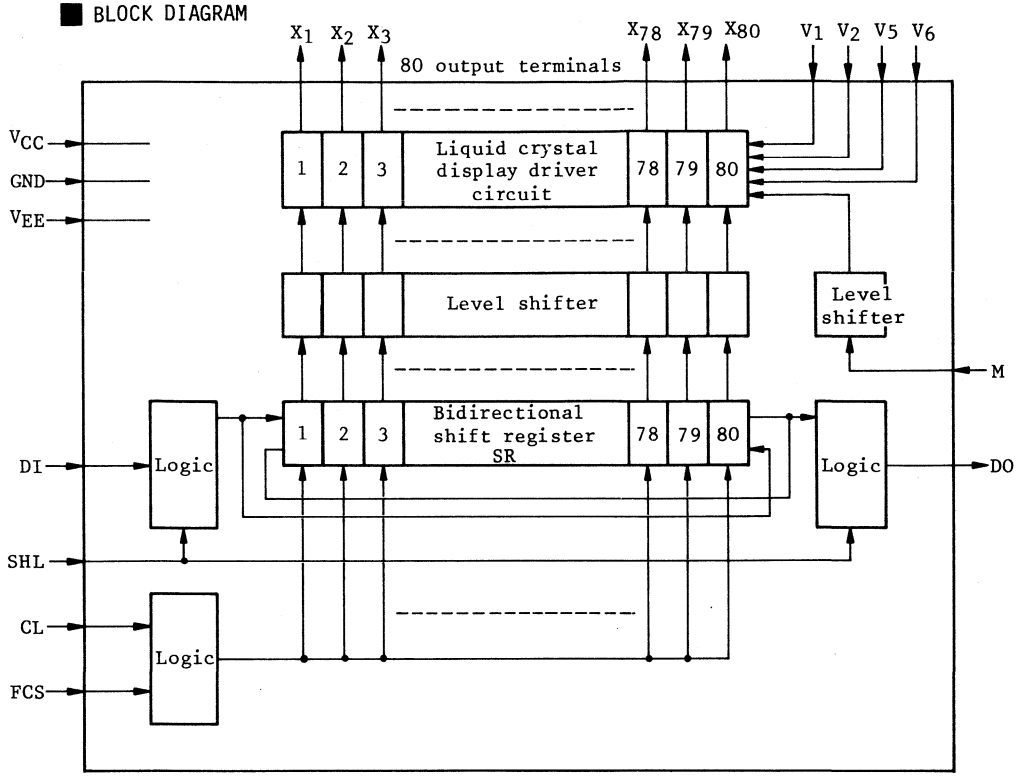


● Output Terminal

Applicable Terminals: X1 ∿ X80



BLOCK DIAGRAM



BLOCK FUNCTIONS

● Bidirectional Shift Register

This is a 80-bit bidirectional register. The data from the DI terminal is shifted by the shift clock CL. The output terminal DO outputs the last shifted data. In case of serial cascade connection, the terminal DO functions as the data input to the next LSI. The terminal SHL selects the data shift direction, and the terminal FCS selects the shift clock phase.

Truth Table

(Positive Logic)

SHL	Data Shift Direction
1	DI→SR1→SR2→SR3 ------- SR79→SR80→DO
0	DI→SR80→SR79→SR78 -------- SR2→SR1→DO

FCS	Shift Clock Phase
0	Shifted at the falling edge of CL.
1	Shifted at the rising edged of CL.

● Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Truth Table

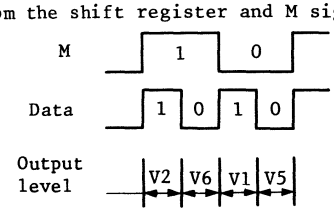
(Positive Logic)

Data from the shift register	M	Output level
0	0	V5
1	0	V1
0	1	V6
1	1	V2

● HD61105 TERMINAL FUNCTIONS

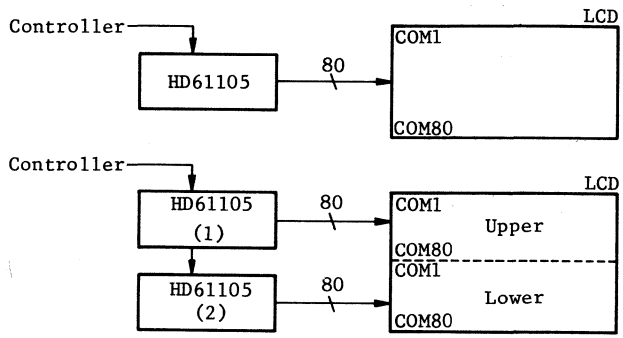
Terminal name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} - GND: Power supply for internal logic V_{CC} - V_{EE}: Power supply for LCD drive circuit
V1 V2 V5 V6	4		Liquid crystal drive level power supply	Power supply for liquid crystal drive V1, V2 --- selection level V5, V6 --- non-selection level
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC} Shift register operates at the rising edge of CL. FCS = GND Shift register operates at the fall of CL.
M	1	I	Controller	Signal to convert LCD driver signal into AC.

- to be continued

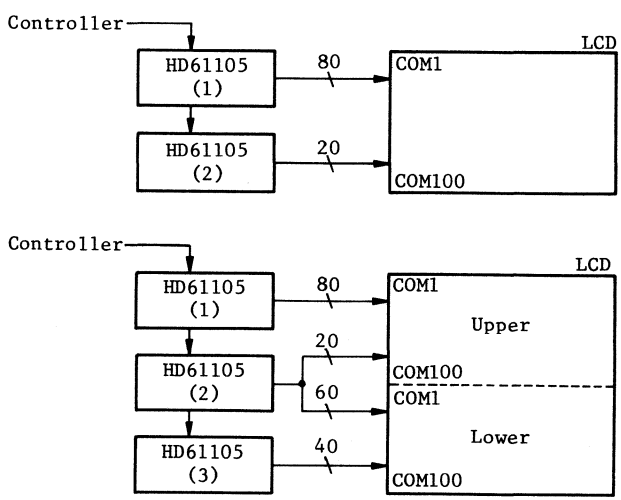
<table>
<tr><th>Terminal name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>CL</td><td>1</td><td>I</td><td>Controller</td><td>Shift clock
FCS = V_{CC} Shift register operates at the rise of CL.
FCS = GND Shift register operates at the fall of CL.</td></tr>
<tr><td>DI</td><td>1</td><td>I</td><td>Controller or the terminal DO of HD61105</td><td>Shift register data input
In case of cascade connection, the terminal DI is connected to the terminal DO of the preceding LSI.</td></tr>
<tr><td>DO</td><td>1</td><td>0</td><td>Open or the terminal DI of HD61105</td><td>Shift register data output
In case of cascade connection, the terminal DO is connected to the terminal DI of the next LSI.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table><tr><th>SHL</th><th>Shift direction</th><th>Common scanning direction</th></tr><tr><td>VCC</td><td>DI→SR1→SR2→SR80</td><td>X1→X80</td></tr><tr><td>GND</td><td>DI→SR80→SR79→SR1</td><td>X80→X1</td></tr></table></td></tr>
<tr><td>X1 ∿ X80</td><td>80</td><td>0</td><td>Liquid crystal display</td><td>Liquid crystal display driver output
Outputs one of the four liquid crystal display driver levels V1, V2, V5 and V6 with the combination of the data from the shift register and M signal.
 
Data "1" --- Selection level
"0" --- Non-selection level
When SHL is VCC, X1 corresponds to COM1 and X80 corresponds to COM80.
When SHL is GND, X80 corresponds to COM1 and X1 corresponds to COM80.</td></tr>
<tr><td>NC</td><td>7</td><td></td><td>Open</td><td>Unused.
No line is to be connected.</td></tr>
</table>

● OUTLINE OF HD61105 SYSTEM CONFIGURATION

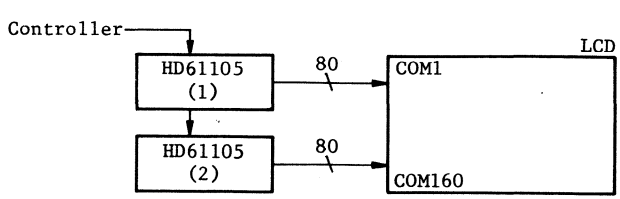
1) When display duty ratio of LCD is 1/80



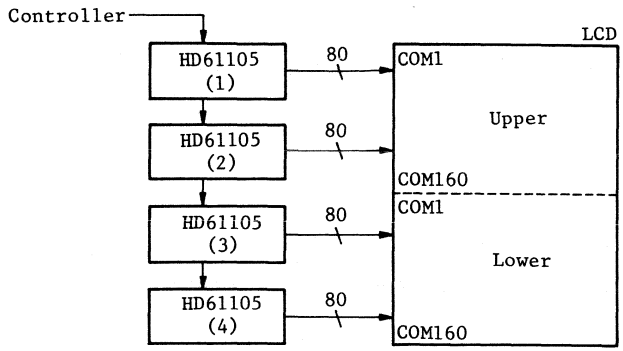
2) When display duty ratio of LCD is 1/100



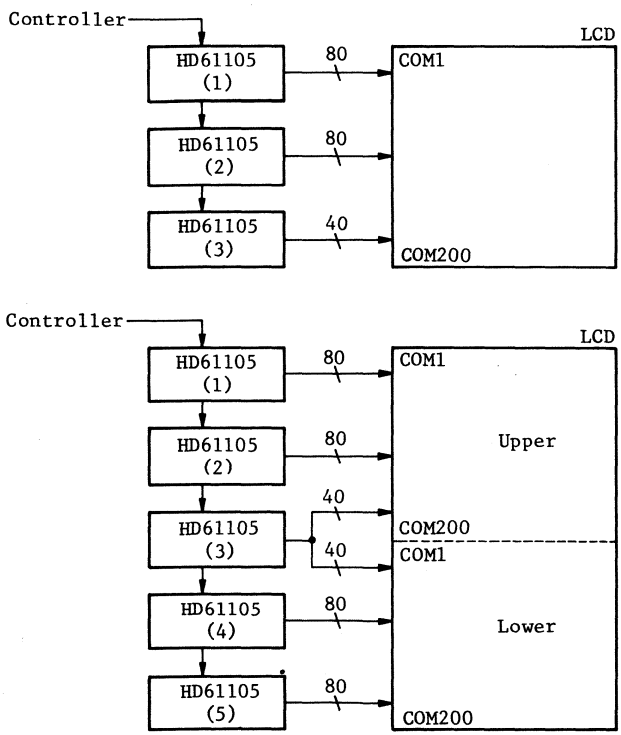
3) When display duty ratio of LCD is 1/160



4) When display duty ratio of LCD is 1/160



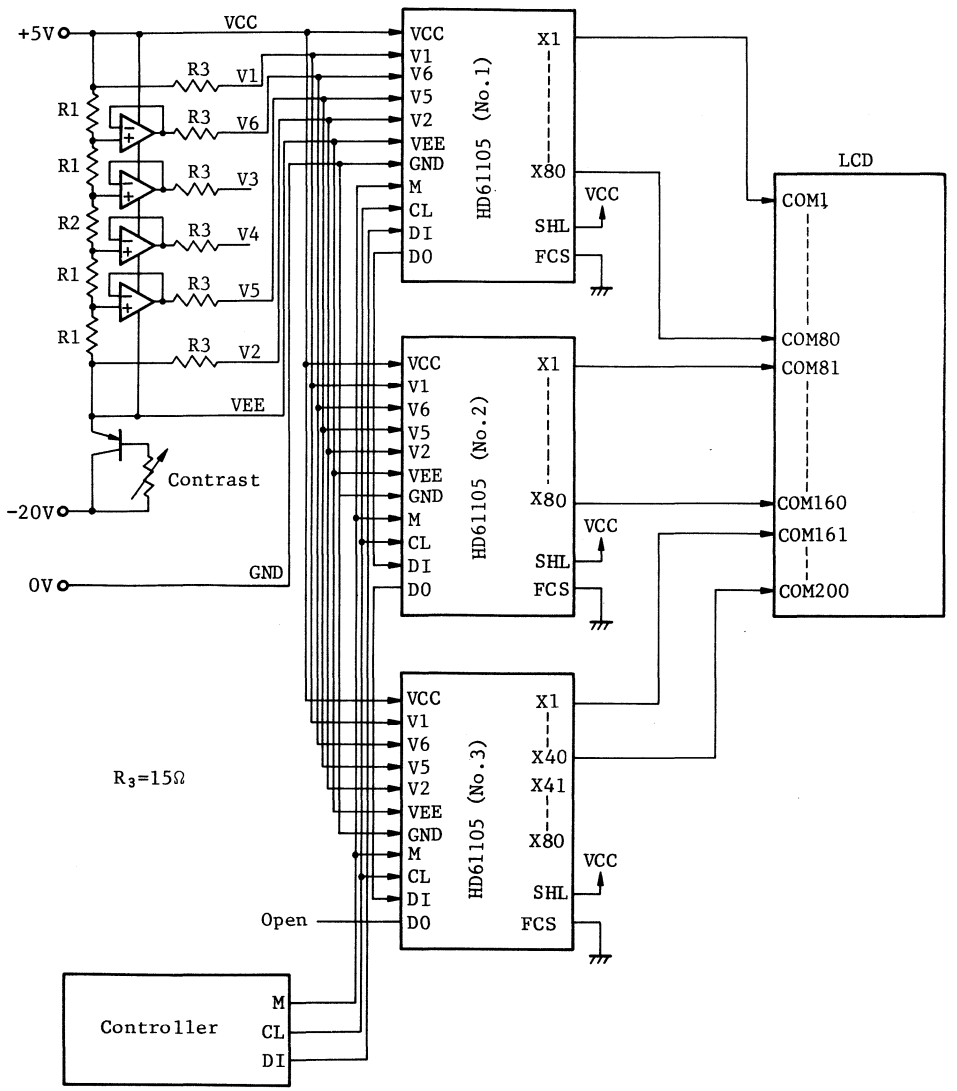
5) When display duty ratio of LCD is 1/200



● EXAMPLE OF CONNECTION

1) 1/200 duty ratio

a) Example of connection (SHL = V_{CC}, FCS = GND)



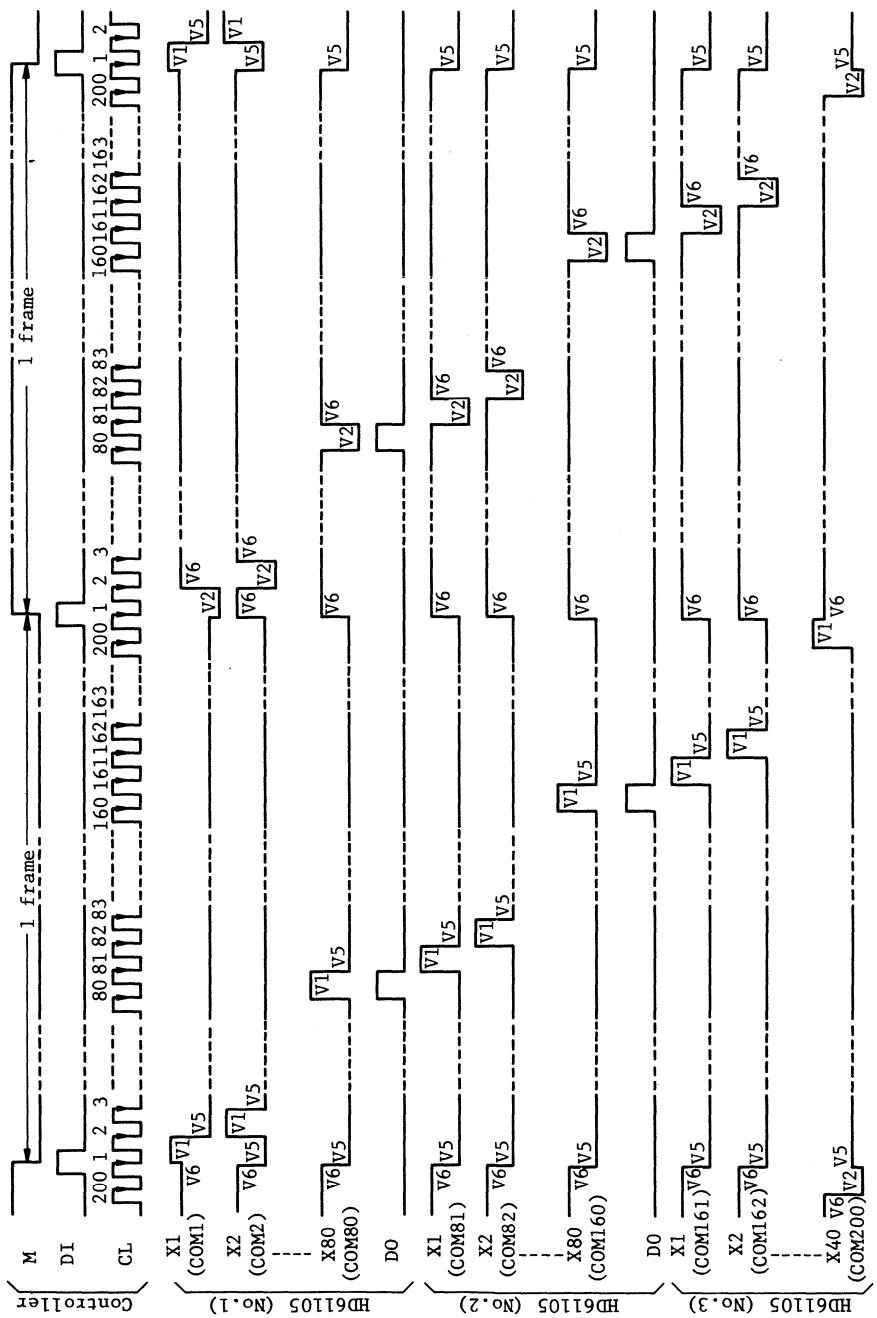
Note 1) The values of R1 and R2 vary with the LCD panel used.

When bias factor is 1/15, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{15}$$

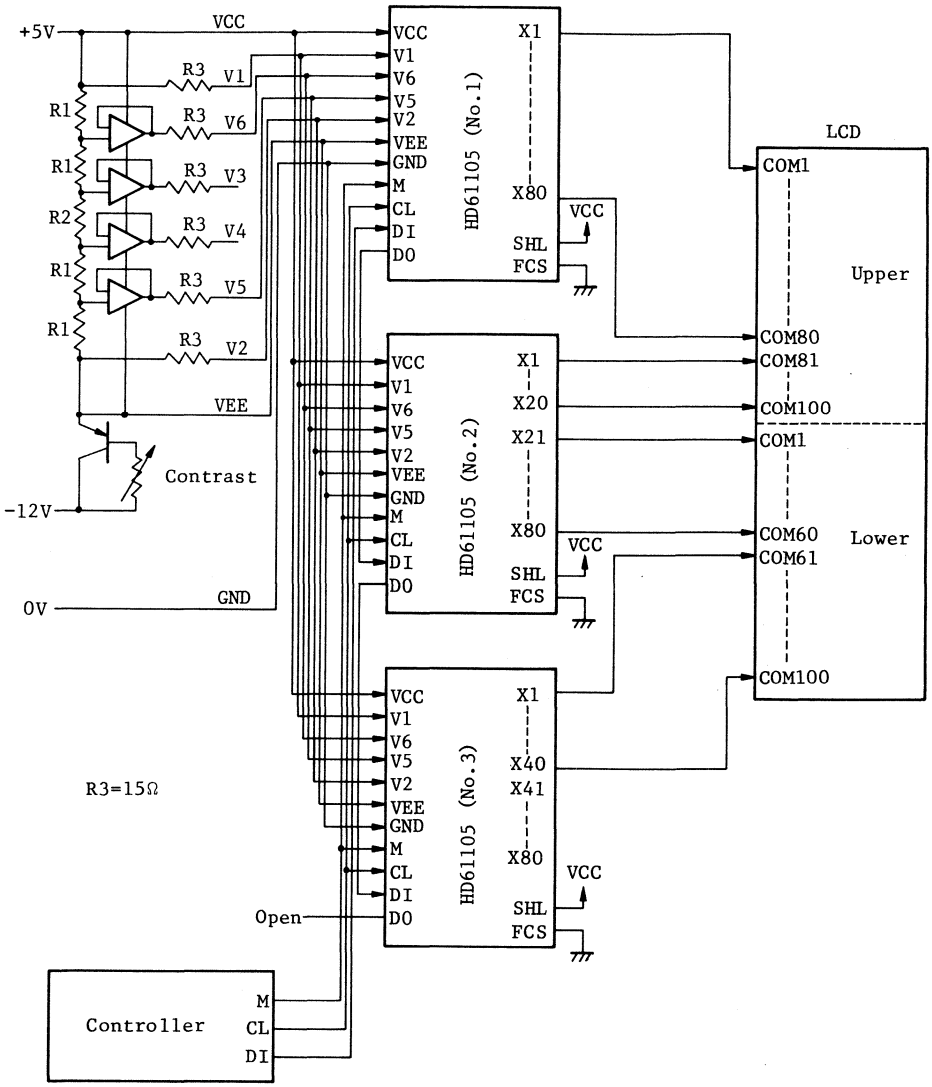
For example, R1 = 3k, R2 = 33kΩ

b) Example of Waveform



2) 1/100 duty ratio

a) Example of connection 1 (SHL = V_{CC}, FCS = GND)



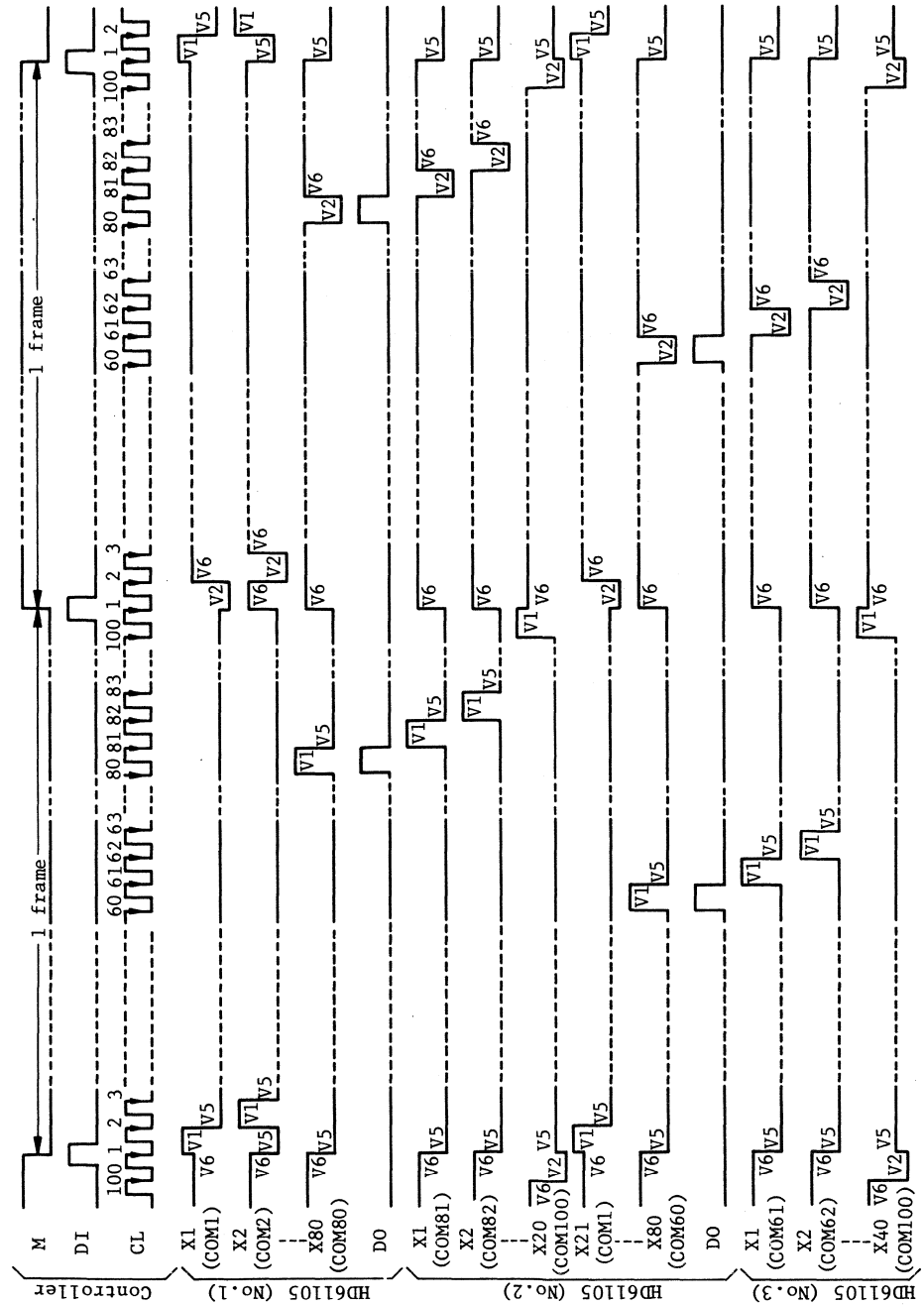
Note 1) The values of R1 and R2 vary with the LCD panel used.

When bias factor is 1/11, the values of R1 and R2 should satisfy

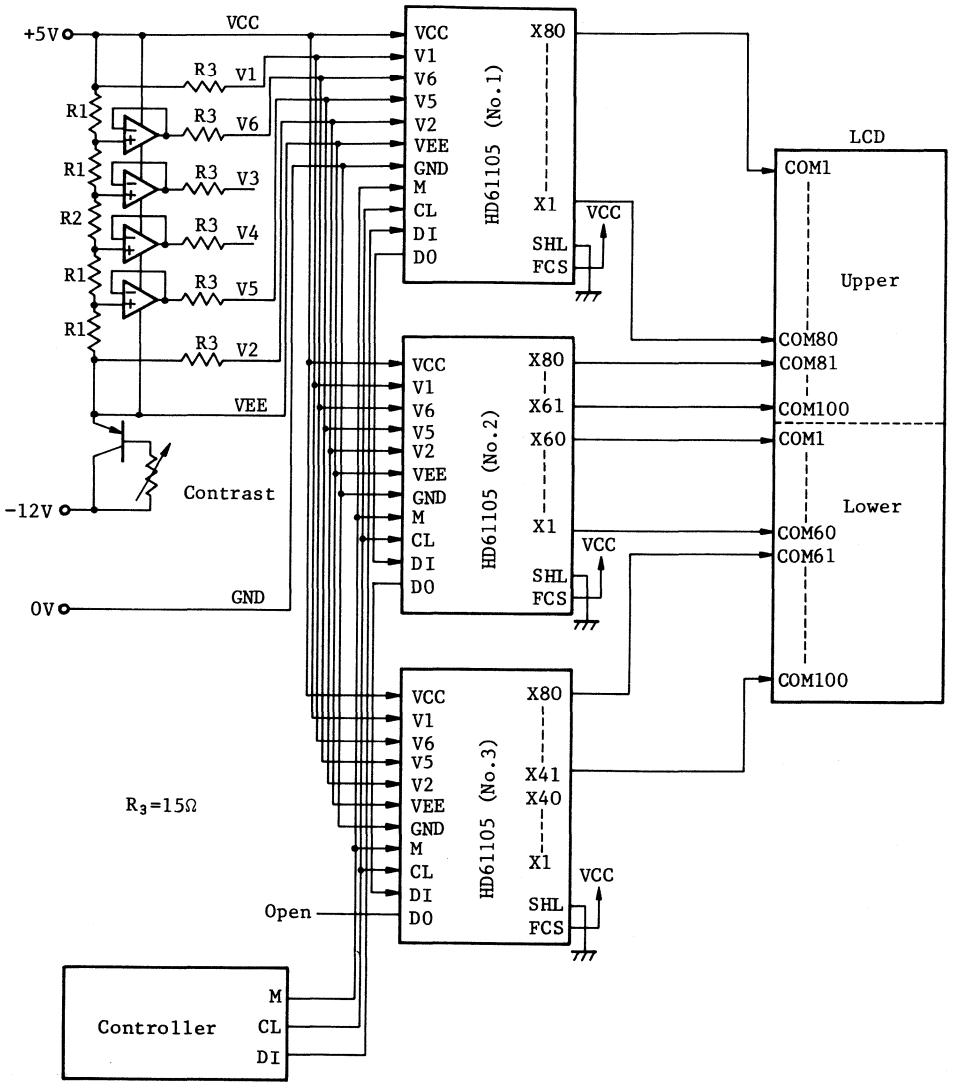
$$\frac{R1}{4R1 + R2} = \frac{1}{11}$$

For example, R1 = 3kΩ, R2 = 21kΩ

b) Example of Waveform



c) Example of connection 2 (SHL = GND, FCS = V_{CC})



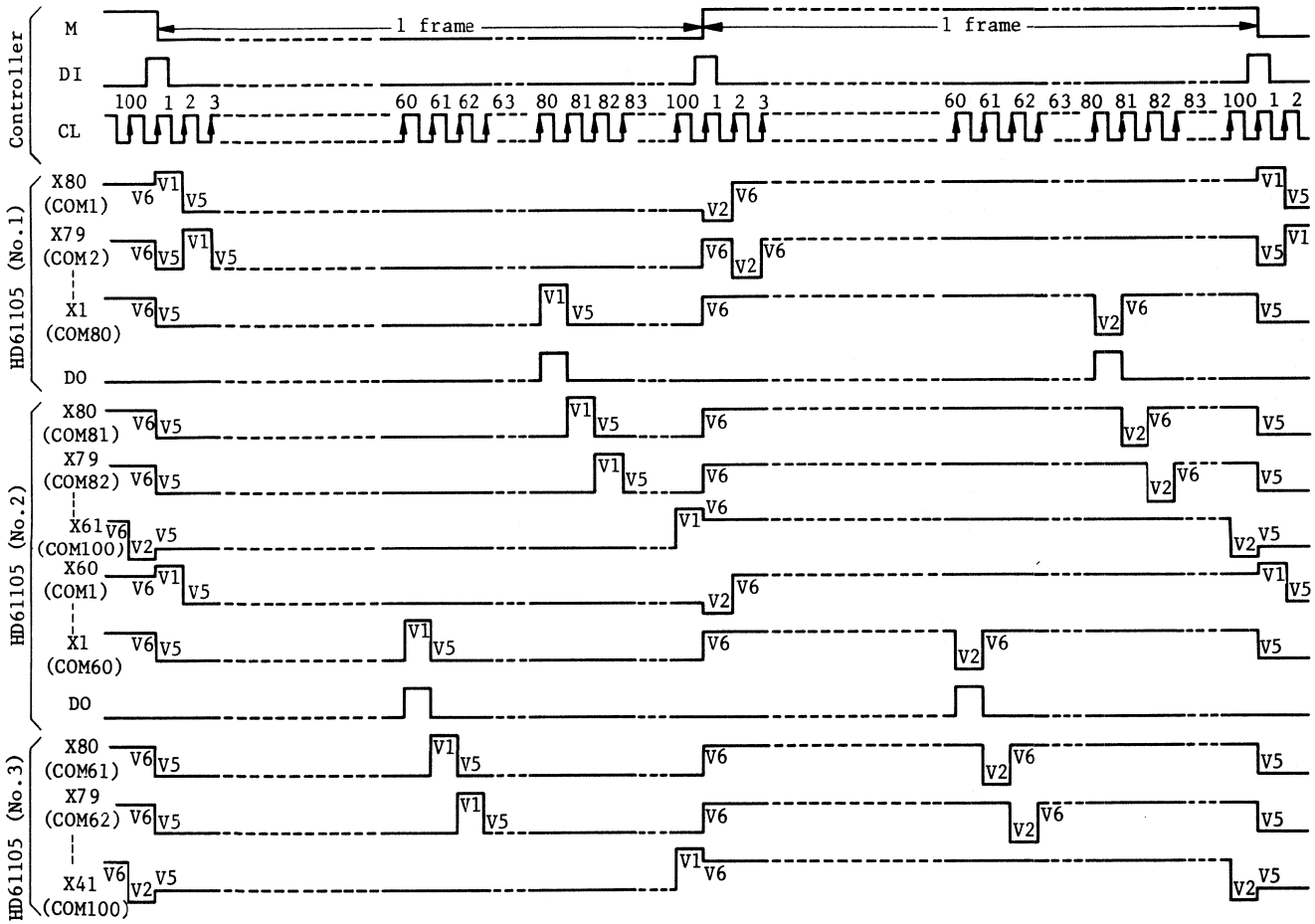
Note 1) The values of R1 and R2 vary with the LCD panel used.

When bias factor is 1/11, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{11}$$

For example, R1 = 3kΩ, R2 = 21kΩ

d) Example of Waveform



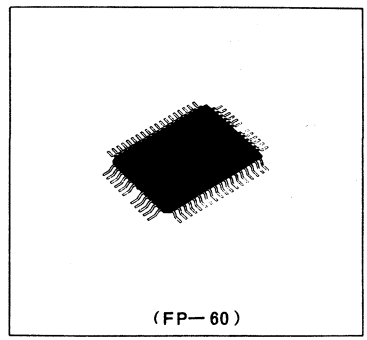
HD61830

(Dot Matrix Liquid Crystal Graphic Display Controller)

The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

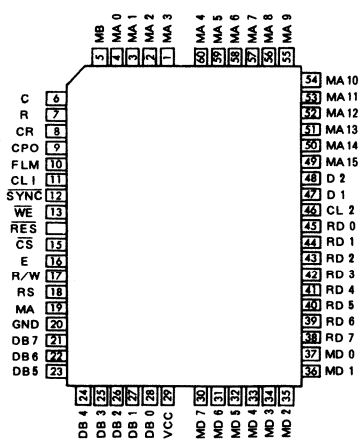
It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830 is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power dissipation.



(FP—60)

■ PIN ARRANGEMENT

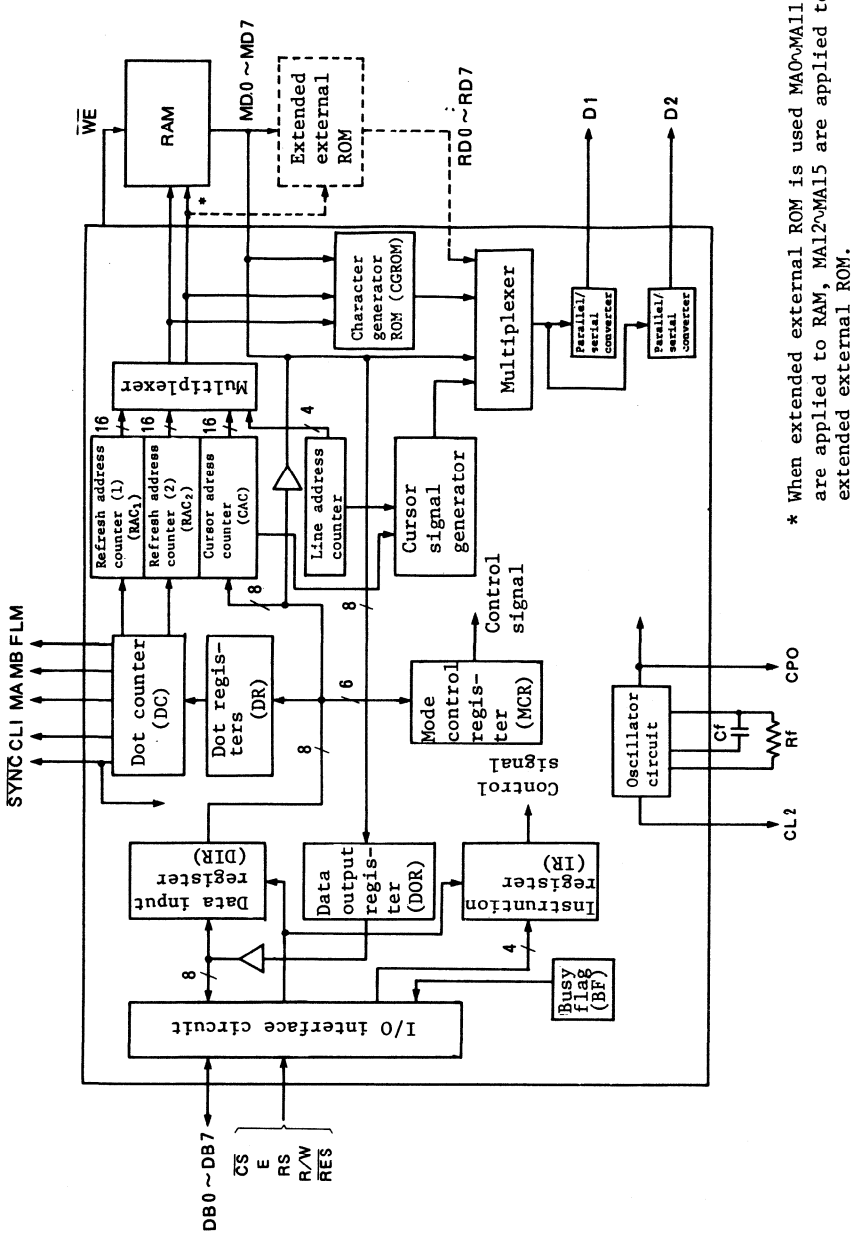


(Top View)

■ FEATURES

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  Graphic mode ..... 512K dots (2^{16} bytes)
  Character mode ..... 4096 characters (2^{12} characters)
- Internal character generator ROM ..... 7360 bits
  160 types of 5×7 dot character fonts
  32 types of 5×11 dot character fonts
  Total 192 types
  (Can be extended to 256 types (4K bytes max.) by external ROM)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  Static to 1/128 duty selectable
- Various instruction functions
  Scroll, Cursor ON/OFF/blink, Character blink, Bit manipulation
- Display method ..... Selectable A or B types
- Internal oscillator (with external resistor and capacitor)
- Low power dissipation
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package

■BLOCK DIAGRAM



* When extended external ROM is used MA0~MA11 are applied to RAM, MA12~MA15 are applied to extended external ROM.

■BLOCK FUNCTIONS

●Registers

The HD61830 has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR) and mode control register (MCR).

The IR is a 4-bit register which stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at "High" level).

The DR are registers used to store the dot informations such as character pitches and the number of vertical dots and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display ON/OFF and cursor ON/OFF/blink. The information sent from the MPU is written in it via the DIR.

● Busy Flag (BF)

With "1", the busy flag indicates the HD61830 is performing an internal operation. The next instruction cannot be accepted. As shown in Control Instruction(14),the busy flag is output on DB7 under the conditions of RS=1, R/W=1 and E=1. Make sure the busy flag is "0" before writing the next instruction.

● Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

● Refresh Address Counters (RAC1/RAC2)

The refresh address counters are counters used to control the addresses of external RAM, character generator ROM (CGROM) and extened external ROM having the two types: RAC1 and RAC2. The RAC1 is used for upper half of screen and the RAC2 for lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12∿MA15) are ignored. The 4 bits of line address counter are output instead of it and used as the address of extended ROM.

● Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 types) or 5×11 (32 types). The use of extended ROM allows 8×16 (256 types max.) to be used.

● Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by the instruction. It is used to hold an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of cursor address counter is automatically increased by 1 after the display data is read or written and after the Set/Clear Bit instruction is executed.

● Cursor Signal Generator

The cursor can be displayed by the instruction in the character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

● Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

■TERMINAL FUNCTIONS

Name	Function
DB0∿7	Data bus ... Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{CS}$	Chip select ... Selected state with $\overline{CS}$=0.
R/W	Read/Write ... R/W=1 ... MPU ← HD61830 R/W=0 ... MPU → HD61830
RS	Register select ... RS=1 ... Instruction register RS=0 ... Data register
E	Enable ... Data is written at the fall of E. Data can be read while E is 1.
CR, R, C	CR oscillator
$\overline{RES}$	Reset ... Reset=0 results in display OFF, slave mode and Hp=6.
MA0∿15	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 ("0": Character 1st line, "F": Character 16th line).
MD0∿7	Display data bus ... Three-state I/O common terminal.
RD0∿7	ROM data input ... Dot data from external character generator is input.
$\overline{WE}$	Write enable ... Write signal for external RAM.
CL2	Display data shift clock for LCD drivers.
CL1	Display data latch signal for LCD drivers.
FLM	Frame signal for display synchronization.
MA	Signal for converting liquid crystal driving signal into AC, A type
MB	Signal for converting liquid crystal driving signal into AC, B type
D1, D2	Display data serial output D1 ... For upper half of screen D2 ... For lower half of screen
CPO	Clock signal for HD61830 in slave mode.
$\overline{SYNC}$	Synchronous signal for parallel operation. Three-state I/O common terminal (with pull-up MOS). Master ... Synchronous signal is output. Slave ... Synchronous signal is input.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	1, 2
Terminal voltage	V_T	-0.3 ∿ V_{CC}+0.3	V	1, 2
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: All voltage is referred to GND=0V.

Note 2: If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI's within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

■ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±5%, GND=0V, Ta=-20∿+75°C)

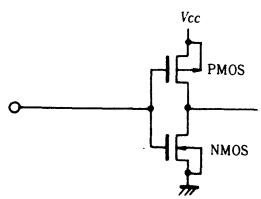
Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "High" voltage (TTL)	V_{IH}		2.2	-	V_{CC}	V	1
Input "Low" voltage (TTL)	V_{IL}		0	-	0.8	V	2
Input "High" voltage	V_{IHR}		3.0	-	V_{CC}	V	3
Input "High" voltage (CMOS)	V_{IHC}		0.7V_{CC}	-	V_{CC}	V	4
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3V_{CC}	V	4
Output "High" voltage (TTL)	V_{OH}	$-I_{OH}$=0.6mA	2.4	-	V_{CC}	V	5
Output "Low" voltage (TTL)	V_{OL}	I_{OL}=1.6mA	0	-	0.4	V	5
Output "High" voltage(CMOS)	V_{OHC}	$-I_{OH}$=0.6mA	V_{CC}-0.4	-	V_{CC}	V	6
Output "Low" voltage (CMOS)	V_{OLC}	I_{OL}=0.6mA	0	-	0.4	V	6
Input leakage current	I_{IN}	V_{IN}=0∿V_{CC}	-5	-	5	µA	7
Three-state leakage current	I_{TSL}	V_{OUT}=0∿V_{CC}	-10	-	10	µA	8
Power dissipation (1)	P_{w1}	CR oscillation fosc=500kHz	-	10	15	mW	9
Power dissipation (2)	P_{w2}	External clock fcp=1MHz	-	20	30	mW	9
Internal clock operation							
Clock oscillation frequency	f_{osc}	Cf=15pF±5% Rf=39kΩ±2%	400	500	600	kHz	10

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
External clock operation							
External clock operating frequency	f_{cp}		100	500	1100	kHz	11
External clock duty	Duty		47.5	50	52.5	%	11
External clock rise time	t_{rcp}		-	-	0.05	µs	11
External clock fall time	t_{fcp}		-	-	0.05	µs	11
Pull-up current	I_{PL}	V_{IN}=GND	2	10	20	µA	12

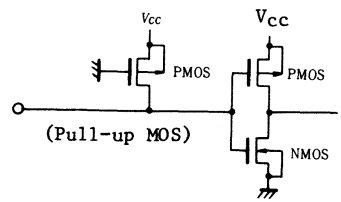
Note: The I/O terminals are of the following configuration:

● Shape of Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (Without pull-up MOS)

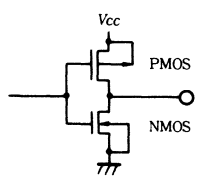


Applicable terminal: RD0∿RD7 (With pull-up MOS)



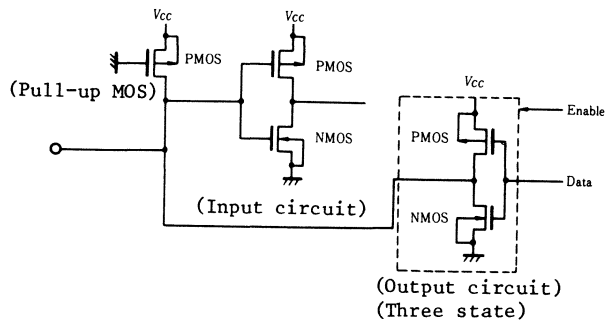
● Shape of Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, CP0, D1, D2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA0∿MA15



● Shape of I/O Common Terminal

Applicable terminal: DB0∿DB7, $\overline{SYNC}$, MD0∿MD7



Note 1: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR and $\overline{RES}$.

Note 2: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.

Note 3: Applied to terminal $\overline{RES}$.

Note 4: Applied to terminals $\overline{SYNC}$ and CR.

Note 5: Applied to terminals DB0∿DB7, $\overline{WE}$, MA0∿MA15,and MD0∿MD7.

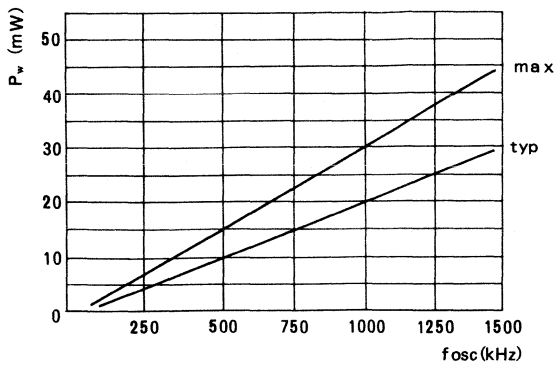
Note 6: Applied to terminals $\overline{SYNC}$, CP0, FLM, CL1, CL2, D1, D2, MA and MB.

Note 7: Applied to input terminals.

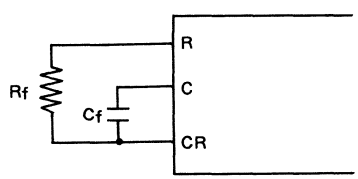
Note 8: Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

Note 9: The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

The relationship between the operating frequency and the power dissipation is given below.

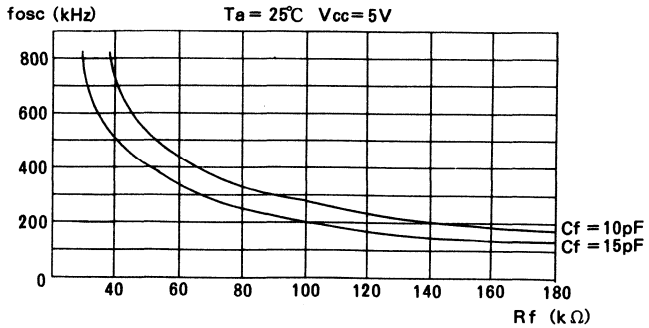


Note 10: Applied to the operation of internal oscillator when oscillation resistor Rf and oscillation capacity Cf are used.

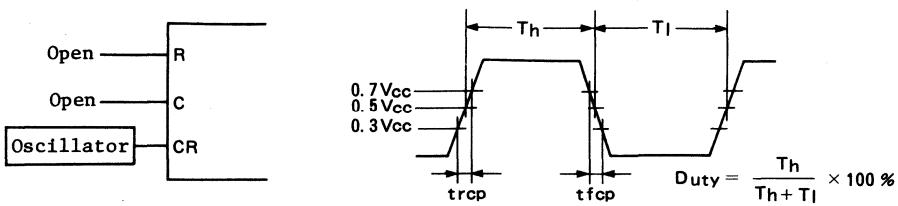


C_f = 15pF ± 5%
R_f = 39kΩ ± 2%
(when fosc = 500kHz typ)

The relationship among oscillation frequency, Rf and Cf is given below.



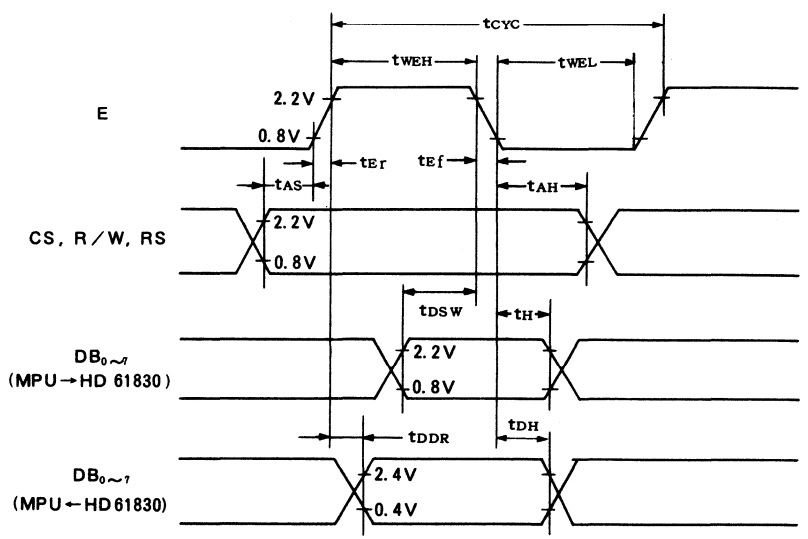
Note 11: Applied to external clock operation.



Note 12: Applied to $\overline{SYNC}$, DB0∿DB7, and RD0∿RD7.

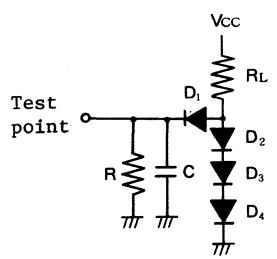
■TIMING CHARACTERISTICS

●Bus Read/Write Operation (Interface to MPU)



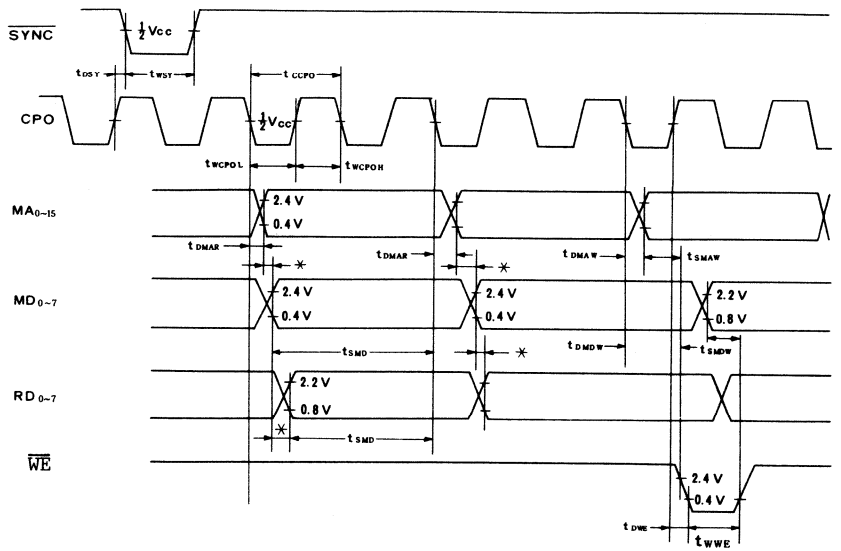
Item		Symbol	Min.	Typ	Max.	Unit	
Enable cycle time		t_{CYC}	1.0	-	-	µs	
Enable pulse width	"High" level	t_{WEH}	0.45	-	-	µs	
	"Low" level	t_{WEL}	0.45	-	-	µs	
Enable rise time		t_{Er}	-	-	25	ns	
Enable fall time		t_{Ef}	-	-	25	ns	
Setup time		t_{AS}	140	-	-	ns	
Data setup time		t_{DSW}	225	-	-	ns	
Data delay time		t_{DDR}	-	-	225	ns	Note
Data hold time		t_H	10	-	-	ns	
Address hold time		t_{AH}	10	-	-	ns	
Data hold time		t_{DH}	20	-	-	ns	

Note: The following load circuit is connected for specification:



R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF
Diodes D1 to D4: 1S2074 Ⓗ

●Interface to External RAM and ROM

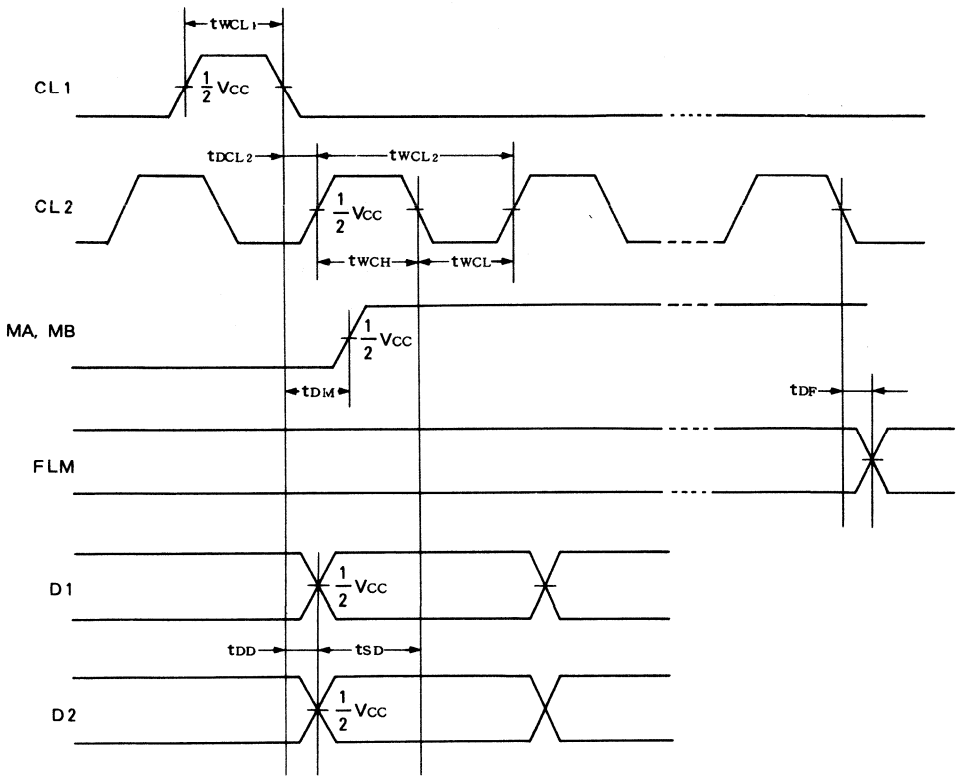


Item		Symbol	Min.	Typ	Max.	Unit
$\overline{\text{SYNC}}$ delay time		t_{DSY}	-	-	200	ns
$\overline{\text{SYNC}}$ pulse width	"High" level	t_{WSY}	900	-	-	ns
CPO cycle time		t_{CCPO}	900	-	-	ns
CPO pulse width	"High" level	t_{WCPOH}	450	-	-	ns
	"Low" level	t_{WCPOL}	450	-	-	ns
MA0 to MA15 refresh delay time		t_{DMAR}	-	-	200	ns
MA0 to MA15 write address delay time		t_{DMAW}	-	-	200	ns
MD0 to MD7 write data delay time		t_{DMDW}	-	-	200	ns
MD0 to MD7, RD0 to RD7 setup time		t_{SMD}	900	-	-	ns
Memory address setup time		t_{SMAW}	250	-	-	ns
Memory data setup time		t_{SMDW}	250	-	-	ns
$\overline{\text{WE}}$ delay time		t_{DWE}	-	-	200	ns
$\overline{\text{WE}}$ pulse width ("Low" level)		t_{WWE}	450	-	-	ns

Note 1: No load is applied to all the output terminals.

Note 2: "*" indicates the delay time of RAM and ROM.

● Data Transfer to Driver LSI



Item		Symbol	Min.	Typ	Max.	Unit
Clock pulse width ("High" level)		t_{WCL1}	450	–	–	ns
Clock delay time		t_{DCL2}	–	–	200	ns
Clock cycle time		t_{WCL2}	900	–	–	ns
Clock pulse width	"High" level	t_{WCH}	450	–	–	ns
	"Low" level	t_{WCL}	450	–	–	ns
MA, MB delay time		t_{DM}	–	–	300	ns
FLM delay time		t_{DF}	–	–	300	ns
Data delay time		t_{DD}	–	–	200	ns
Data setup time		t_{SD}	250	–	–	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D1 and D2).

● Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

(1) Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character display (Character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/ slave	Blink	Cursor	Graphic/ character mode	Ext./ Int.CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

(2) Set character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p - 1) binary				0	(H_p - 1) binary		

Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

The Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	" 7
8	1	1	1	" 8

(3) Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(H_N - 1) binary						

H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = Hp \times H_N$$

H_N can be set with an even number of 2 to 128 (decimal).

(4) Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time shares reg.	0	0	0	(Nx - 1) binary						

Nx indicates the number of time division in multiplex display.

1/Nx is a display duty ratio.

A value of 1 to 128 (decimal) can be set to Nx.

(5) Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(Cp - 1) binary			

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying Cp=8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the number of vertical character pitches Vp is set ($Cp \leqq Vp$), and a character is overlapped with the cursor, the cursor has higher priority of display (at cursor display ON). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

(6) Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

(7) Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address ($DB_3 \sim DB_0$) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

(8) Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

(9) Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. Namely, data at address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the digit specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements. When setting the cursor address.

1.	When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
2.	When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.

3.	When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

The cursor address counter is a 16 bit up-counter with SET and RESET functions. When the bit N changes from 1 to 0, the bit N+1 is added by 1. When setting the low order address, the LSB (bit 1) of the high order address is added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in above table.

(10) Write display data

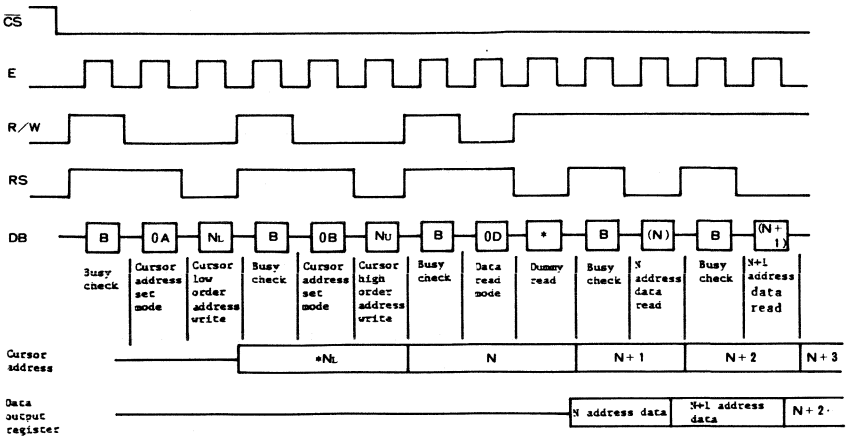
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

After the code $'0C' is written into the instruction register with RS=1, 8 bit data with RS=0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

(11) Read display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

Data can be read from the RAM with RS=0 after writing code $'0D' into the instruction register. The read procedure is as follows:



This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second time. Thus, make one dummy read when reading data after setting the cursor address.

(12) Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B - 1) binary		

(13) Set bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B - 1) binary		

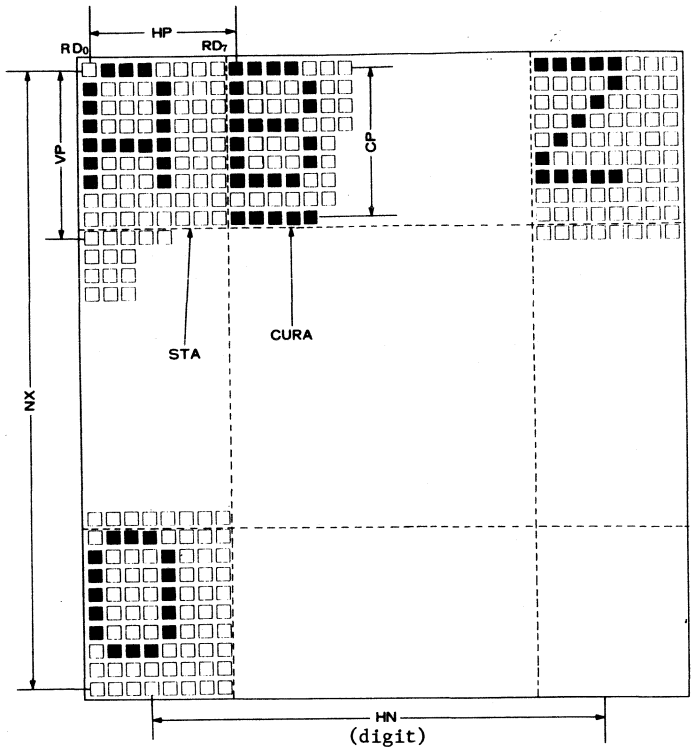
The Clear/Set Bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value of 1 to 8. N_B=1 and N_B=8 indicates LSB and MSB, respectively.

(14) Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0							

When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instructions (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag=1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS=1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1.

The busy flag can be read without specifying any instruction register.

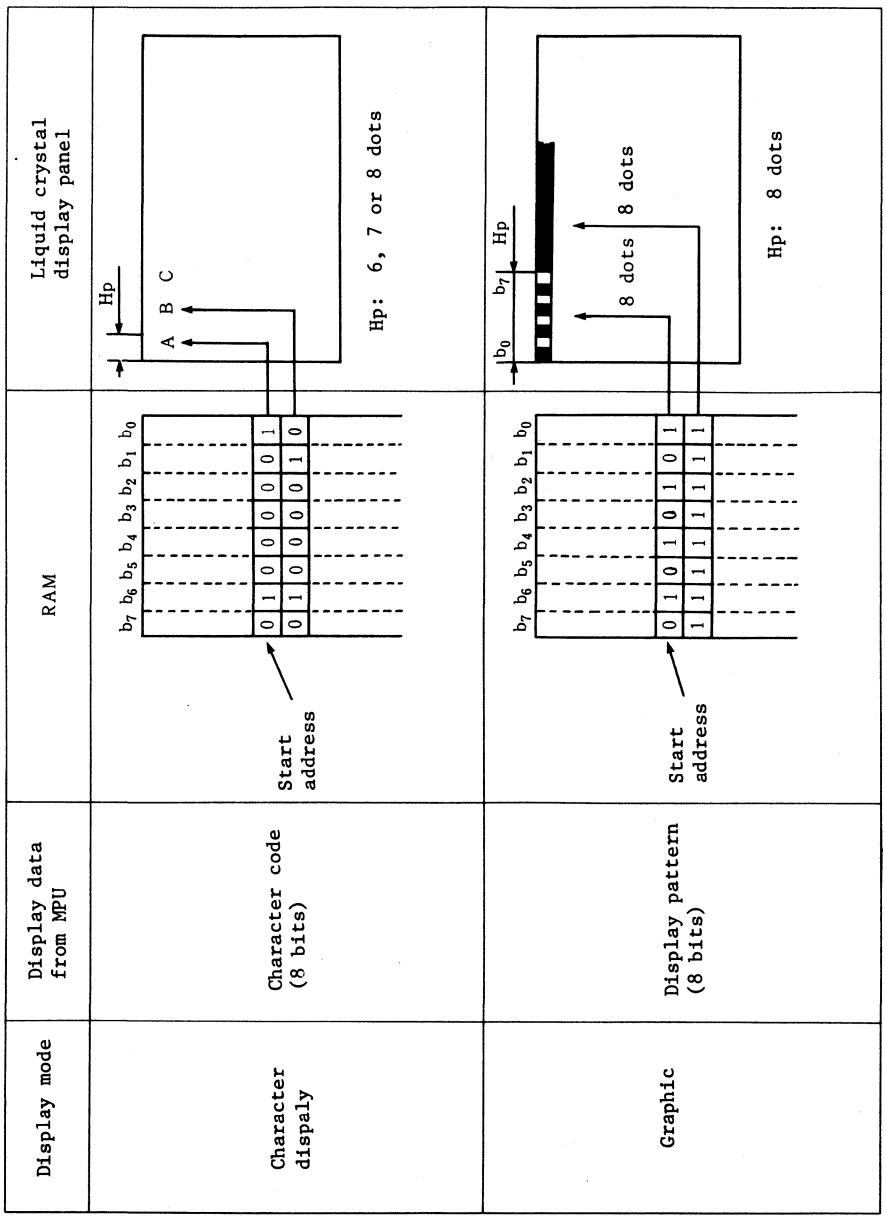


Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Lateral character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 128 digits (an even number)
V_p	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_x	Number of time division	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on screen is taken as m, and the number of horizontal dots as n,

$1/m = 1/Nx$ = display duty ratio
$n = Hp \times H_N$, m/Vp = Number of display lines
$C_p \leqq V_p$

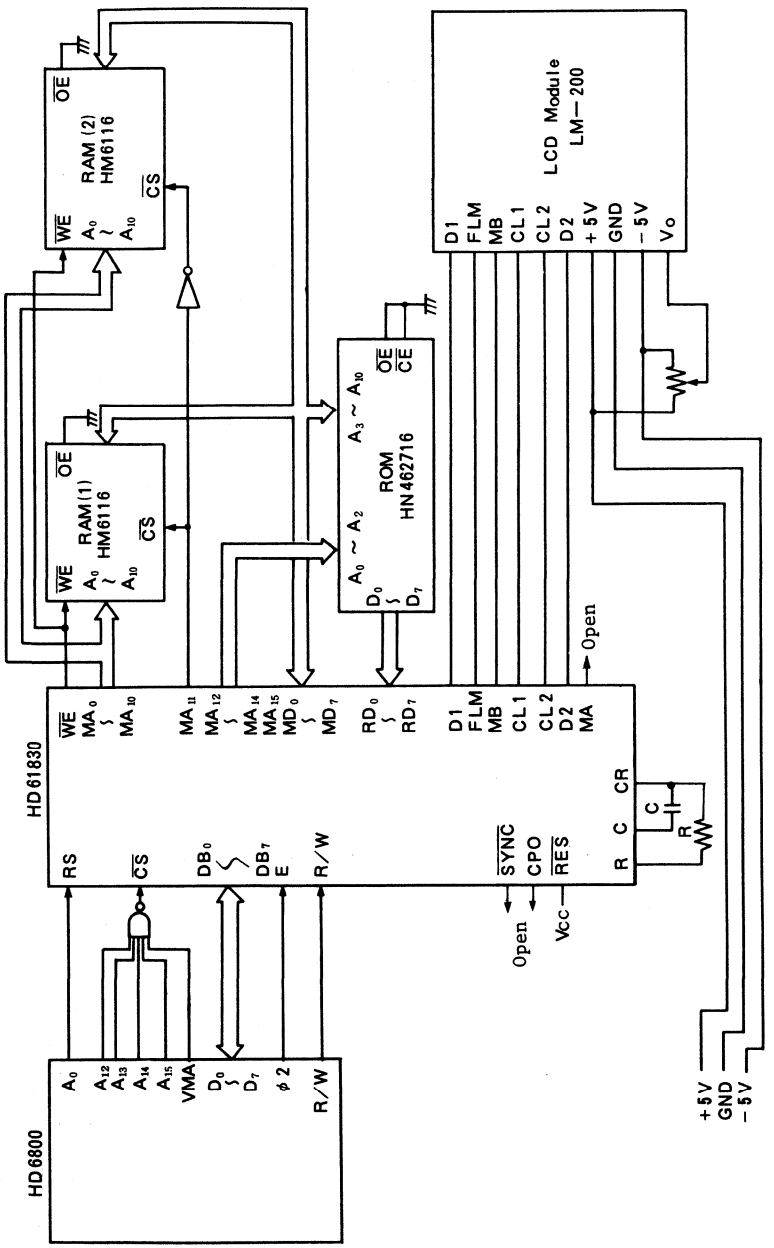
● Display Mode



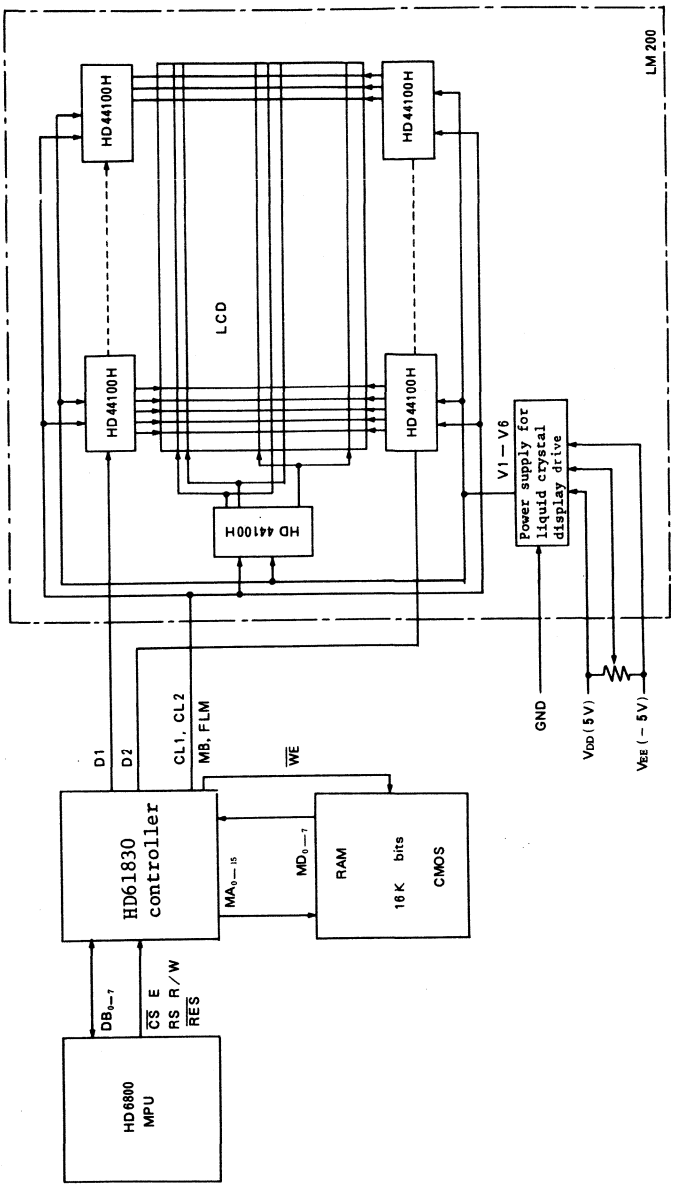
● Internal Character Generator Patterns and Character Codes

Lower 4bit \ Higher 4bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000												
xxxx0001												
xxxx0010												
xxxx0011												
xxxx0100												
xxxx0101												
xxxx0110												
xxxx0111												
xxxx1000												
xxxx1001												
xxxx1010												
xxxx1011												
xxxx1100												
xxxx1101												
xxxx1110												
xxxx1111												

■APPLICATION (CHARACTER MODE, EXTERNAL CG, CHARACTER FONT 8×8)

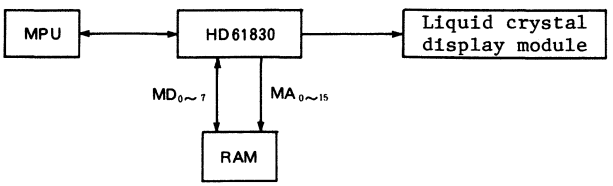


■APPLICATION (GRAPHIC MODE)

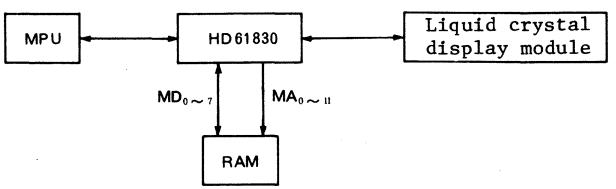


■EXAMPLE OF CONFIGURATION

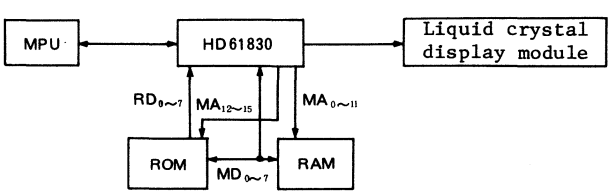
●Graphic Mode



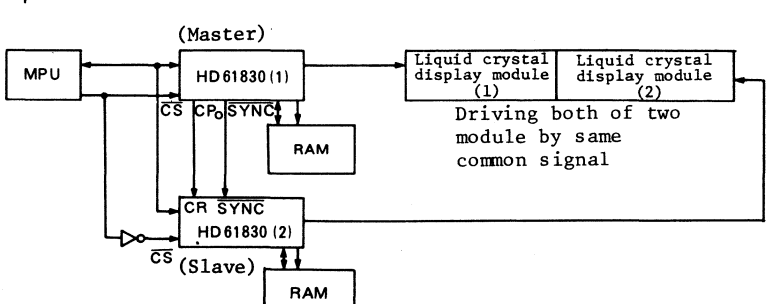
●Character Mode (1) (Internal Character Generator)



●Character Mode (2) (External Character Generator)



●Parallel Operation

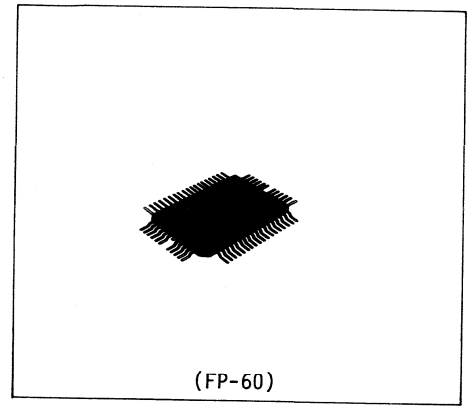


HD61830B
(Dot Matrix Liquid Crystal Graphic Display Controller)

The HD61830B is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

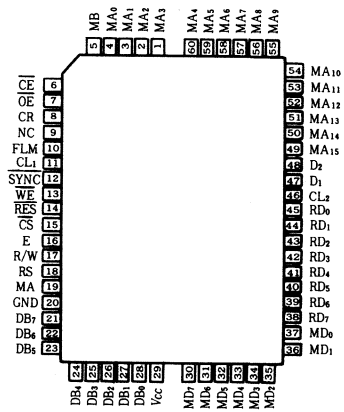
It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830B is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power dissipation.



(FP-60)

PIN ARRANGEMENT

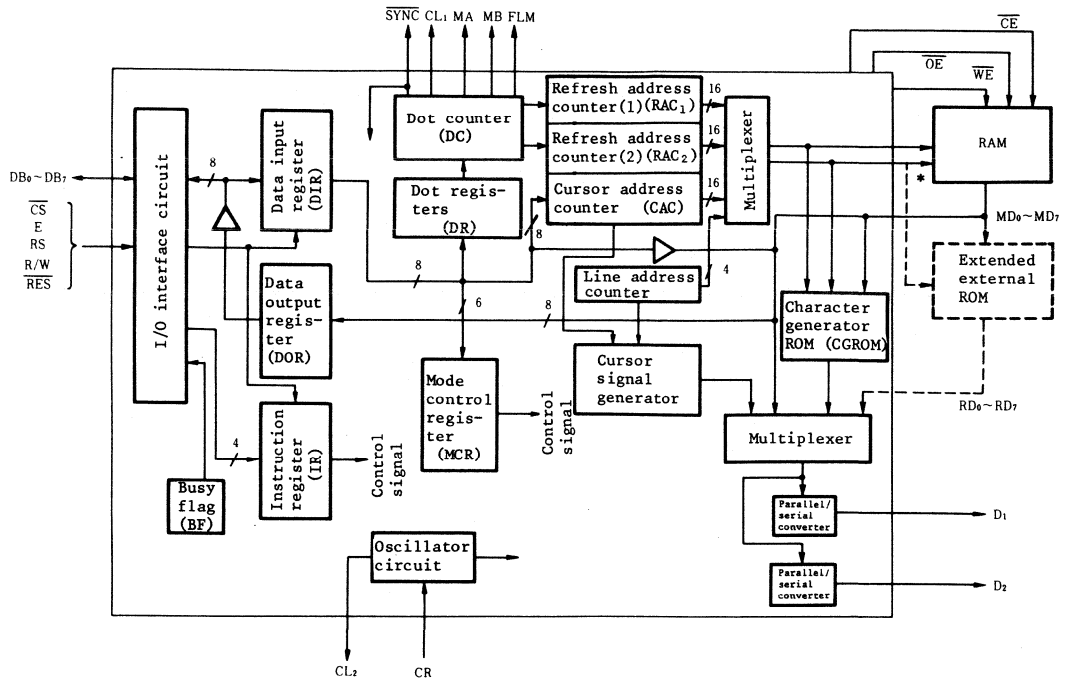


(Top View)

FEATURES

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - Graphic mode ..... 512K dots (2^{16} bytes)
  - Character mode ..... 4096 characters (2^{12} characters)
- Internal character generator ROM ..... 7360 bits
  - 160 types of 5×7 dot character fonts
  - 32 types of 5×11 dot character fonts
  - Total 192 types
  - (Can be extended to 256 types (4K bytes max.) by external ROM)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  - Static to 1/128 duty selectable
- Various instruction functions
  - Scroll, Cursor ON/OFF/blink, Character blink, Bit manipulation
- Display method ..... Selectable A or B types
- Operating frequency 2.4MHz
- Low power dissipation
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package

BLOCK DIAGRAM



* When extended external ROM is used MA0 ∿ MA11 are applied to RAM, MA12 ∿ MA15 are applied to extended external ROM.

BLOCK FUNCTIONS

Registers

The HD61830B has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR) and mode control register (MCR).

The IR is a 4-bit register which stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at "High" level).

The DR are registers used to store the dot informations such as character pitches and the number of vertical dots and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display ON/OFF and cursor ON/OFF/blink etc. The information sent from the MPU is written in it via the DIR.

Busy Flag (BF)

With "1", the busy flag indicates the HD61830B is performing an internal operation. The next instruction cannot be accepted. As shown in Control Instruction (14), the busy flag is output on DB7 under the conditions of RS=1, R/W=1 and E=1. Make sure the busy flag is "0" before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

- Refresh Address Counters (RAC1/RAC2)

The refresh address counters are counters used to control the addresses of external RAM, character generator ROM (CGROM) and extened external ROM having the two types: RAC1 and RAC2. The RAC1 is used for upper half of screen and the RAC2 for lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12 ∿ MA15) are ignored. The 4 bits of line address counter are output instead of it and used as the address of extended ROM.

- Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 types) or 5×11 (32 types). The use of extended ROM allows 8×16 (256 types max.) to be used.

- Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by the instruction. It is used to hold an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of cursor address counter is automatically increased by 1 after the display data is read or written and after the Set/Clear Bit instruction is executed.

- Cursor Signal Generator

The cursor can be displayed by the instruction in the character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

- Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

TERMINAL FUNCTIONS

Name	Function
DB0∿7	Data bus ... Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{CS}$	Chip select ... Selected state with $\overline{CS}$=0.
R/W	Read/Write ... R/W=1 ... MPU ← HD61830B R/W=0 ... MPU → HD61830B
RS	Register select ... RS=1 ... Instruction register RS=0 ... Data register
E	Enable ... Data is written at the fall of E. Data can be read while E is 1.
CR	External clock input.
$\overline{RES}$	Reset ... $\overline{RES}$=0 results in display OFF, slave mode and Hp=6.
MA0∿15	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 ("0": Character 1st line, "F": Character 16th line).
MD0∿7	Display data bus ... Three-state I/O common terminal.
RD0∿7	ROM data input ... Dot data from external character generator is input.
$\overline{WE}$	Write enable ... Write signal for external RAM.
CL2	Display data shift clock for LCD drivers.
CL1	Display data latch signal for LCD drivers.
FLM	Frame signal for display synchronization.
MA	Signal for converting liquid crystal driving signal into AC, A type.
MB	Signal for converting liquid crystal driving signal into AC, B type.
D1, D2	Display data serial output D1 ... For upper half of screen D2 ... For lower half of screen
$\overline{SYNC}$	Synchronous signal for parallel operation. Three-state I/O common terminal (with pull-up MOS). Master ... Synchronous signal is output. Slave .... Synchronous signal is input.

-to be continued

Name	Function
$\overline{CE}$	Chip enable $\overline{CE}$=0 ... Chip enable make external RAM in active.
$\overline{OE}$	Output enable $\overline{OE}$=1 ... Output enable informs external RAM that HD61830B requires data bus.
NC	Unused terminal. Don't connect any wires to this terminal.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	1,2
Terminal voltage	V_T	-0.3 ∿ V_{CC}+0.3	V	1,2
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: All voltage is referred to GND=0V.

Note 2: If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI's within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, GND=0V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	Note
Input "High" voltage (TTL)	V_{IH}		2.2	-	V_{CC}	V	1
Input "Low" voltage (TTL)	V_{IL}		0	-	0.8	V	2
Input "High" voltage	VIHR		3.0	-	V_{CC}	V	3
Input "High" voltage (CMOS)	V_{IHC}		0.7V_{CC}	-	V_{CC}	V	4
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3V_{CC}	V	4
Output "High" voltage (TTL)	V_{OH}	$-I_{OH}$=0.6mA	2.4	-	V_{CC}	V	5
Output "Low" voltage (TTL)	V_{OL}	I_{OL}=1.6mA	0	-	0.4	V	5
Output "High" voltage(CMOS)	V_{OHC}	$-I_{OH}$=0.6mA	V_{CC}-0.4	-	V_{CC}	V	6
Output "Low" voltage (CMOS)	V_{OLC}	I_{OL}=0.6mA	0	-	0.4	V	6
Input leakage current	I_{IN}	V_{IN}=0∿V_{CC}	-5	-	5	µA	7
Three-state leakage current	I_{TSL}	V_{OUT}=0∿V_{CC}	-10	-	10	µA	8
Pull-up current	I_{PL}	Vin=GND	2	10	20	µA	9
Power dissipation	P_W	External clock fcp=2.4MHz	-	-	50	mW	10

Note 1: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR and $\overline{RES}$.

Note 2: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.

Note 3: Applied to terminal $\overline{RES}$.

Note 4: Applied to terminals $\overline{SYNC}$ and CR.

Note 5: Applied to terminals DB0∿DB7, $\overline{WE}$, MA0∿MA15, $\overline{OE}$, $\overline{CE}$, and MD0∿MD7.

Note 6: Applied to terminals $\overline{SYNC}$, FLM, CL1, CL2, D1, D2, MA and MB.

Note 7: Applied to input terminals.

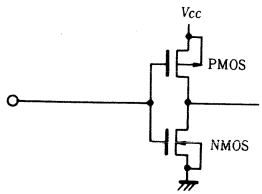
Note 8: Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

Note 9: Applied to $\overline{SYNC}$, DB0∿DB7, and RD0∿RD7.

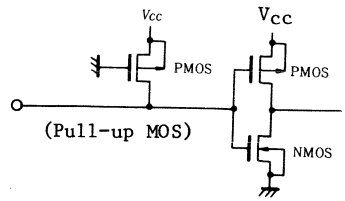
Note 10: The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

● Shape of Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (Without pull-up MOS)

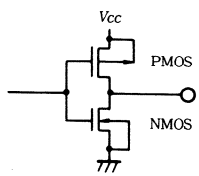


Applicable terminal: RD0∿RD7 (With pull-up MOS)



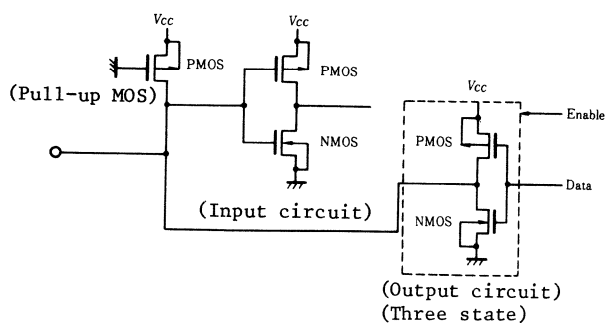
● Shape of Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, D1, D2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA0∿MA15



● Shape of I/O Common Terminal

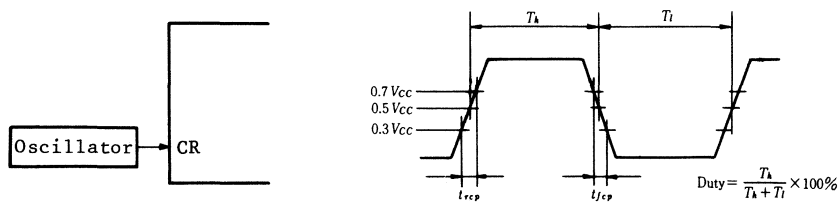
Applicable terminal: DB0∿DB7, $\overline{SYNC}$, MD0∿MD7 (MD0∿MD7 have no pull-up MOS)



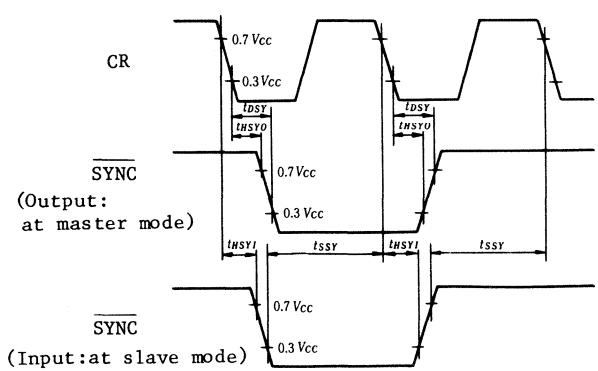
● Clock Operation

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	Note
External clock operating frequency	f_{cp}		100	-	2400	kHz	1
External clock duty	Duty		47.5	50	52.5	%	1
External clock rise time	t_{rcp}		-	-	25.0	ns	1
External clock fall time	t_{fcp}		-	-	25.0	ns	1
$\overline{SYNC}$ output hold time	t_{HSYO}		30	-	-	ns	2, 3
$\overline{SYNC}$ output delay time	t_{DSY}		-	-	210	ns	2, 3
$\overline{SYNC}$ input hold time	t_{HSYI}		10	-	-	ns	2
$\overline{SYNC}$ input set-up time	t_{SSY}		-	-	180	ns	2

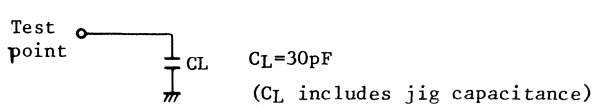
Note 1: Applied to external clock input terminal.



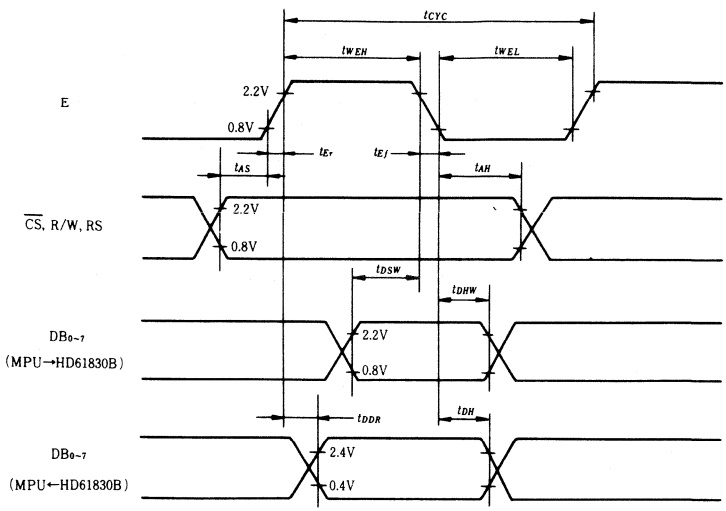
Note 2: Applied to $\overline{SYNC}$ terminal.



Note 3: Testing load circuit.

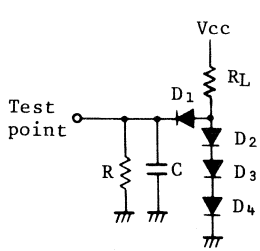


● Bus Read/Write Operation (Interface to MPU)



Item		Symbol	Min.	Typ.	Max.	Unit
Enable cycle time		t_{CYC}	1.0	-	-	µs
Enable pulse width	"High" level	t_{WEH}	0.45	-	-	µs
	"Low" level	t_{WEL}	0.45	-	-	µs
Enable rise time		t_{Er}	-	-	25	ns
Enable fall time		t_{Ef}	-	-	25	ns
Setup time		t_{AS}	140	-	-	ns
Data setup time		t_{DSW}	225	-	-	ns
Data delay time		t_{DDR}	-	-	225	ns(Note)
Data hold time		t_{DHW}	10	-	-	ns
Address hold time		t_{AH}	10	-	-	ns
Data hold time		t_{DH}	20	-	-	ns

Note: The following load circuit is connected for specification:

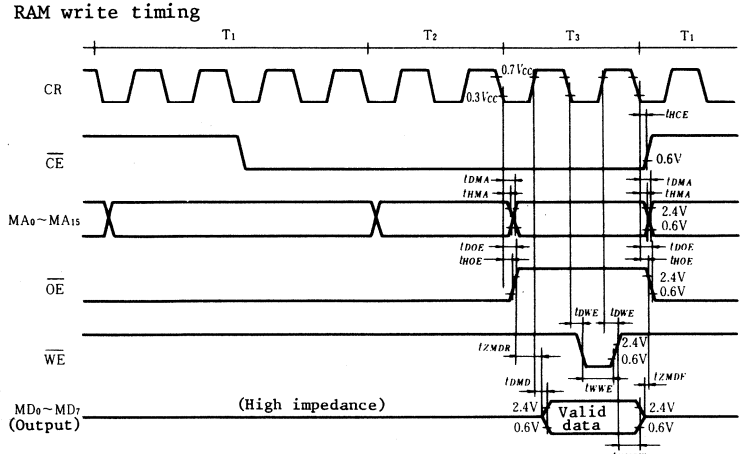


R_L = 2.4kΩ
R = 11kΩ
C = 130 pF (C includes jig capacitance)
Diodes D1 to D4: 1S2074 Ⓗ

● Interface to External RAM and ROM

Item	Symbol	Test condition	Min.	Typ.	Max.	unit	Note
MA0∿MA15 delay time	t_{DMA}		-	-	300	ns	1, 2, 3
MA0∿MA15 hold time	t_{HMA}		40	-	-	ns	1, 2, 3
$\overline{CE}$ delay time	t_{DCE}		-	-	300	ns	1, 2, 3
$\overline{CE}$ hold time	t_{HCE}		40	-	-	ns	1, 2, 3
$\overline{OE}$ delay time	t_{DOE}		-	-	300	ns	1, 3
$\overline{OE}$ hold time	t_{HOE}		40	-	-	ns	1, 3
MD output delay time	t_{DMD}		-	-	150	ns	1, 3
MD output hold time	t_{HMDW}		10	-	-	ns	1, 3
$\overline{WE}$ delay time	t_{DWE}		-	-	150	ns	1, 3
$\overline{WE}$ clock pules width	t_{WWE}		150	-	-	ns	1, 3
MD output high impedance time (1)	t_{ZMDF}		10	-	-	ns	1, 3
MD output high impedance time (2)	t_{ZMDR}		50	-	-	ns	1, 3
RD data set-up time	t_{SRD}		50	-	-	ns	2
RD data hold time	t_{HRD}		40	-	-	ns	2
MD data set-up time	t_{SMD}		50	-	-	ns	2
MD data hold time	t_{HMD}		40	-	-	ns	2

Note 1: RAM write timing

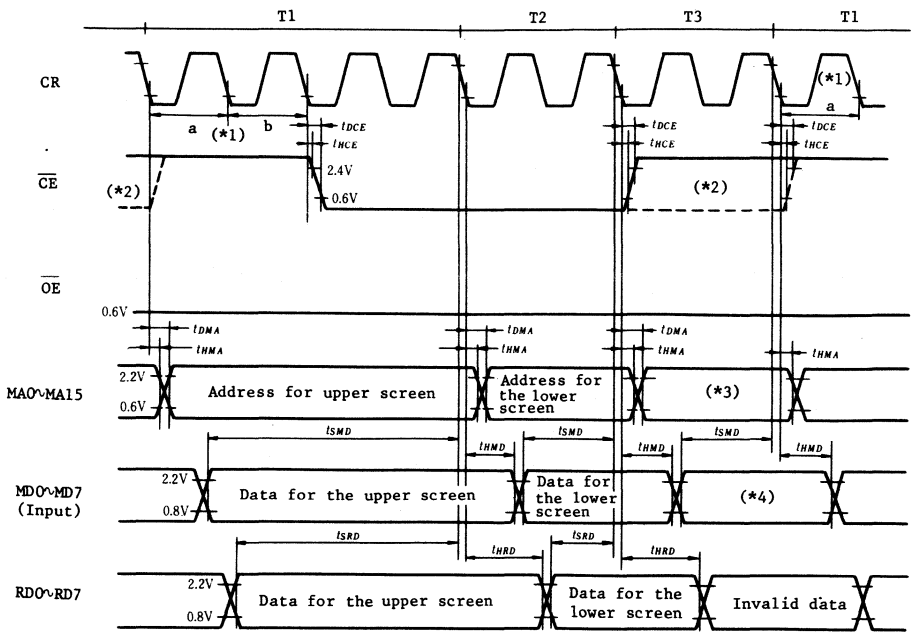


T1: Memory data refresh timing for upper screen

T2: Memory data refresh timing for lower screen

T3: Memory read/write timing

Note 2: ROM/RAM read timing



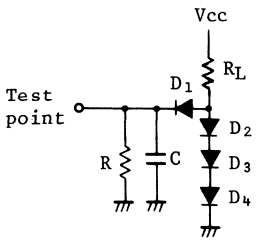
(*1) This figure shows the timing in the case of Hp=8.
In the case of Hp=7, time shown by "b" becomes zero., and in the case of Hp=6, time shown by "a" and "b" becomes zero. Therefore, the number of clock pulse during Tl become 4, 3 or 2 in the case of Hp=8, Hp=7 or Hp=6 respectively.

(*2) The waveform in the case of instruction with memory read is shown with a dash line. In other case, the waveform shown with a solid line is generated.

(*3) When the instruction with RAM read/write is excuted, the value of cursor address is output. In other case, invalid data is output.

(*4) When the instruction with RAM read is excuted, HD61830B latch the data at this timing. In other case, this data is invalid.

Note 3: Test load circuit



R_L=2.4kΩ

R =11kΩ

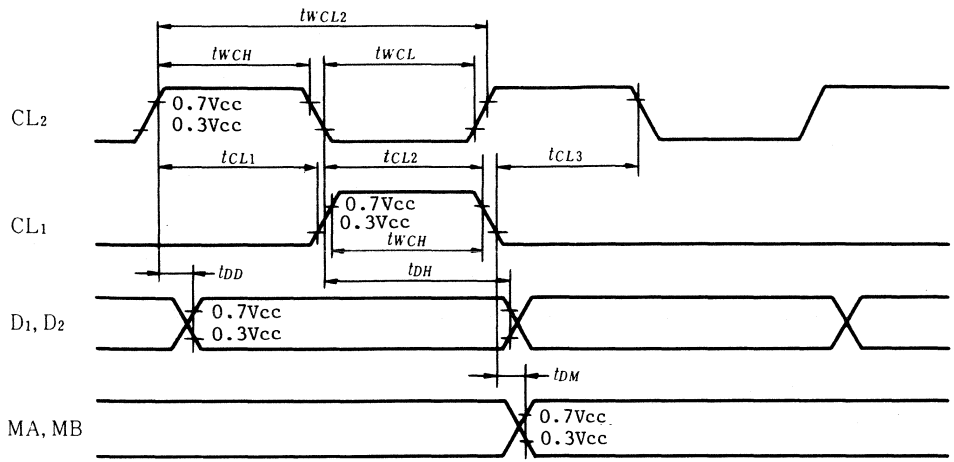
C =50 pF (C includes jig capacitance)

Diodes D1 to D4: 1S2074Ⓗ

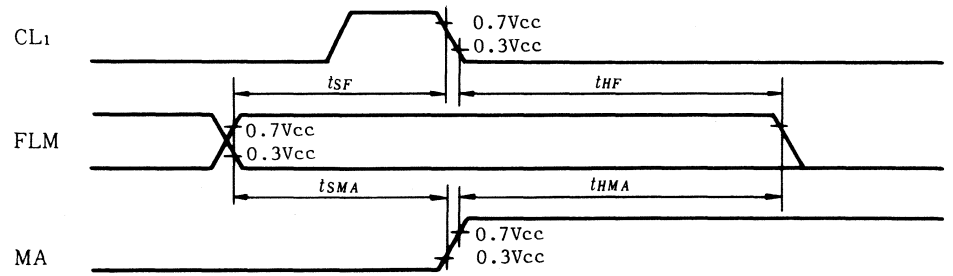
● Data Transfer to Driver LSI

Items	Symbol	Test condition	Min.	Typ.	Max	Unit	Note
Clock cycle time	t_{WCL2}		416	-	-	ns	1, 3
Clock pulse width (High level)	t_{WCH}		150	-	-	ns	1, 3
Clock pulse width (Low level)	t_{WCL}		150	-	-	ns	1, 3
Data delay time	t_{DD}		-	-	50	ns	1, 3
Data hold time	t_{DH}		100	-	-	ns	1, 3
Clock phase difference (1)	t_{CL1}		100	-	-	ns	1, 3
Clock phase difference (2)	t_{CL2}		100	-	-	ns	1, 3
Clock phase difference (3)	t_{CL3}		100	-	-	ns	1, 3
MA, MB delay time	t_{DM}		-200	-	200	ns	1, 3
FLM set-up time	t_{SF}		400	-	-	ns	2, 3
FLM hold time	t_{HF}		1000	-	-	ns	2, 3
MA set-up time	t_{SMA}		400	-	-	ns	2, 3
MA hold time	t_{HMA}		1000	-	-	ns	2, 3

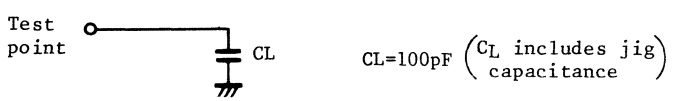
Note 1:



Note 2:



Note 3: Test load circuit



● Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

(1) Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character display (Character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/ slave	Blink	Cursor	Graphic/ character mode	Ext./ Int.CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

(2) Set character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p-1) binary				0	(Hp-1) binary		

Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

The Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	Horizontal character pitch 7
8	1	1	1	Horizontal character pitch 8

(3) Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(H_N - 1) binary						

H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = Hp \times H_N$$

H_N can be set with an even number of 2 to 128 (decimal).

(4) Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time shares reg.	0	0	0	(Nx - 1) binary						

Nx indicates the number of time division in multiplex display.
1/Nx is a display duty ratio.

A value of 1 to 128 (decimal) can be set to Nx.

(5) Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(Cp - 1) binary			

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying Cp=8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the number of vertical character pitches Vp is set (Cp≦Vp), and a character is overlapped with the cursor, the cursor has higher priority of display (at cursor display ON). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

(6) Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

(7) Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address ($DB_3 \sim DB_0$) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

(8) Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

(9) Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. Namely, data at address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the digit specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements. When setting the cursor address.

1.	When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
2.	When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.
3.	When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

The cursor address counter is a 16 bit up-counter with SET and RESET functions. When the bit N changes from 1 to 0, the bit N+1 is added by 1. When setting the low order address, the LSB (bit 1) of the high order address is added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in above table.

(10) Write display data

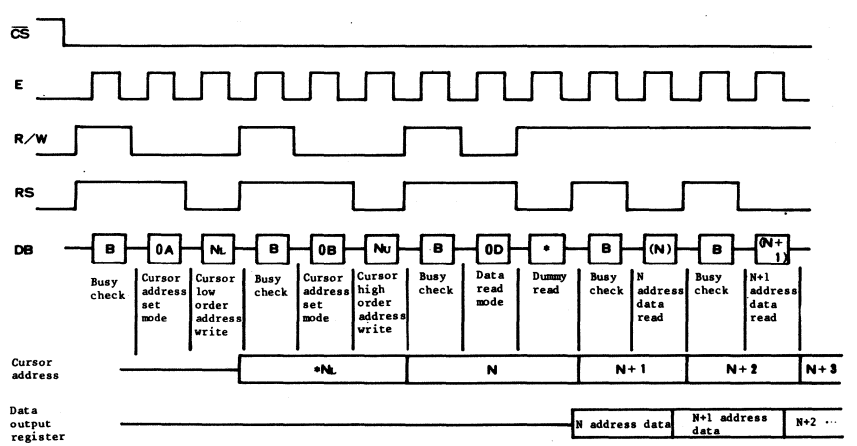
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

After the code $'0C' is written into the instruction register with RS=1, 8 bit data with RS=0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

(11) Read display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

Data can be read from the RAM with RS=0 after writing code $'0D' into the instruction register. The read procedure is as follows:



This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second time. Thus, make one dummy read when reading data after setting the cursor address.

(12) Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B-1)binary		

(13) Set bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B-1) binary		

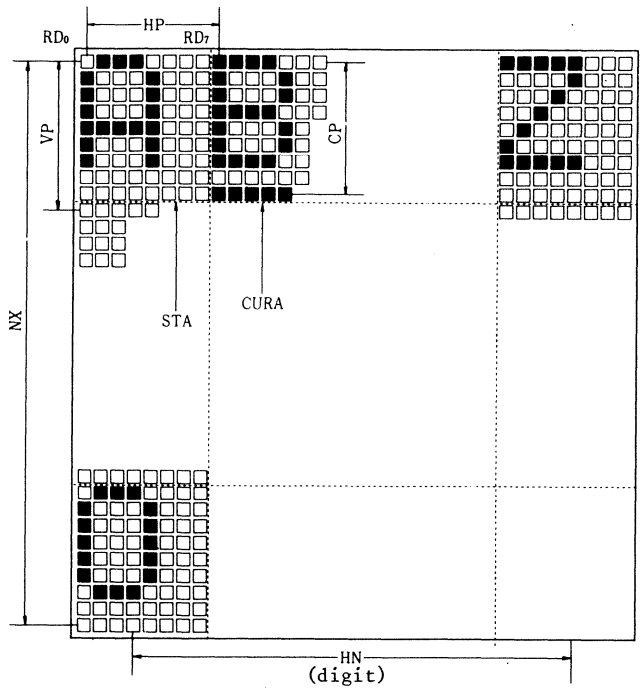
The Clear/Set Bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value of 1 to 8. N_B=1 and N_B=8 indicates LSB and MSB, respectively.

(14) Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0	*						

When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instructions (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag=1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS=1), busy flag doesn't change. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1.

The busy flag can be read without specifying any instruction register.



Symbol	Name	Meaning	Value
Hp	Horizontal character Pitch	Lateral character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 128 digits (an even number)
Vp	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
Cp	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
Nx	Number of time division	Inverse of display duty ratio	1 to 128 lines

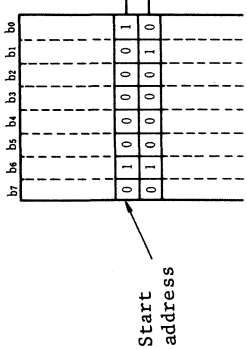
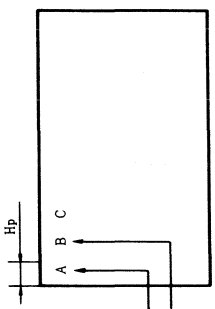
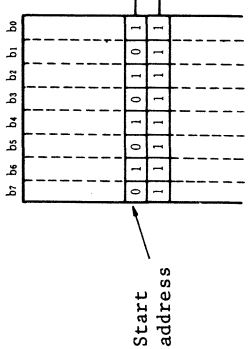
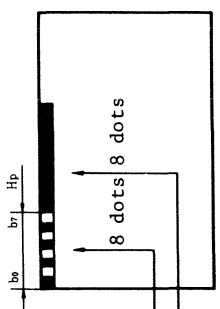
Note: if the number of vertical dots on screen is taken as m, and the number of horizontal dots as n,

$1/m = 1/Nx$ = display duty ratio

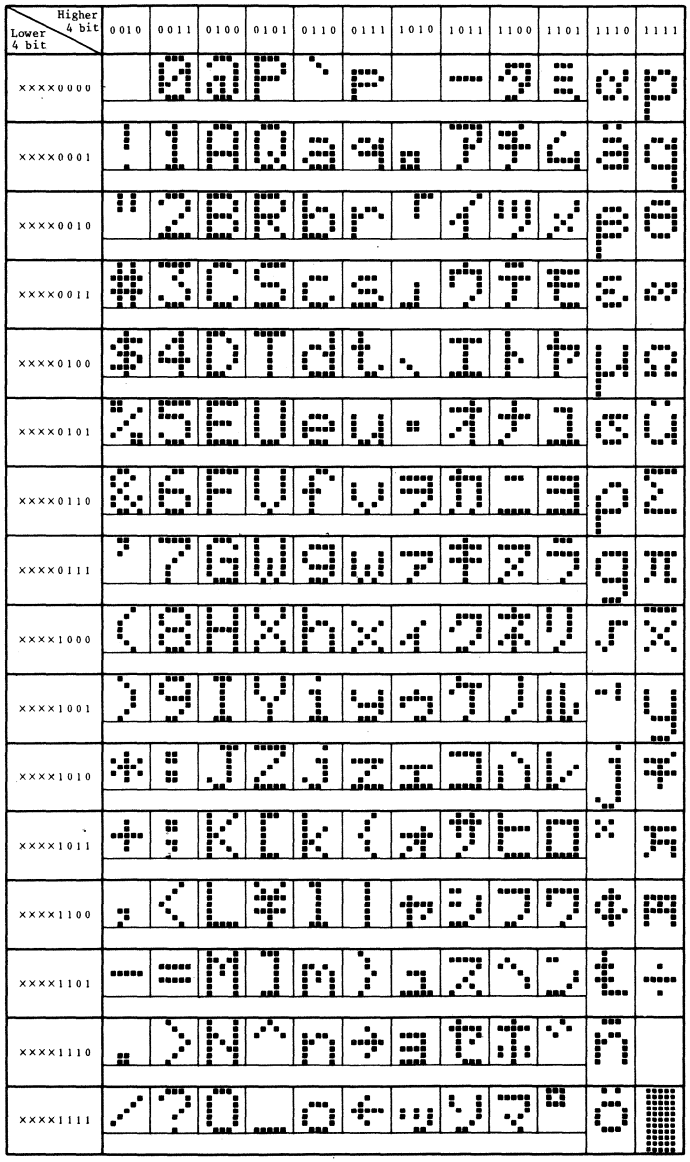
$n = Hp \times H_N$, m/Vp = Number of display lines

$Cp \leq Vp$

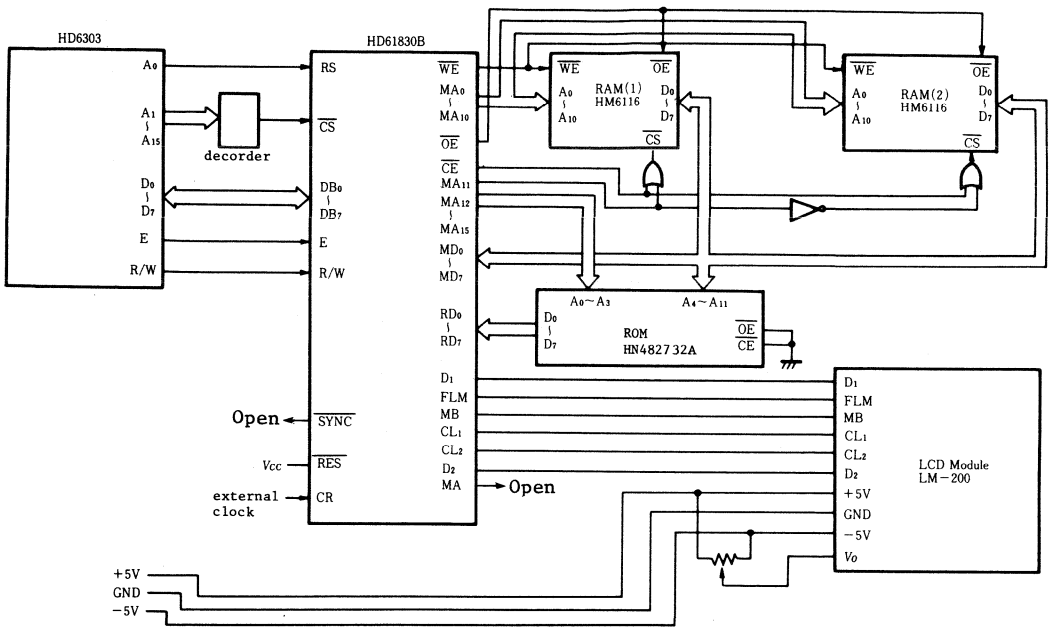
● Display Mode

Display mode	Display data from MPU	RAM	Liquid crystal display panel
Character display	Character code (8 bits)		
Graphic	Display pattern (8 bits)		

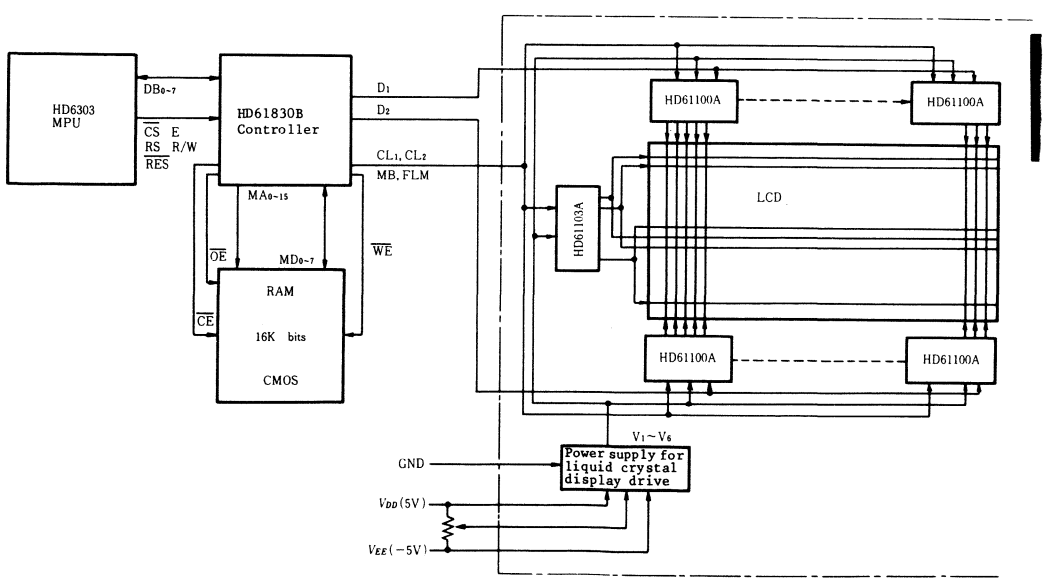
● Internal Character Generator Patterns and Character Codes



APPLICATION (CHARACTER MODE, EXTERNAL CG, CHARACTER FONT 8X8)

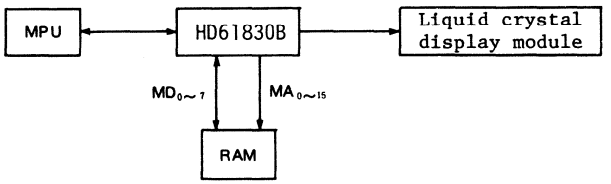


APPLICATION (GRAPHIC MODE)

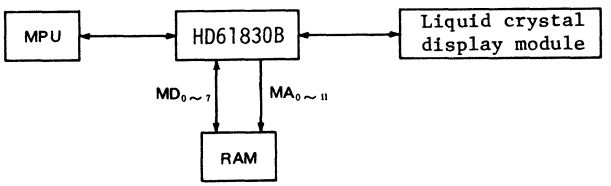


■EXAMPLE OF CONFIGURATION

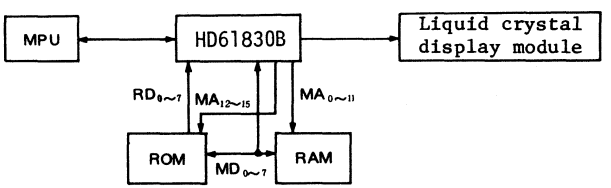
●Graphic Mode



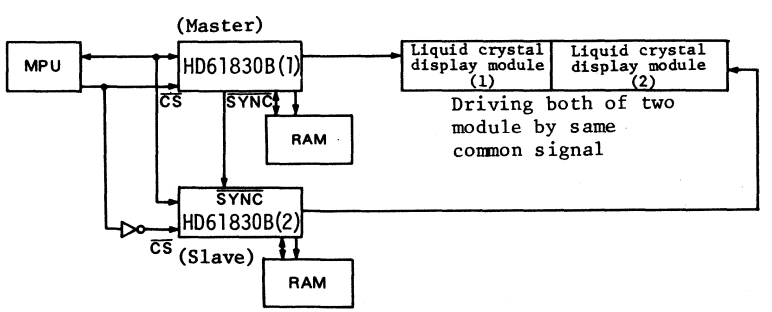
●Character Mode (1) (Internal Character Generator)



●Character Mode (2) (External Character Generator)



●Parallel Operation



HD63645/HD64645

LCD Timing Controller (LCTC)

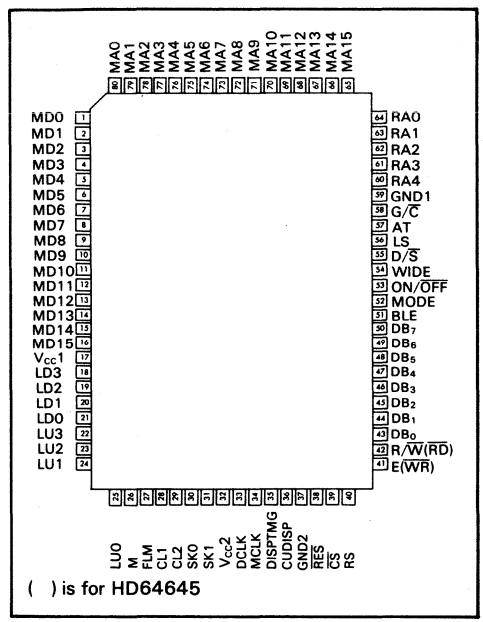
Description

The HD63645/HD64645 LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



( ) is for HD64645

Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/sec in character mode
  —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106
- CPU interface: 68 family (HD63645), 80 family (HD64645)
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	80-pin Plastic QFP (FP-80)
HD64645	4 MHz	80 System	80-pin Plastic QFP (FP-80)
HD64646	4MHz	80 System	80-pin Plastic QFP (FP-80A)

Note: See HD64646 data sheet is this data book.

Pin Description

Symbol	Pin Number	Name	I/O
$V_{CC}1$, $V_{CC}2$	17, 32	V_{CC}	—
GND1, GND2	37, 59	Ground	—
LU0-LU3	22-25	LCD Up Panel Data 0-3	O
LD0-LD3	18-21	LCD Down Panel Data 0-3	O
CL1	28	Clock One	O
CL2	29	Clock Two	O
FLM	27	First Line Marker	O
M	26	M	O
MA0-MA15	65-80	Memory Address 0-15	O
RA0-RA4	60-64	Raster Address 0-4	O
MD0-MD7	1-8	Memory Data 0-7	I
MD8-MD15	9-16	Memory Data 8-15	I
DB_0-DB_7	43-50	Data Bus 0-7	I/O
$\overline{CS}$	39	Chip Select	I
E	41	Enable (HD63645 Only)	I
R/$\overline{W}$	42	Read/Write (HD63645 Only)	I
$\overline{WR}$	41	Write (HD64645 Only)	I
$\overline{RD}$	42	Read (HD64645 Only)	I
RS	40	Register Select	I
$\overline{RES}$	38	Reset	I
DCLK	33	D Clock	I
MCLK	34	M Clock	O
DISPTMG	35	Display Timing	O
CUDISP	36	Cursor Display	O
SK0	30	Skew 0	I
SK1	31	Skew 1	I
ON/$\overline{OFF}$	53	On/Off	I
BLE	51	Blink Enable	I
AT	57	Attribute	I
G/$\overline{C}$	58	Graphic/Character	I
WIDE	54	Wide	I
LS	56	Large Screen	I
D/$\overline{S}$	55	Dual/Single	I
MODE	52	Mode	I

Pin Functions

Power Supply ($V_{CC}1$, 2, GND)

Power Supply Pin (+5 V): Connect $V_{CC}1$ and $V_{CC}2$ with +5 V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0 V.

LCD Interface

LCD Up Panel Data (LU0-LU3), LCD Down Panel Data (LD0-LD3): LU0-LU3 and LD0-LD3 output LCD data as shown in table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0-MA15): MA0-MA15 supply the display memory address.

Raster Address (RA0-RA4): RA0-RA4 supply the raster address.

Memory Data (MD0-MD7): MD0-MD7 receive the character dot data and bit-mapped data.

Memory Data (MD8-MD15): MD8-MD15 receive attribute code data and bit-mapped data.

MPU Interface

Data Bus (DB0-DB7): DB0-DB7 send/receive data as a three-state I/O common bus.

Chip Select ($\overline{CS}$): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock. (HD63645F only).

Read/Write (R/$\overline{W}$): R/$\overline{W}$ enables MPU read of the LCTC internal registers when R/$\overline{W}$ is high, and MPU write when low. (HD63634F only).

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write signal. (HD64645F Only)

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read signal. (HD64645F Only)

Register Select (RS): RS selects registers. (Refer to table 5.)

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor Display (CUDISP): CUDISP supplies cursor display timing; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to table 2.

Mode Select

The mode select pins ON/$\overline{OFF}$, BLE, AT, G/$\overline{C}$,

Table 1. LCD Up Panel Data and LCD Down Panel Data

	Single Screen		
Pin name	**4-Bit Data**	**8-Bit Data**	**Dual Screen**
LU0-LU3	Data output	Data output	Data output for upper screen
LD0-LD3	Disconnected	Data output	Data output for lower screen

and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{\text{OFF}}$): ON/$\overline{\text{OFF}}$ switches display on and off. (High = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{\text{C}}$): G/$\overline{\text{C}}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to page 26.

Dual/Single (D/$\overline{\text{S}}$): D/$\overline{\text{S}}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to table 9.)

Table 2. Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Inhibited combination

Function Overview

LCD and CRT Display Systems

Figure 1 shows a system using both LCD and CRT displays.

Main Features of HD63645F/HD64645F

Main features of the LCTC are :

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3. Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen Format	Programmable horizontal scanning cycle by the character clock period Programmable multiplexing duty ratio from static up to 1/512 Programmable number of displayed characters per character row Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor Control	Programmable cursor display position, corresponding to RAM address Programmable cursor height by setting display start/end rasters Programmable blink rate, 1/32 or 1/64 frame rate
	Memory Rewriting	Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory Addressing	16-bit memory address output, up to 64 kbytes x 2 memory accessible DRAM refresh address output
	Paging and Scrolling	Paging by updating start address Horizontal scrolling by the character, by setting horizontal virtual screen width Vertical smooth scrolling by updating display start raster
	Character Attributes	Reverse video, blinking, nondisplay (white or black) character attributes
Application	CRTC Compatible	Facilitates system replacement of CRT display with LCD.
	OR Function	Enables superimposing display of character screen and graphic screen
Configuration	LCTC Configuration	Single 5 V power supply I/O TTL compatible except $\overline{RES}$, MODE, SK0, SK1 Bus connectable with HMCS 6800 family (HD63645) Bus connectable with 80 family (HD64645) CMOS process Internal logic fully static 80-pin flat plastic package

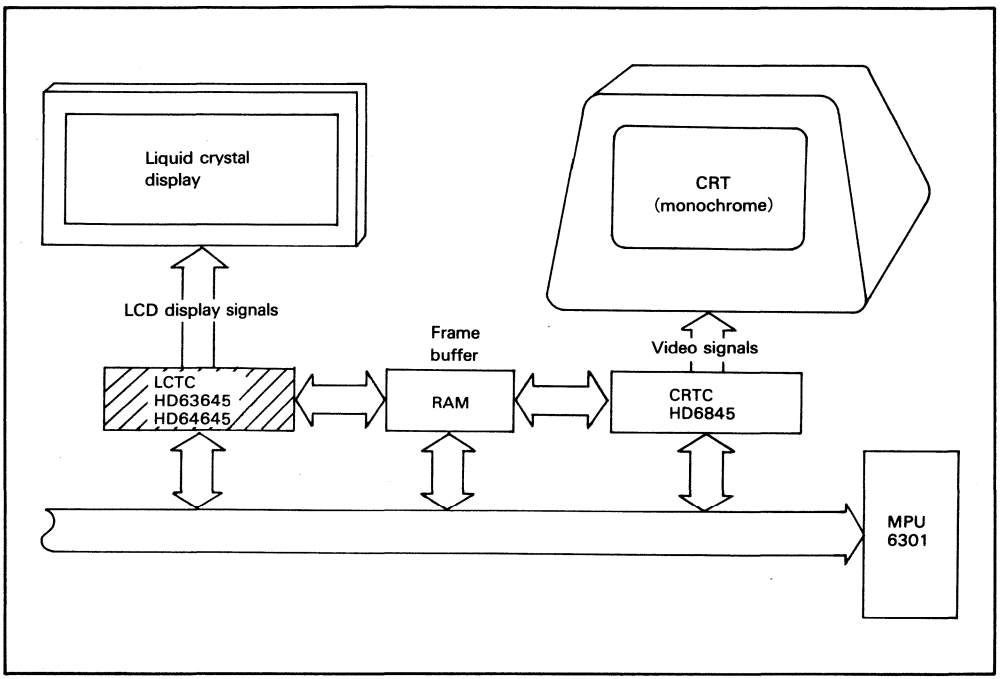


Figure 1. LCD and CRT Displays

Internal Block Diagram

Figure 2 is a block diagram of the LCTC.

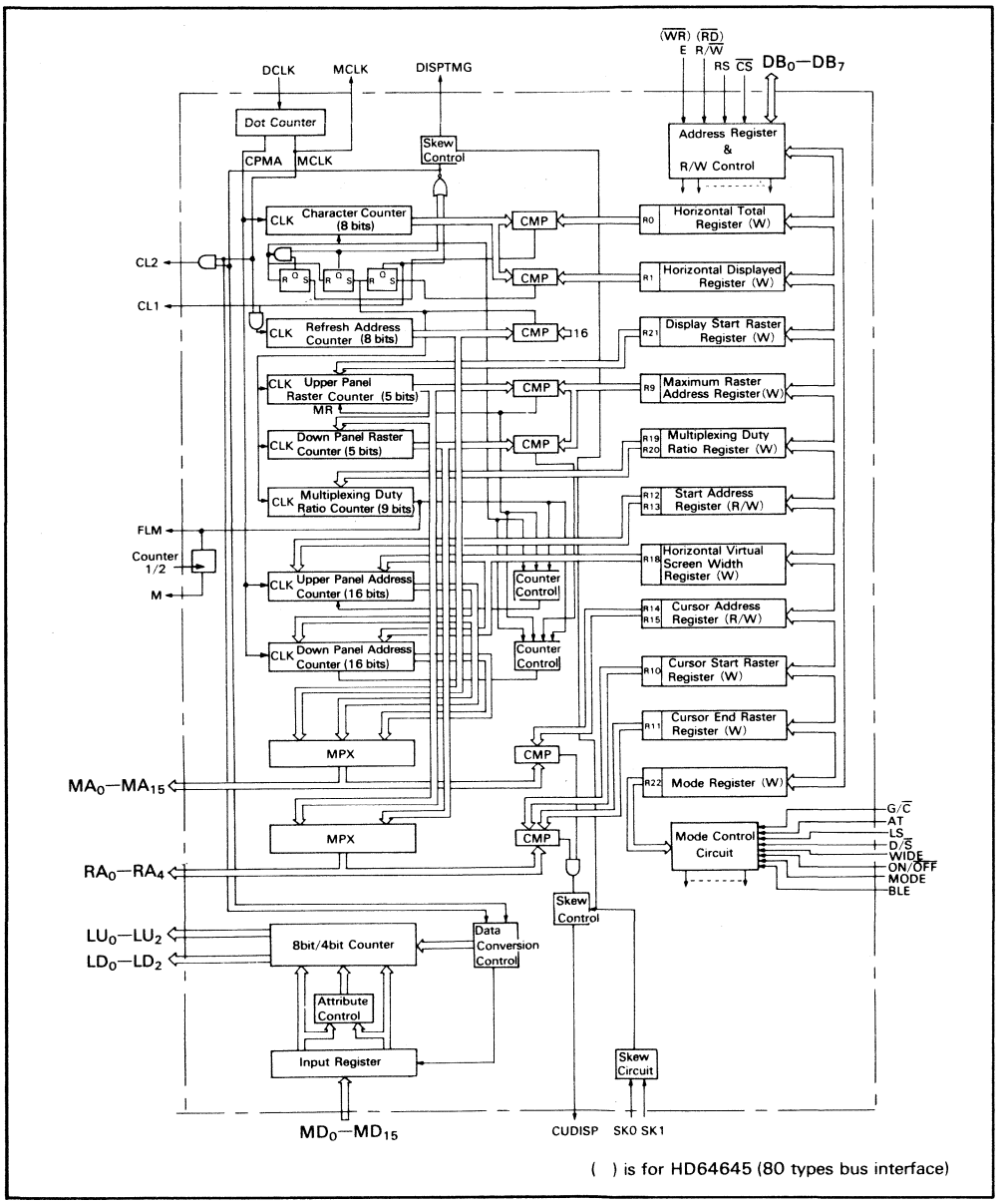


Figure 2. LCTC Block Diagram

System Block Configuration Examples

Figure 3 is a block diagram of a character graphic display system. Figure 5 shows two examples using LCD drivers.

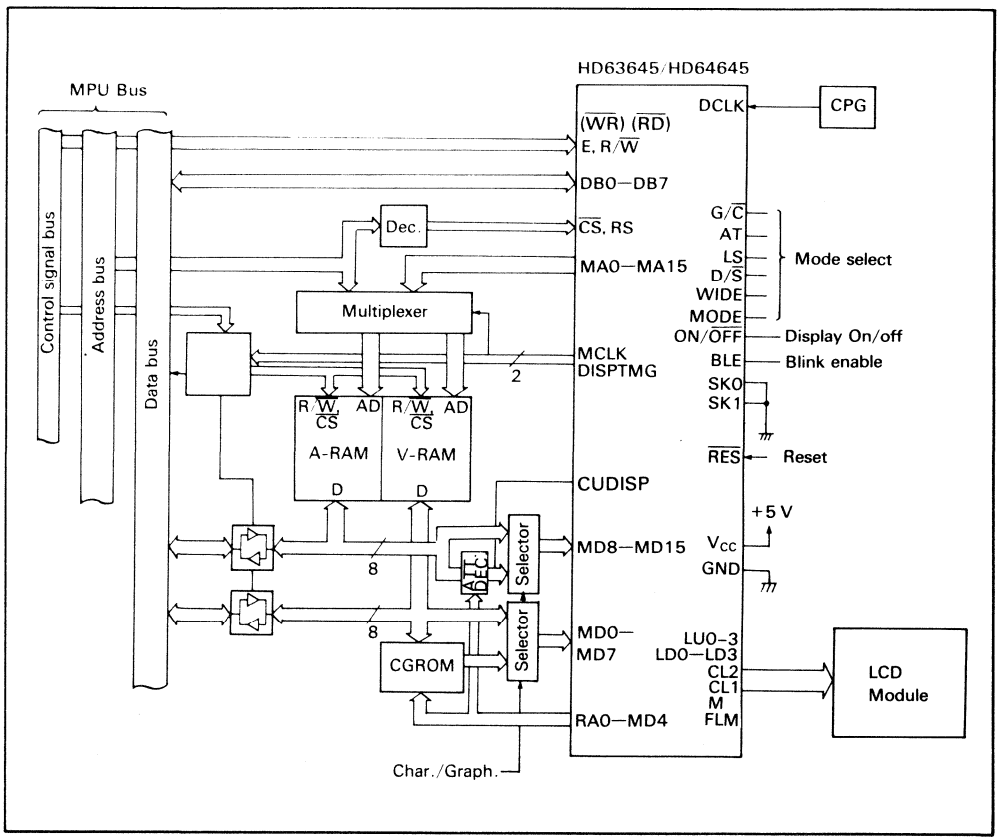
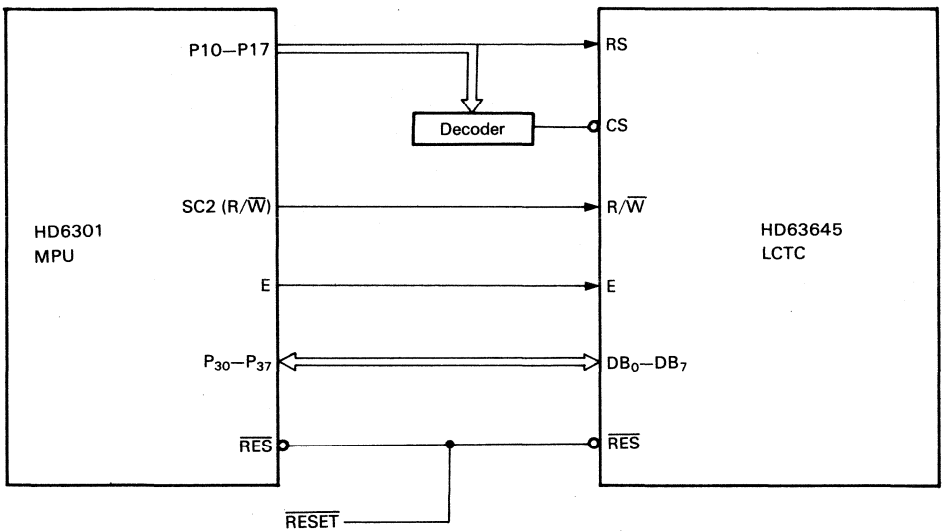


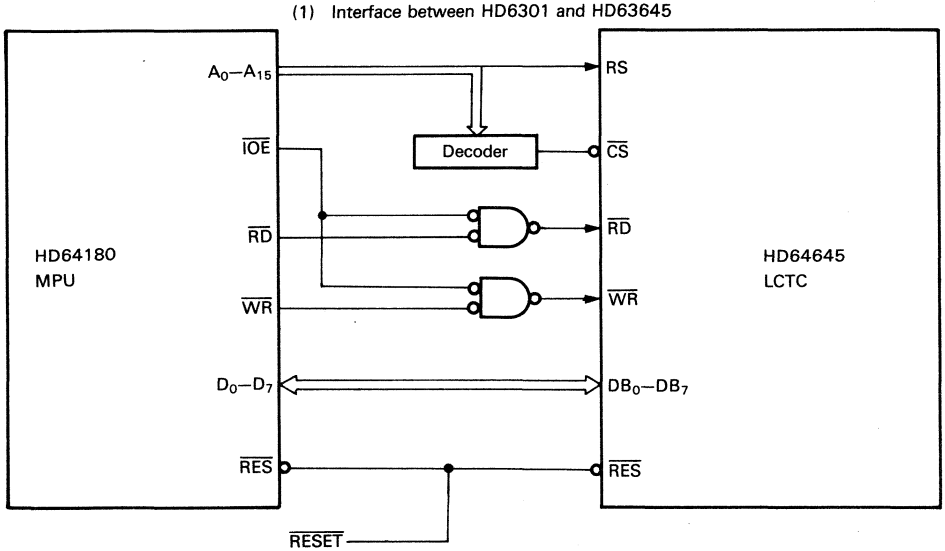
Figure 3. Character/Graphic Display System Example

Interface to MPU



Note: HD6301 is set in mode 5. P10—P17 are used as output ports, and P30—P37 as data buses. SC2 outputs R/$\overline{W}$ here.

(1) Interface between HD6301 and HD63645



Note: Concerning 80 family MPU's, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ANDed signals of the interface signals and $\overline{IOE}$. So $\overline{IOE}$ and $\overline{RD}$, and $\overline{IOE}$ and $\overline{WR}$ should be ORed to satisfy t_{AS}, the timing of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

(2) Interface between HD64180 and HD64645

Figure 4. Interface to MPU

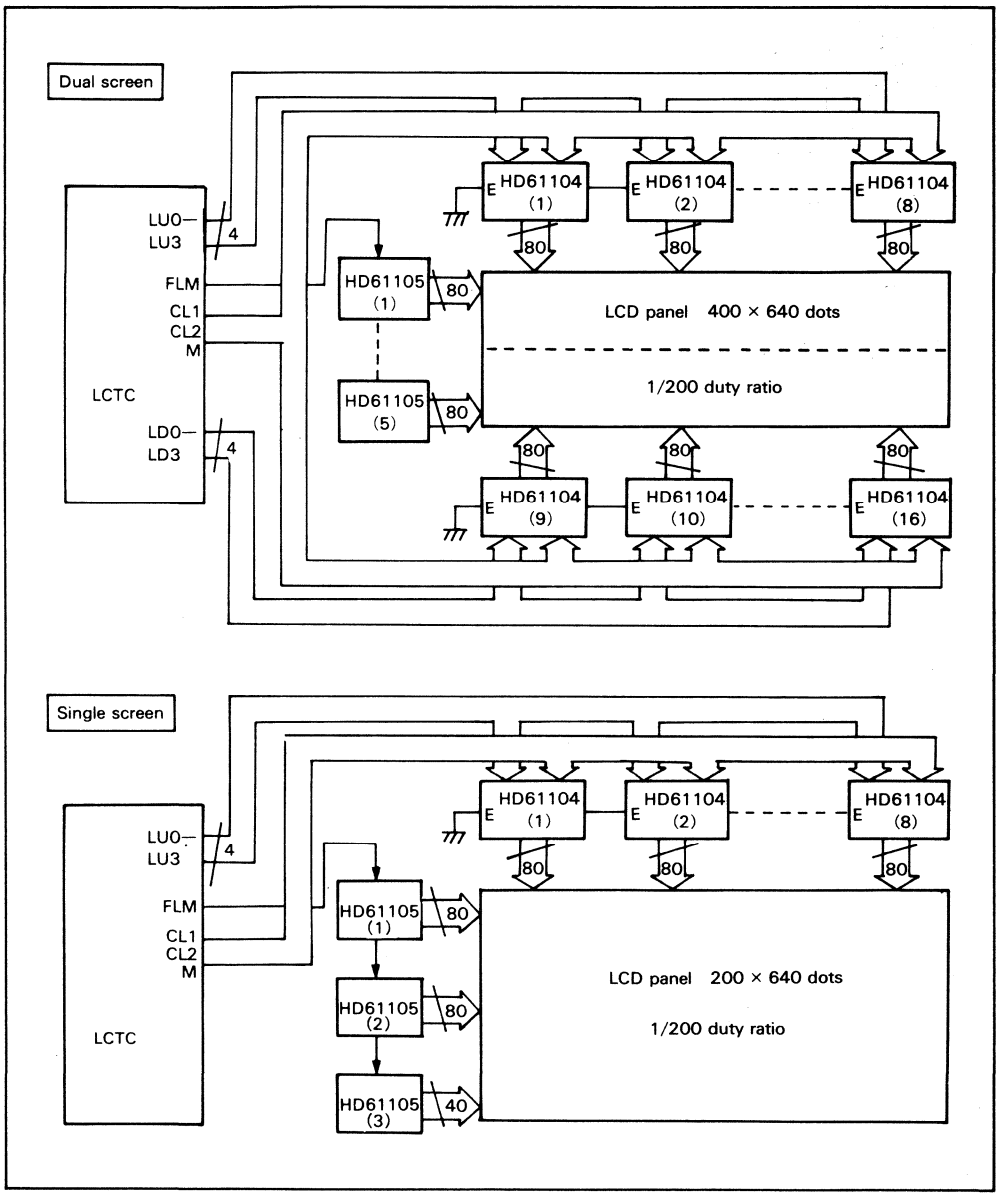


Figure 5. LCD Driver Examples

Registers

Table 5 shows the register mapping. Table 5 describes the in function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4. Registers Mapping

		Address Register	Reg.					Data Bit							
CS	RS	4 3 2 1 0	No.	Register Name	Program Unit	Symbol	R/W	7	6	5	4	3	2	1	0
1	–	------		Invalid	–	–	–								
0	0	------	AR	Address Register	–	–	W								
0	1	0 0 0 0 0	R0	Horizontal Total Characters	Character[3]	Nht	W								
0	1	0 0 0 0 1	R1	Horizontal Displayed Characters	Character	Nhd	W								
0	1	0 1 0 0 1	R9	Maximum Raster Address	Raster	Nr	W								
0	1	0 1 0 1 0	R10	Cursor Start Raster	Raster[4]	Ncs	W		B	P					
0	1	0 1 0 1 1	R11	Cursor End Raster	Raster	Nce	W								
0	1	0 1 1 0 0	R12	Start Address (H)	Memory Address	–	R/W								
0	1	0 1 1 0 1	R13	Start Address (L)	Memory Address	–	R/W								
0	1	0 1 1 1 0	R14	Cursor Address (H)	Memory Address	–	R/W								
0	1	0 1 1 1 1	R15	Cursor Address (L)	Memory Address	–	R/W								
0	1	1 0 0 1 0	R18	Horizontal Virtual Screen Width	Character	Nir	W								
0	1	1 0 0 1 1	R19	Multiplexing Duty Ratio (H)	Raster[3]	Ndh	W								
0	1	1 0 1 0 0	R20	Multiplexing Duty Ratio (L)	Raster[3]	Ndl	W								
0	1	1 0 1 0 1	R21	Display Start Raster	Raster	Nsr	W								
0	1	1 0 1 1 0	R22	Mode Register	–Note[5]	–	W				ON/ OFF	G/C	WIDE	BLE	AT

Notes : 1. ▓▓▓ : Invalid data bits

2. R/W indicates whether write access or read access is enabled to/from each register.
   W : Only write accessible
   R/W : Both read and write accessible
3. The "value to be specified less 1" should be programmed in these registers (R0, R1) and R20).
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below. (For more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on ; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming to these registers, will be ignored.

Table 5. Internal Register Description

Reg. No.	Register Name	Size (Bits)	Description
AR	Address Register	5	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed
R0	Horizontal Total Characters	8	Specifies the horizontal scanning period
R1	Horizontal Displayed Characters	8	Specifies the number of displayed characters per character row
R9	Maximum Raster Address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor Start Raster	5+2	Specifies the cursor start raster address and its blink mode
R11	Cursor End Raster	5	Specifies the cursor end raster address
R12	Start Address (H)	16	Specify the display start address
R13	Start Address (L)		
R14	Cursor Address (H)	16	Specify the cursor display address
R15	Cursor Address (L)		
R18	Horizontal Virtual Screen Width	8	Specifies the length of one row in memory space for horizontal scrolling
R19	Multiplexing Duty Ratio (H)	9	Specify the number of rasters for one screen
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode Register	5	Controls the display mode

*For more details of registers, refer to "Internal Registers".

Table 6. Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD63645/HD64645	Comparison	CRTC HD6845
AR	Address Register	Equivalent to CRTC	Address Register
R0	Horizontal Total Characters		Horizontal Total Characters
R1	Horizontal Displayed Characters		Horizontal Displayed Characters
R2		Particular to CRTC ;	Horizontal Sync Position
R3		unnecessary for LCTC	Sync Width
R4			Vertical Total Characters
R5			Vertical Total Adjust
R6	—		Vertical Displayed Characters
R7			Vertical Sync Position
R8			Interlace and Skew
R9	Maximum Raster Address	Equivalent to CRTC	Maximum Raster Address
R10	Cursor Start Raster		Cursor Start Raster
R11	Cursor End Raster		Cursor End Raster
R12	Start Address (H)		Start Address (H)
R13	Start Address (L)		Start Address (L)
R14	Cursor Address (H)		Cursor (H)
R15	Cursor Address (L)		Cursor (L)
R16		Particular to CRTC ;	Light Pen (H)
R17		unnecessary for LCTC	Light Pen (L)
R18	Horizontal Virtual Screen Width	Additional registers for LCTC	
R19	Multiplexing Duty Ratio (H)		
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster		
R22	Mode Register		

Functional Description

Programmable Screen Format

Figure 6 illustrates the relation between LCD display screen and registers. Figure 7 shows a timing chart of signals output from the LCTC in mode 5 as an example.

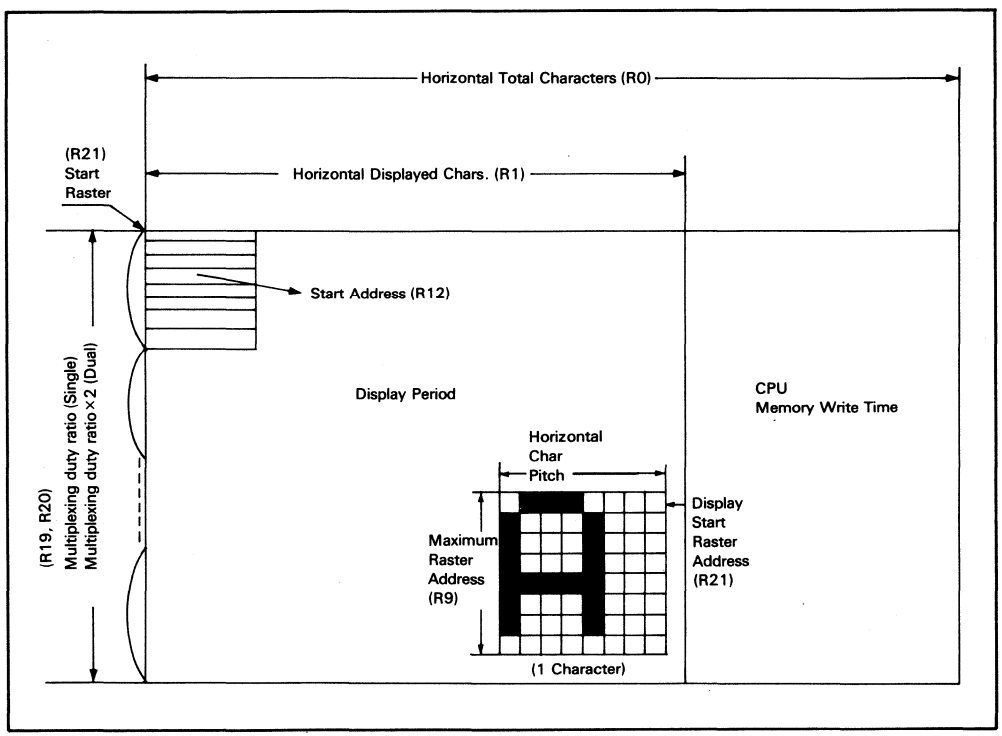


Figure 6. Relation between Display Screen and Registers

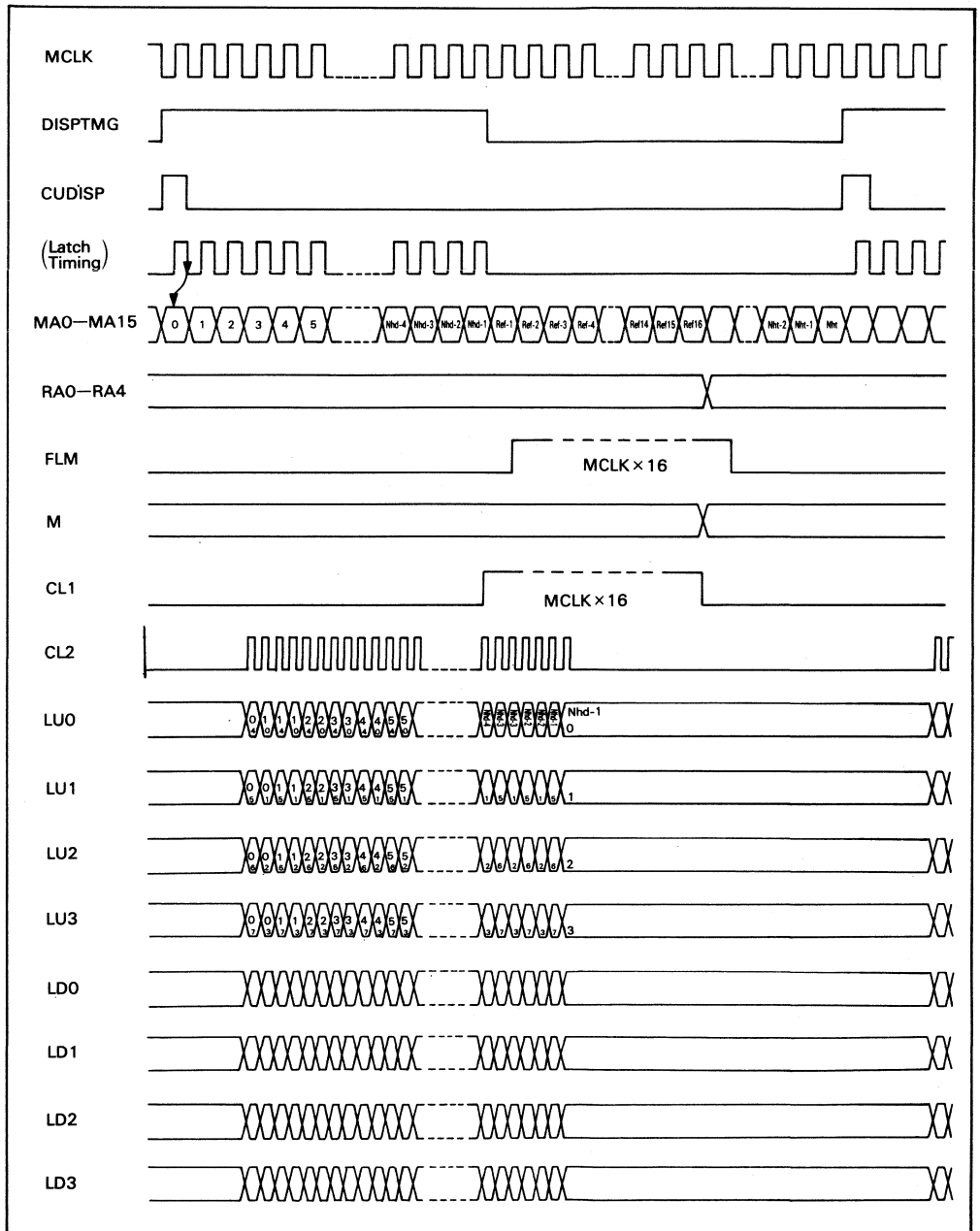


Figure 7. LCTC Timing Chart (In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (figure 8) can be controlled by programming specific registers.

- Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

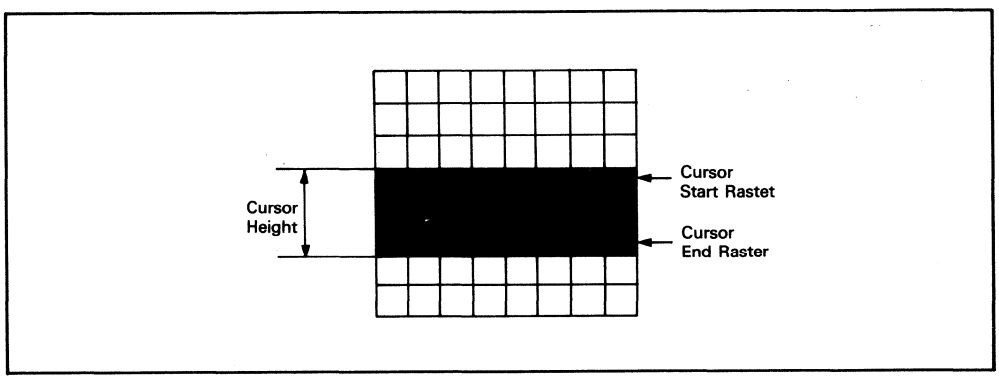


Figure 8. Cursor Display

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode : Character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black), etc., by storing the attribute data in attribute RAM (A-RAM).

Figure 9 illustrates the relation between character display screen and memory contents.

Graphic Mode 1 : Graphic Mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 10 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2 : Graphic mode 2 utilizes software for the system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly a number of times specified by maximum raster register (R9). The raster address is output in the same way as character mode.

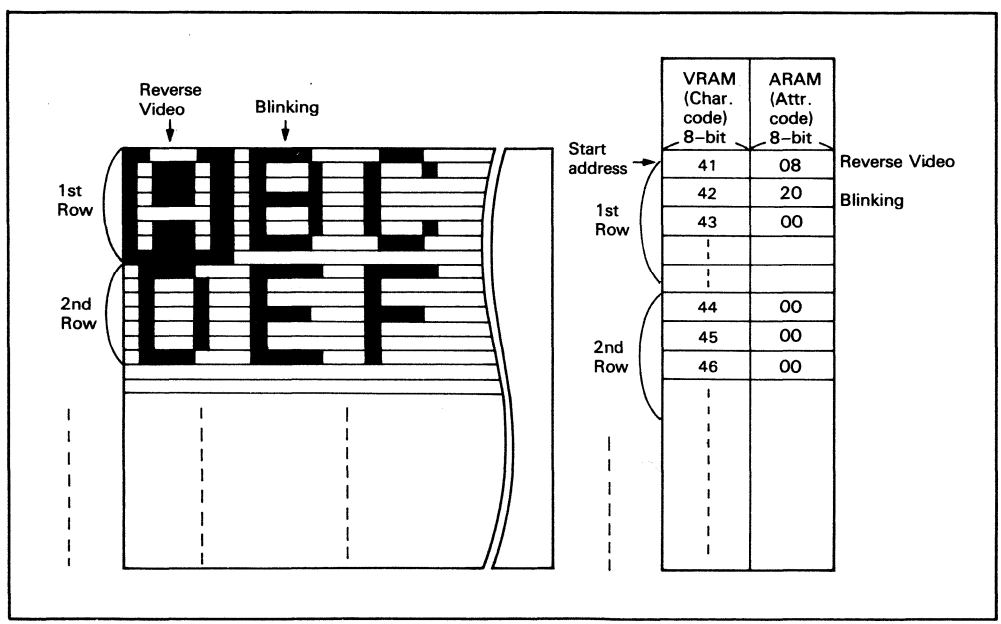


Figure 9. Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (figure 11).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 12 shows an example.

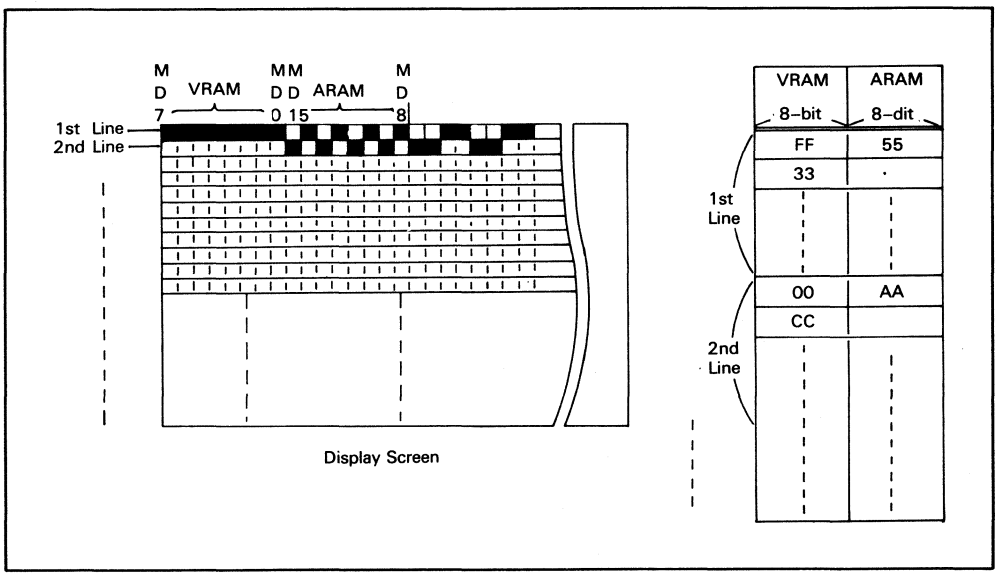


Figure 10. Relation between Graphic Screen and Memory Contents

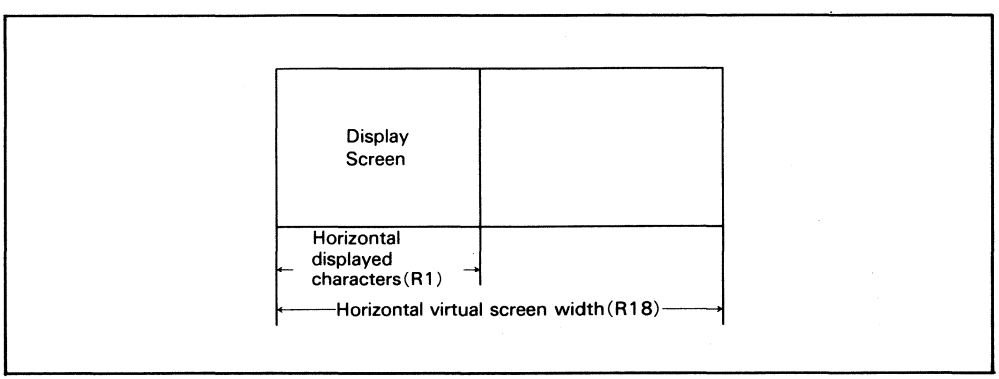


Figure 11. Horizontal Virtual Screen Width

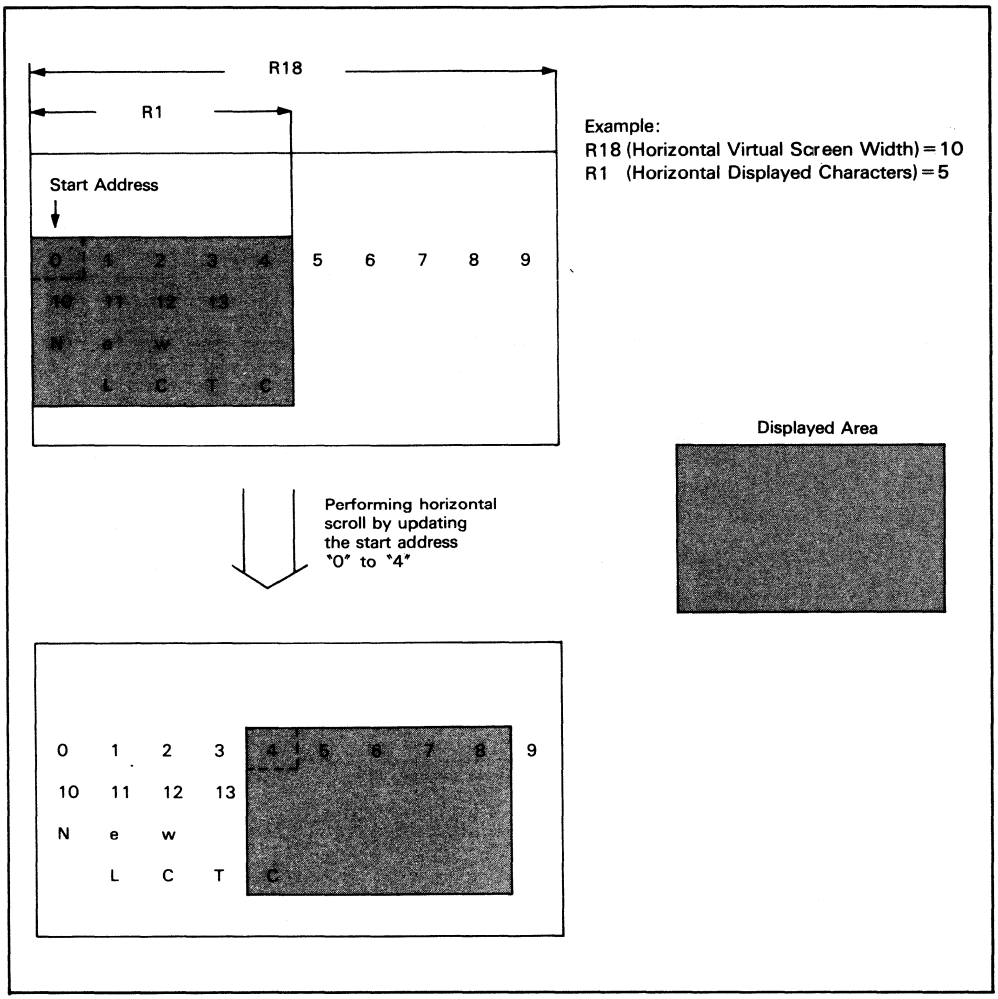


Figure 12. Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (figure 13) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (figure 14). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

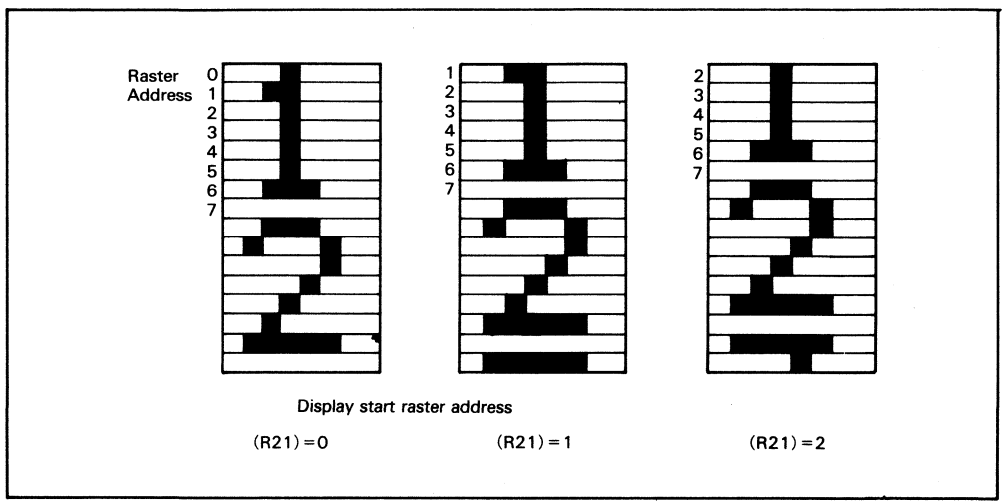


Figure 13. Example of Smooth Scroll by Setting Display Start Raster Address

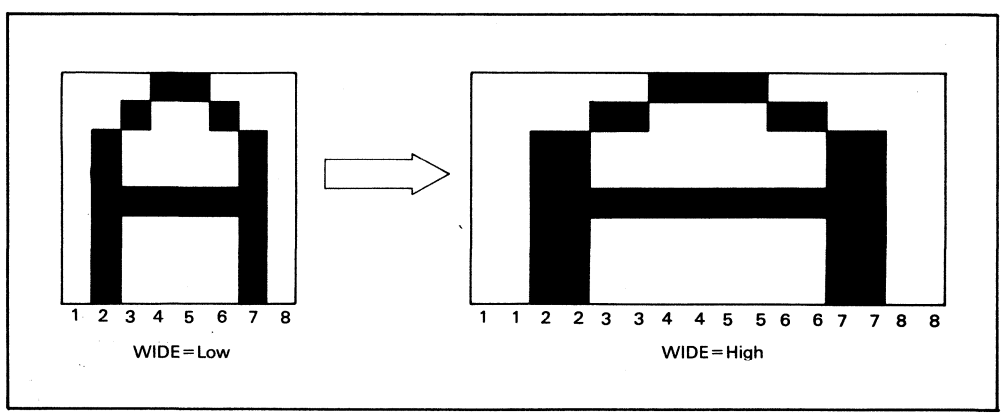


Figure 14. Example of Wide Display

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 15 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (R22) or the AT pin. As shown in figure 15, a character attribute can be specified by placing the character code on MD0-MD7, and the attribute code on MD11-MD15. MD8-MD10 are invalid.

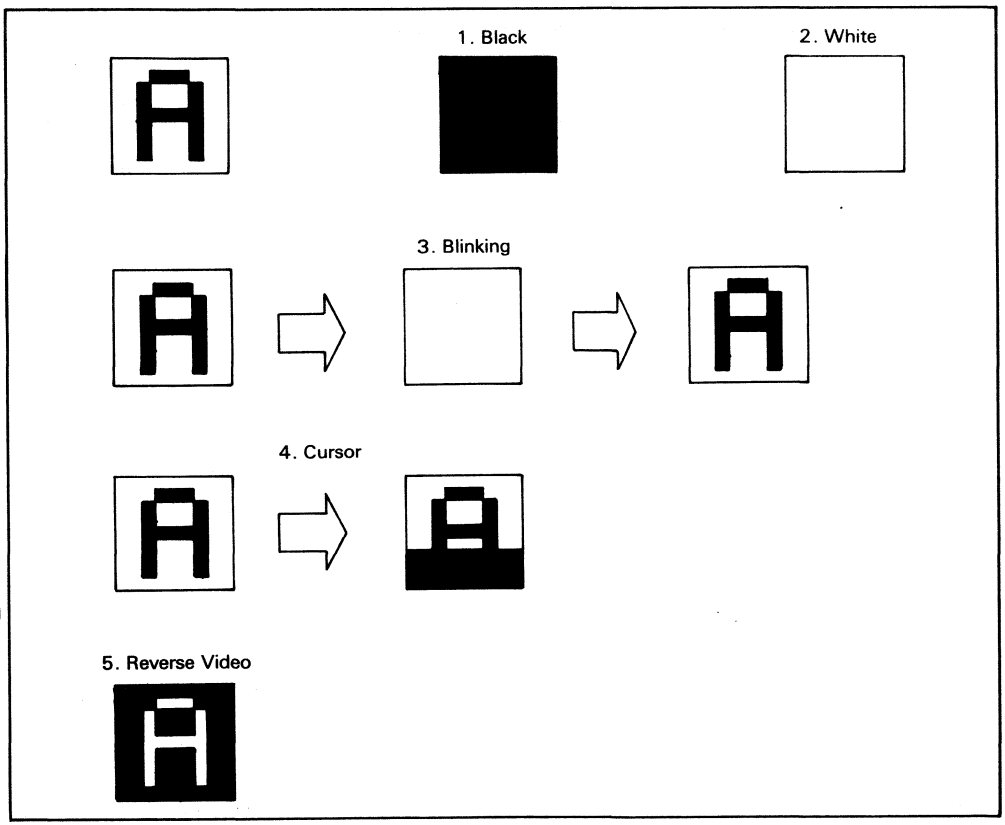


Figure 15. Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10-8	7-0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	* * *	Character Code

*: Invalid

Figure 16. Attribute Code

OR Function —Superimposing Characters and Graphics

The OR function (figure 17) generates the OR of the data entered into MD0-MD7 (e.g. character data) and the data into MD8-MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

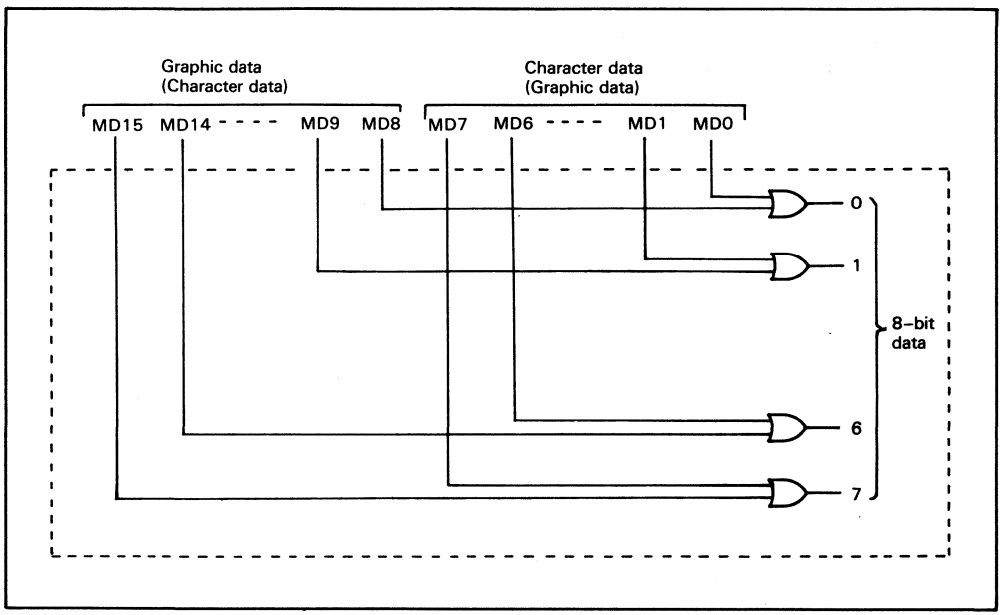


Figure 17. OR Function

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in figure 18. The 16 refresh addresses per scanned line are output 16 times, from $00-$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in table 7.

Table 7. Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

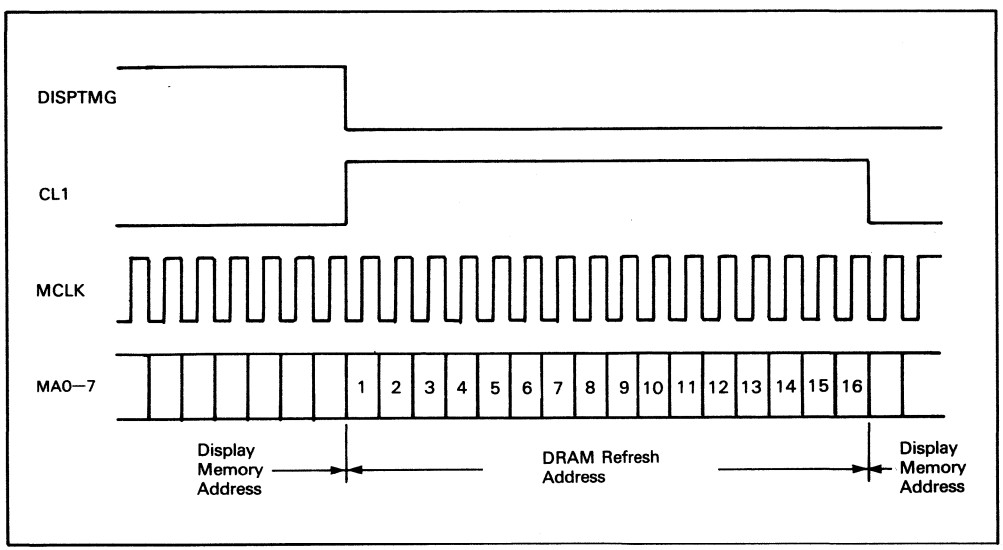


Figure 18. DRAM Refresh Address Output

Easy Mode

This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Paster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of display spreading over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See figure 19.)

Table 8. Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

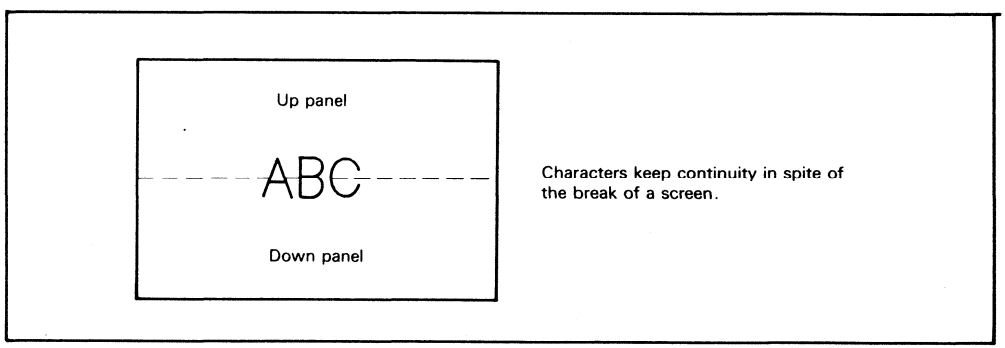


Figure 19. Example of the Display in the Character Mode

System Configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (figure 20).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column driversis smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations:

- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format:

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screeen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.

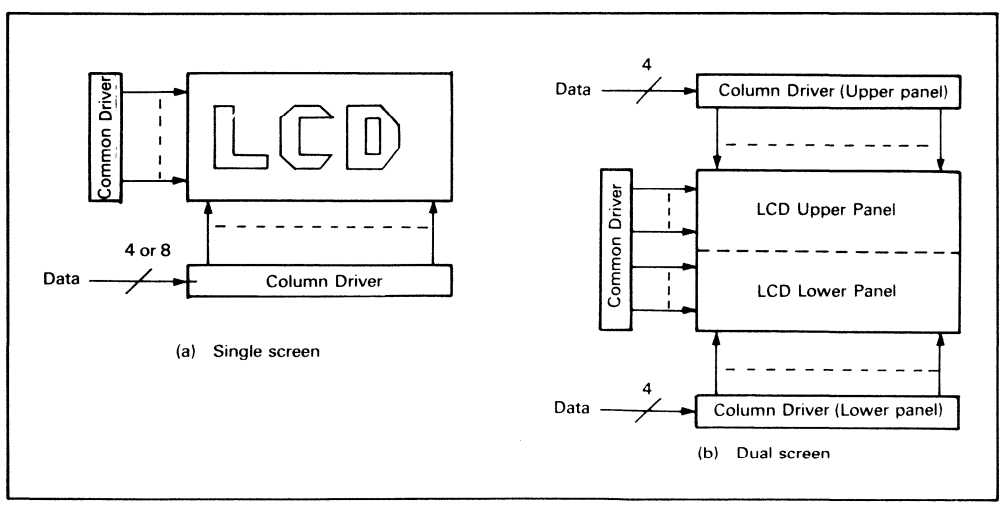


Figure 20. Hardware Configuration According to Screen Format

Table 9. Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configuration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum data transfer speed (MBPS)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	5
				Wide	$\frac{AT}{OR}$	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	$\frac{AT}{OR}$	20	1
				Wide	$\frac{AT}{OR}$	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	9
				Wide	$\frac{AT}{OR}$	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note : Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

Mode List

Table 10. Mode List

No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Config.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic			
4	Dual-screen graphic 2	1	1	0	0	0				—	—
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic			
8	Single-screen graphic 2	0	1	0	0	0				—	—
9	8-bit character	0	0	1	0	0		Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic			
12	8-bit graphic 2	0	1	1	0	0				—	—
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note : The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are inhibited, because they may cause malfunctions. If you set an inhibited combination, set the right combination again.

Internal Registers

The HD63645/HD64645 has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2-R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (figure 21) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (figure 22) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. The "Nht" indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its unit is, then, converted from time into the number of characters. This value is to be specified according to the specification of the LCD system to be used.

Horizontal Displayed Characters Register (R1)

R1 register (figure 23) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

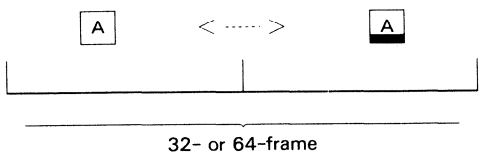
The "Nhd" must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (figure 24) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Cursor Start Raster Register (R10)

R10 register (figure 25) specifies the cursor start raster address and its blink mode. Refer to table 11.



Cursor End Raster Register (R11)

R11 register (figure 26) specifies the cursor end raster address.

Start Address Register (H/L)(R12/R13)

R12/R13 register (figure 27) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	
—	—	—	Register address						W

Figure 21. Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nhd (Displayed characters)								Character	W

Figure 23. Horizontal Displayed Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nht (Total characters − 1)								Character	W

Figure 22. Horizontal Total Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nr					Raster	W

Figure 24. Maximum Raster Address Register

the MPU.

Cursor Address Register (H/L)(R14/R15)
R14/R15 register (figure 28) specifies a cursor display address. Cusor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Horizontal Virtual Screen Width Register (R18)
R18 register (figure 29) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Multiplexing Duty Ratio Register (H/L) (R19/R20)
R19/R20 register (figure 30) specifies the number of vertical dots of the display screen.

The programmed value differs according to the LCD screen configuration.

In single screen configuration :
(Programmed value) = (Number of vertical dots) − 1.

In dual screen configuration :
$$\text{(Programmed value)} = \frac{\text{(Number of vertical dots)}}{2} - 1.$$

Display Start Raster Register (R21)
R21 register (figure 31) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode register (R22)
The OR of the data bits of R22 (figure 32) register and the external terminals of the same name determines a particular mode. (figure 33)

Table 11 Cursor Blink Mode

B	P	Cursor blink mode
0	0	Cursor on ; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	B	P	Ncs (Raster address)					Raster	W

Figure 25. Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (Raster address)					Raster	W

Figure 26. Cursor End Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R12)								Memory	R/W
Memory address (L) (R13)								address	

Figure 27. Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R14)								Memory	R/W
Memory address (L) (R15)								address	

Figure 28. Cursor Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 29. Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Raster address					Raster	W

Figure 31. Display Start Raster Register

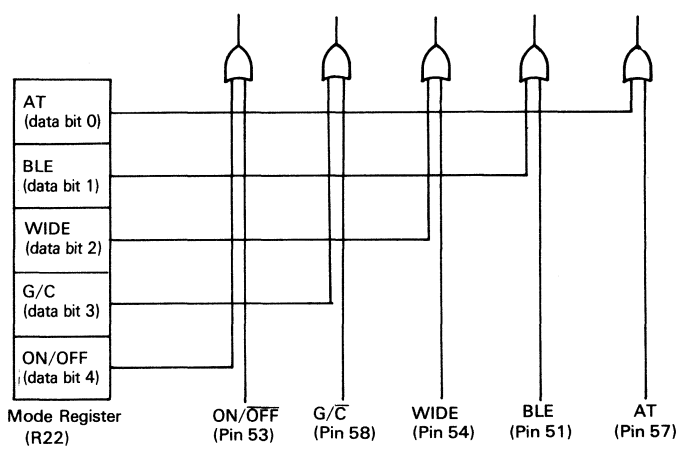
Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters − 1) (R20)									

* : Number of rasters

Figure 30. Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	ON/OFF	G/C	WIDE	BLE	AT	—	W

Figure 32. Mode Register



Notes: 1. AT (valid only when G/C is low (character mode))
AT = High: Attribute functions enabled, OR function disabled.
AT = Low: OR function enabled, attribute functions disabled.

2. BLE (valid only when G/C is low (character mode))
BLE = High: Blinking enable on the character specified by attribute RAM
BLE = Low: No blinking

3. WIDE (valid only when G/C is low (character mode))
WIDE = High: Wide display enabled
WIDE = Low: Normal display

4. G/C
G/C = High: Graphic 1 display (when AT = Low) or Graphic 2 display (when AT = High)
G/C = Low: Character display

5. ON/OFF
ON/OFF = High: Display on state
ON/OFF = Low: Display off state

Figure 33. Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers is restricted as shown in Table 12.

Table 12. Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display Format	$1 < Nhd < Nht + 1 \leqq 256$	R0, R1
	$Nhd + \frac{16}{m} * 1 \leqq Nht + 1$	
	(No. of vertical dots) x (no. of horizontal dots) x (frame frequency; f_{FRM}) ≦ (data transfer speed; V)	R1, R19, R20
	$\left\{\begin{matrix}1\\2\end{matrix}\right\} * 2 \times (Nd + 1) \times Nhd \times \left\{\begin{matrix}8\\16\end{matrix}\right\} * 3\ f_{FRM} \leqq V$	
	$Nhd \leqq Nir$	R1, R18
	$0 \leqq Nd \leqq 511$	R19, R20
Cursor Control	$0 \leqq Ncs \leqq Nce$	R10, R11
	$Nce \leqq Nr$	R10, R9
Smooth Scroll	$Nsr \leqq Nr$	R21, R9
Memory Width Set	$0 \leqq Nir \leqq 255$	R18

*1 m varies according to the modes. See the following table.

Mode No.	m
5,9	1
1,6,7,8,10,11,12,13	2
2,3,4	4

*2 Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5,6,7,8,9,10,11,12	1
1,2,3,4,13	2

*3 Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1,5,9	8
2,3,4,6,7,8,10,11,12,13	16

Reset

$\overline{RES}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

"Reset" is defined as follows (Figure 34) :

- At reset: the time when $\overline{RES}$ goes low
- During reset: the period while $\overline{RES}$ remains low
- After reset: the period on and after the $\overline{RES}$ transition from low to high

$\overline{RES}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{RES}$ pin does not basically control output pins, and operates regardless of other input pins.

(1) Preserves states before reset :
LU0-LU3, LD0-LD3, FLM, CL1, RA0-RA4
(2) Fixed at high level :
MLCK
(3) Preserves states before reset or fixed at low level according to the timing when the reset signal is input :
DISPTMG, CUDISP, MA0-MA15
(4) Fixed at high or low according to mode :
CL2
(5) Unaffected :
DB_0-DB_7

Reset State of Registers

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state ; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD63645/HD64645

(1) The HD63645/HD64645 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.
(2) At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

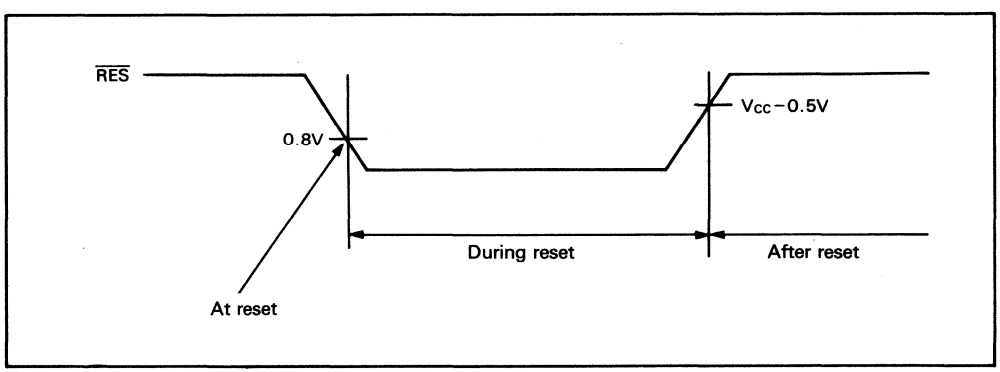


Figure 34. Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. Width respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS Interface				0.8	V	I_{OL} = 400μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface (HD63645 — 68 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500			ns	35
Enable pulse width (high)	P_{WEH}	220			ns	
Enable pulse width (low)	P_{WEL}	220			ns	
Enable rise time	t_{Er}			25	ns	
Enable fall time	t_{Ef}			25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70			ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10			ns	
DB_0-DB_7 setup time	t_{DS}	60			ns	
DB_0-DB_7 hold time	t_{DHW}	10			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

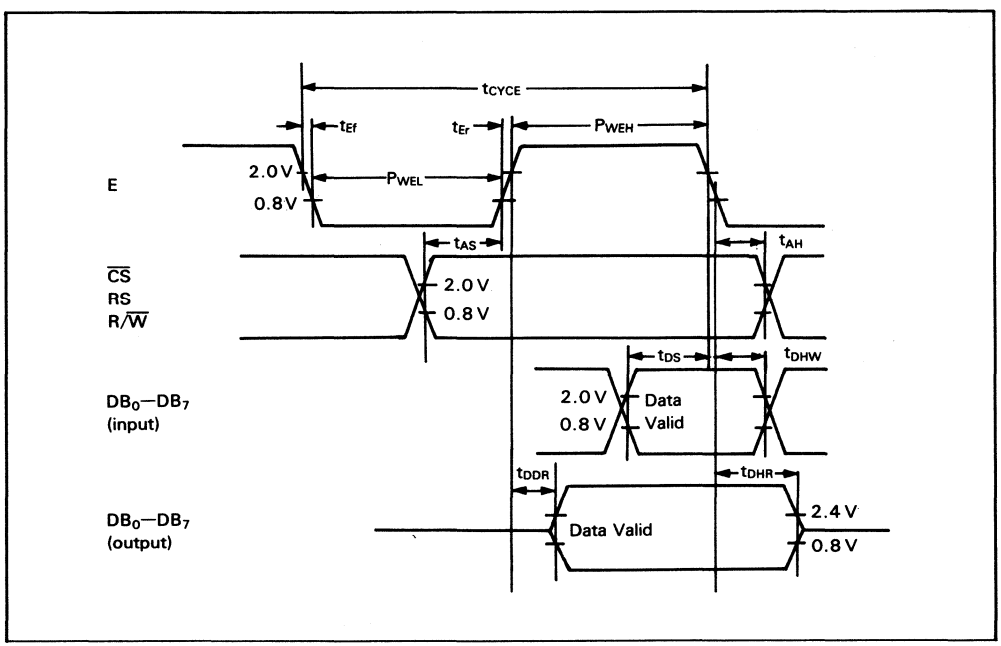


Figure 35. CPU Interface (HD63645)

CPU Interface (HD64645 — 80 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	36
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

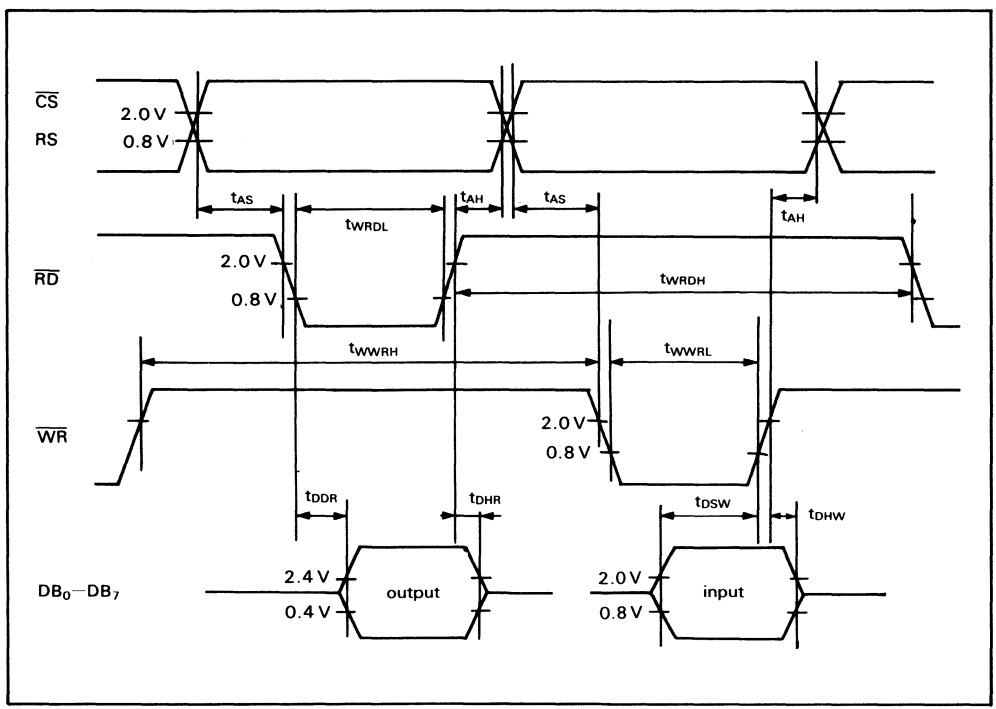


Figure 36. CPU Interface (HD64645)

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	37
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			70	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

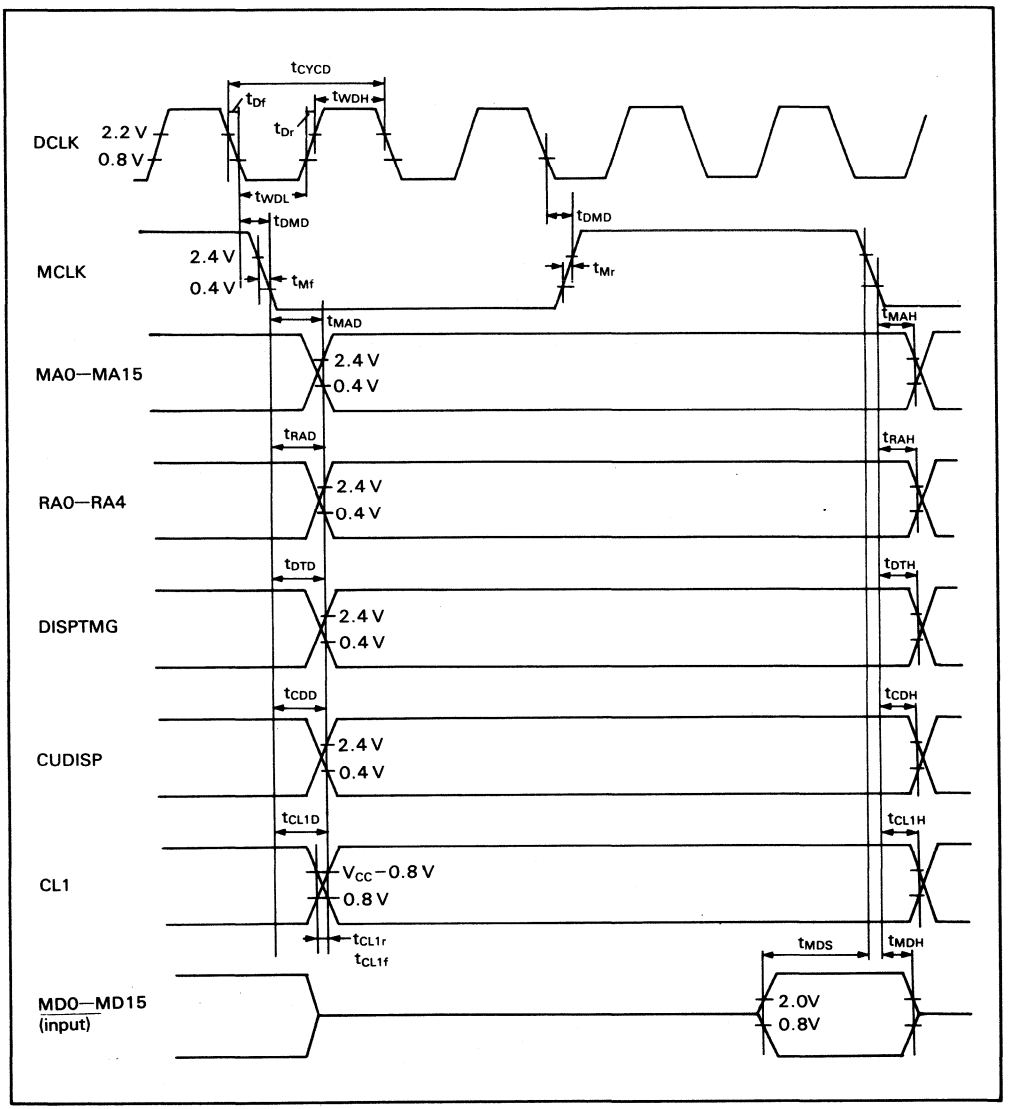


Figure 37. Memory Interface

AC Characteristics (Cont)

LCD Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50			ns	38
Display data hold time	t_{LDH}	100			ns	
CL2 high level width	t_{WCL2H}	100			ns	
CL2 low level width	t_{WCL2L}	100			ns	
FLM setup time	t_{FS}	500			ns	
FLM hold time	t_{FH}	300			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
CL2 rise time	t_{CL2r}			50	ns	
CL2 fall time	t_{CL2f}			50	ns	

Note : At fCL2 = 3 MHz

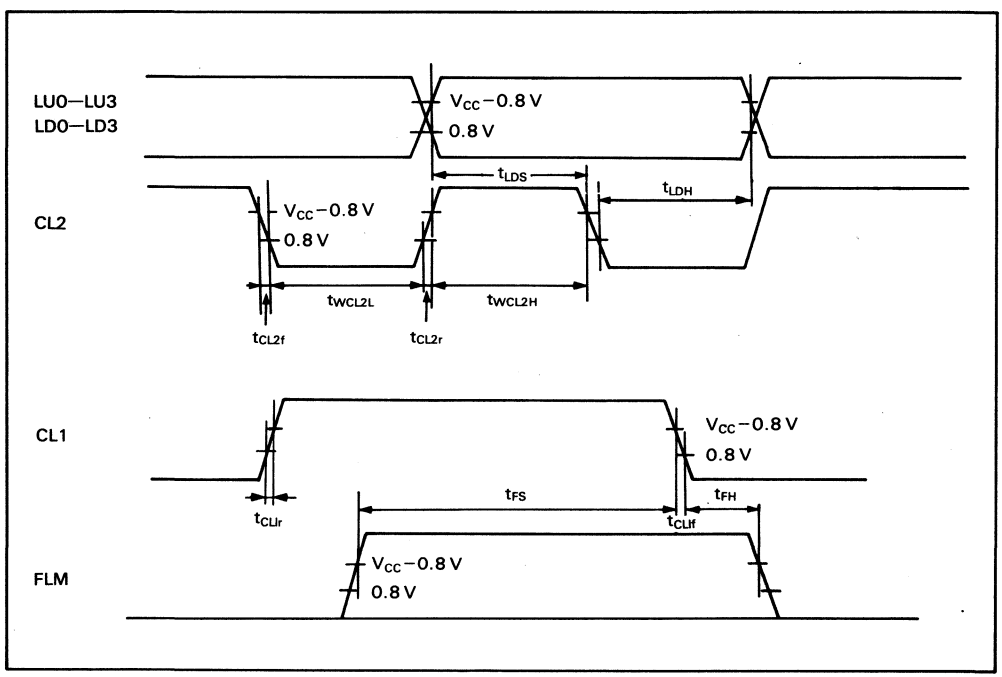
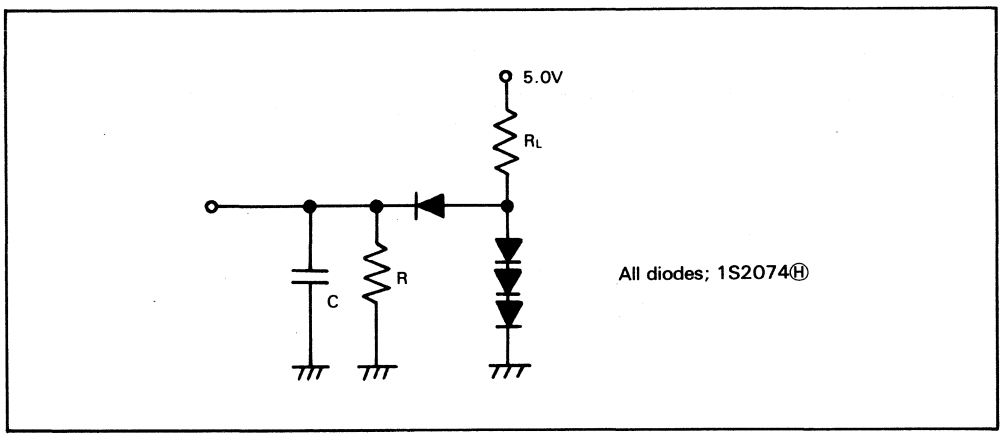


Figure 38. LCD Interface

AC Characteristics

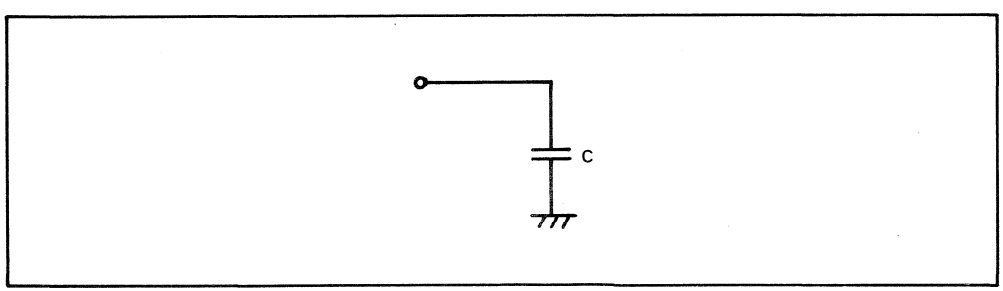
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



Capacity Load

Terminal	C	Remarks
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF	



HD64646

LCD Timing Controller (LCTC)

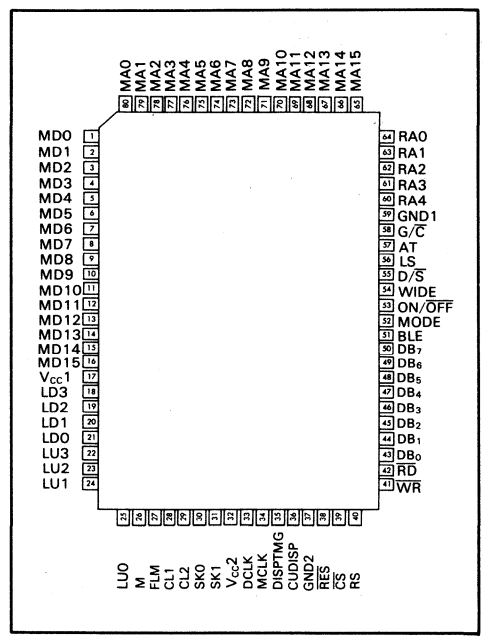
Description

The HD64646 LCTC is a modified version of the HD64645 LCTC with differente LCD interface timing.
The HD64646 is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/sec in character mode
  —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106 (column/common)
- CPU interface:
  80 family
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80A)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	FP-80
HD64645	4 MHz	80 System	FP-80
HD64646	4 MHz	80 System	FP-80B

Differences Between HD64645 and HD64646

Fig.1 and Fig.2 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Fig.1 shows the case without skew function and fig.2 shows the case with skew function.
In Fig.1 "High" period between CL2 and CL1 of HD64645 overlap.
HD64646 has no overlap like HD64645, and except for overlap parts HD64646 is the same as HD64645 functionally.
Besides, in case of skew function, phase relation between CL1 and CL2 changes. As Fig.2 shows, data transfer period and CL1 "High" period of HD64646 never overlap in case of skew function.

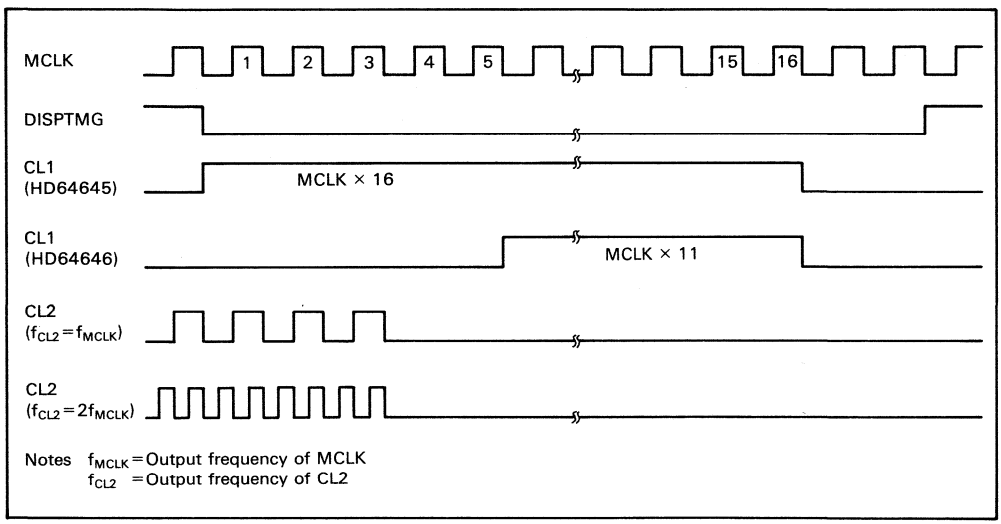


Figure 1. Differences between HD64645 and HD64646 (no skew)

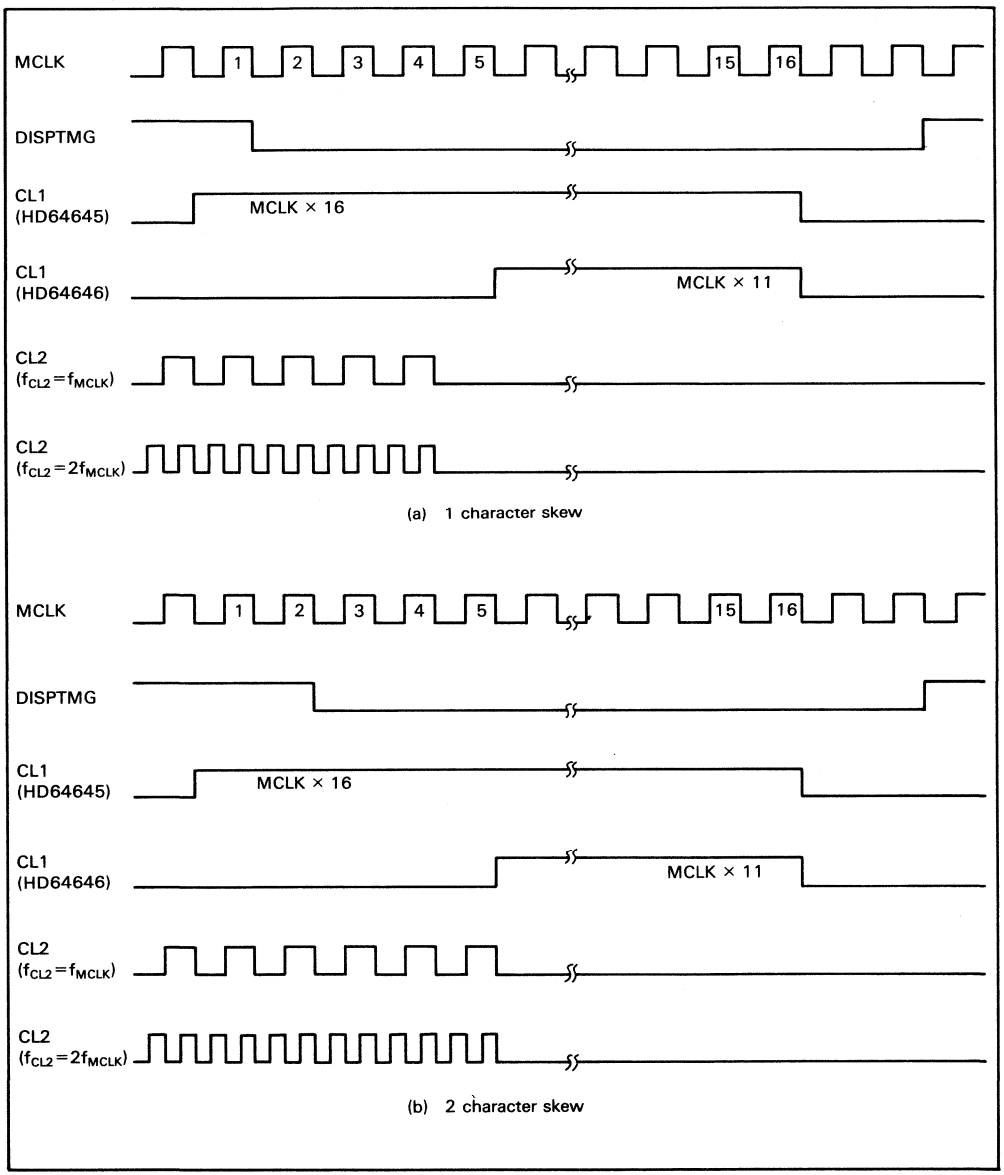


Figure 2. Differences between HD64645 and HD64646 (skew)

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. With respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS Interface				0.8	V	I_{OL} = 400μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes : 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	3
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

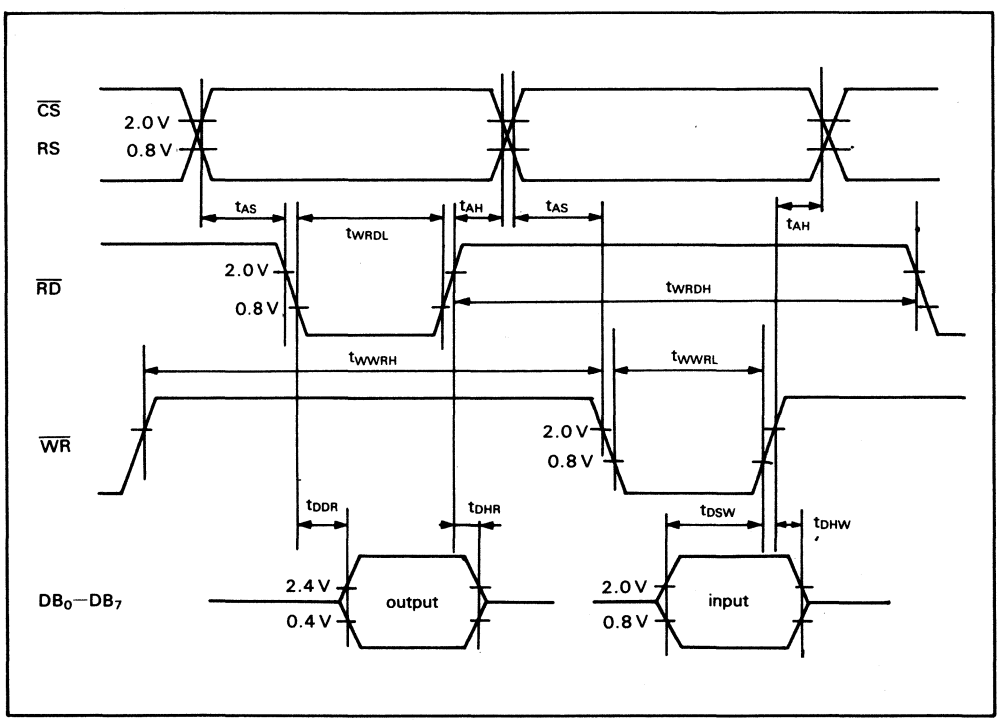


Figure 3. CPU Interface

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	4
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			60	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

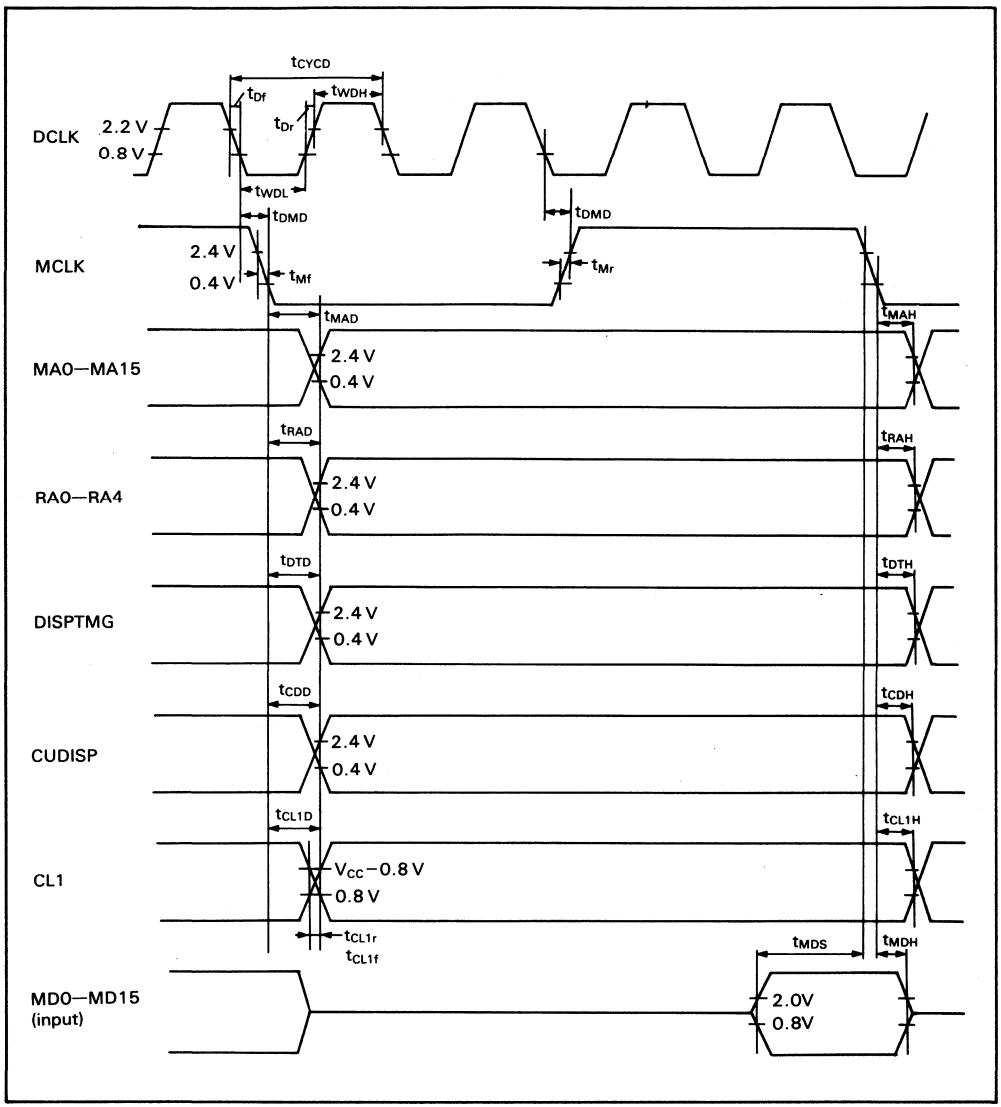


Figure 4. Memory Interface

AC Characteristics (Cont)

LCD Interface 1 (at f_{CL2}=3MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM stetup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	300	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	100	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	100	–	–	ns	
CL2 low level width	t_{CL2L}	100	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	80	–	–	ns	
Display data hold time	t_{LDH}	100	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

LCD Interface 2 (at f_{CL2}=5MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	200	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	70	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	50	–	–	ns	
CL2 low level width	t_{CL2L}	50	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	30	–	–	ns	
Display data hold time	t_{LDH}	30	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

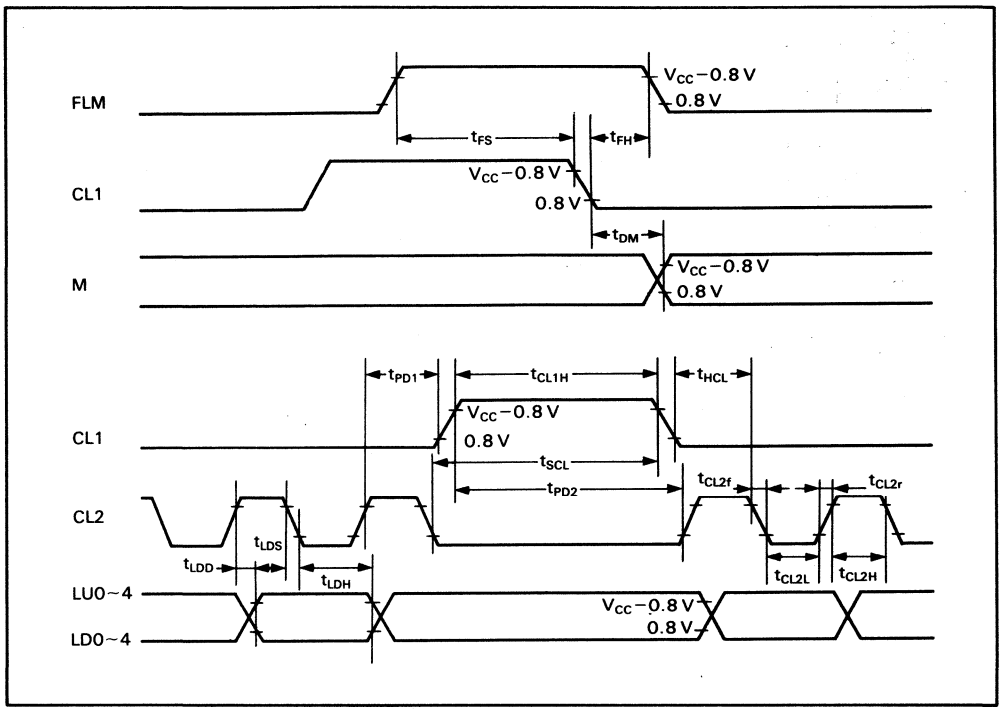
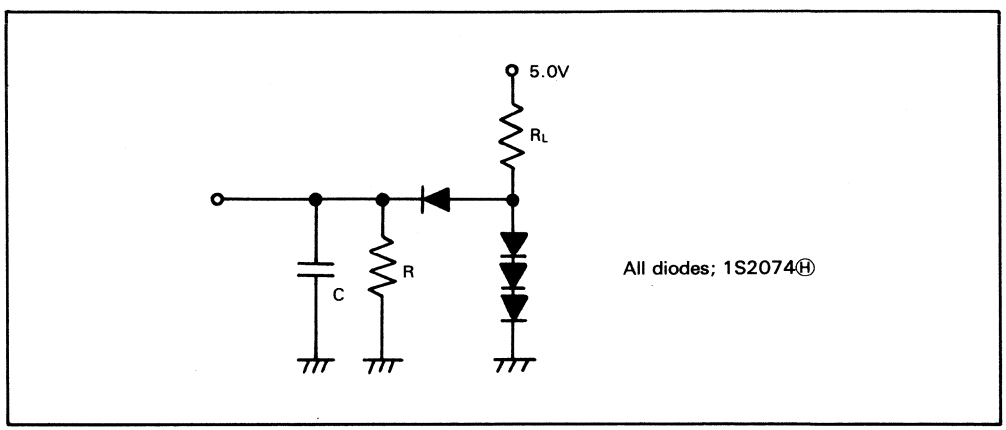


Figure 5. LCD Interface

AC Characteristics

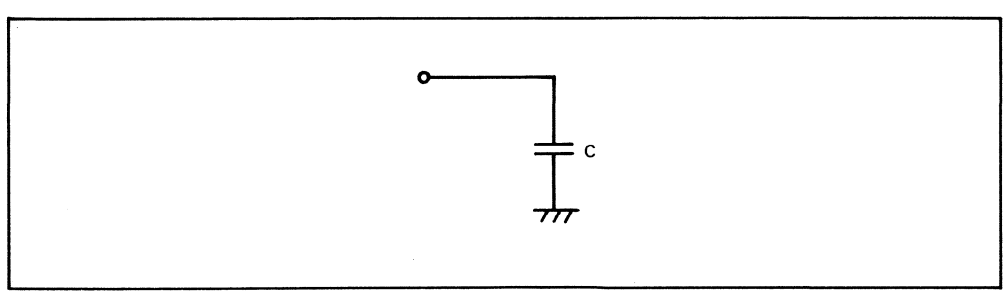
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



Capacity Load

Terminal	C	Remarks
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF	



HD66840

LCD Video Interface Controller (LVIC)

Description

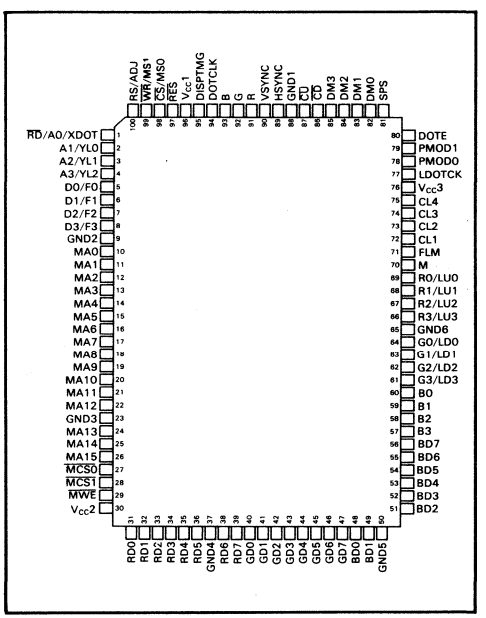
The HD66840 LVIC interface controller converts the standard video signals R, G, B for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes. It also enables the software originally intended for CRT display to control the LCD.

Since the LVIC can control TFT-type LCDs in addition to the current TN-type LCD, it can support color display as well as monochrome display. It can program screen size and can control a large-panel LCD of 720 dots × 512 dots (max).

Features

- Converts video R, G, B signals for CRT display into LCD data:
  - —Monochrome display data
  - —8-level gray scale display data
  - —8-color display data
- Can select LVIC control method:
  - —Pin programming method
  - —Internal register programming method (either with MPU or ROM)
- Can program screen size:
  - —200, 350, 400, 480, 512, or 540 dots (lines) in height and 640, or 720 dots (80, or 90 characters) in width by pin programming method
  - —4-1024 dots (lines) in height and 32-4048 dots (4-506 characters) in width by internal register programming method
- Can regenerate the display timing signal from HSYNC and VSYNC
- Internal PLL circuit can generate the dot clock (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Can control both TN-type LCD and TFT-type LCD
- Maximum operating frequency: 25, 30 MHz (dot clock for CRT display)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, B) parallel data transfer
- Recommended LCD drivers: HD61104, HD61105, and HD66106
- CMOS 1.3 μm process
- Single power supply: +5 V ± 10 %
- 100-pin plastic QFP (FP-100A)

Pin Arrangement



Pin Description

Table 1 describes the pins.

Table 1. Pin Description

Symbol	Pin Number	Pin Name	I/O
$V_{CC}1$-$V_{CC}3$	96, 30, 76	$V_{CC}1$, V_{CC} 2, V_{CC} 3	—
GND1-GND6	88, 9, 23, 37, 50, 65	Ground 1-6	—
R, G, B[1]	91, 92, 93	Red, green, blue serial data	I
HSYNC	89	Horizontal synchronization	I
VSYNC	90	Vertical synchronization	I
DISPTMG[2]	95	Display timing	I
DOTCLK	94	Dot clock	I
R0-R3[3]	69-66	LCD red data 0-3	O
LU0-LU3[4]	69-66	LCD up panel data 0-3	O
G0-G3[3,5]	64-61	LCD green data 0-3	O
LD0-LD3[4,5]	64-61	LCD down panel data 0-3	O
B0-B3[3,6]	60-57	LCD blue data 0-3	O
CL1	72	LCD data line clock	O
CL2	73	LCD data shift clock	O
CL3[7]	74	Y-driver shift clock 1	O
CL4[7]	75	Y-driver shift clock 2	O
FLM	71	First line marker	O
M	70	LCD driving signal alternation	O
LDOTCK	77	LCD dot clock	I
$\overline{MCS0}$, $\overline{MCS1}$[8]	27, 28	Memory chip select 0, 1	O
$\overline{MWE}$[9]	29	Memory write enable	O
MA0-MA15[9]	10-22, 24-26	Memory address 0-15	O
RD0-RD7[9]	31-36, 38-39	Memory red data 0-7	I/O
GD0-GD7[9,10]	40-47	Memory green data 0-7	I/O
BD0-BD7[9,10]	48, 49 51-56	Memory blue data 0-7	I/O

Ordering Information

Type No.	Dot clock (MHz)	Package
HD66840F25	25MHz	100-pin
HD66840F30	30MHz	Plastic QFP (FP-100A)

Table 1. Pin Description (cont)

Symbol	Pin Number	Pin Name	I/O
PMOD0, PMOD1	78, 79	Program mode 0, 1	I
DOTE	80	Dot clock edge change	I
SPS	81	Synchronization polarity select	I
DM0-DM3	82-85	Display mode 0-3	I
$\overline{CS}$ (MPU programming)[11]	98	Chip select	I
MS0 (pin programming)[11]	98	Memory select 0	I
$\overline{WR}$ (MPU programming)[11,12]	99	Write	I
MS1 (pin programming)[11]	99	Memory select 1	I
$\overline{RD}$ (MPU programming)[12]	1	Read	I
A0 (ROM programming)	1	Address 0	O
XDOT (pin programming)	1	X-dot	I
RS (MPU programming)[11]	100	Register select	I
ADJ (pin programming)[11]	100	Adjust	I
D0-D3 (MPU programming)	5-8	Data 0-3	I/O
D0-D3 (ROM programming)	5-8	Data 0-3	I
F0-F3 (pin programming)	5-8	Fine adjust 0-3	I
A1-A3 (ROM programming)[13]	2-4	Address 1-3	O
YL0-YL2 (pin programming)[13]	2-4	Y-line 0-2	I
$\overline{RES}$[14]	97	Reset	I
$\overline{CD}$	86	Charge down	O
$\overline{CU}$	87	Charge up	O

Notes: 1. When CRT display data is monochrome, G and B pins should be fixed low.
2. Fix high or low when regenerating the display timing signal internally.
3. For 8-color display modes.
4. For monochrome and 8-level gray scale display modes.
5. Leave disconnected in 4-bit/single screen data transfer modes.
6. Leave disconnected in monochrome and 8-level gray scale display modes.
7. Leave disconnected when controlling TN-type LCD.
8. Leave disconnected when using no buffer memories.
9. Leave disconnected when using no buffer memories.
10. In monochrome display modes, the LVIC writes the OR of R, G, B signals into R-plane RAMs. Thus, no RAMs are required for G and B planes in these modes.
Pull up these pins 20-kΩ resistance. If G and B plane RAMs are connected in monochrome display modes, the LVIC writes G and B signals into each RAM. However, it does not affect the display or the contents of R-plane RAM whether G- and B-plane RAMs are connected or not.
11. Fix high or low when controlling the LVIC by ROM programming method.
12. $\overline{WR}$ and $\overline{RD}$ must not be low at the same time.
13. Fix high or low when controlling the LVIC by MPU programming method.
14. Make sure to input $\overline{RES}$ signal after power-on.

Power Supply

$V_{CC}1$-$V_{CC}3$: Connect $V_{CC}1$-$V_{CC}3$ with +5 V.

GND1-GND6: Ground GND1-GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYNC: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0-R3: R0-R3 output R data for the LCD.

LU0-LU3: LU0-LU3 output LCD up panel data.

G0-G3: G0-G3 output G data for LCD.

LD0-LD3: LD0-LD3 output LCD down panel data.

B0-B3: B0-B3 output B data for LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see "LCD System Configuration").

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see "LCD System Configuration").

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{MCS0}$, $\overline{MCS1}$: $\overline{MCS0}$ and $\overline{MCS1}$ output the buffer memory chip select signal.

$\overline{MWE}$: $\overline{MWE}$ outputs the write enable signal of buffer memories.

MA0-MA15: MA0-MA15 output buffer memory addresses.

RD0-RD7: RD0-RD7 transfer data between R data buffer memory and the LVIC.

GD0-GD7: GD0-GD7 transfer data between G data buffer memory and the LVIC.

BD0-BD7: BD0-BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0-PMOD1 input signals select a programming method (table 6).

DOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G, B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0-DM3: The DM0-DM3 input signals select a display mode (table 8).

MS0-MS1: The MS0-MS1 input signals select the kind of buffer memories (table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0-YL2: The YL0-YL2 input signals specify the number of vertical displayed lines (table 3).

ADJ: The ADJ input signal determines whether F0-F3 pins adjust the number of vertical displayed lines or the display timing signal. F0-F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0-F3: F0-F3 input data for adjusting the number of vertical displayed lines (table 4), or the display timing signal (see "Fine

Adjustment of Display Timing Signal").

MPU Interface

$\overline{CS}$: The MPU selects the LVIC when $\overline{CS}$ is low.

$\overline{WR}$: The MPU inputs the $\overline{WR}$ write signal to write data into internal registers of the LVIC. The MPU can write data when $\overline{WR}$ is low and cannot write data when high.

$\overline{RD}$: The MPU inputs the $\overline{RD}$ read signal to read data from internal registers of the LVIC. The MPU can read data when $\overline{RD}$ is low and cannot read data when high.

RS: The MPU inputs the RS signal together with $\overline{CS}$ to select internal registers. The MPU selects data registers (R0-R15) when RS is high and $\overline{CS}$ is low, and selects the address register (AR) when RS is low and $\overline{CS}$ is low.

D0-D3: D0-D3 transfer internal register data between the MPU and LVIC.

$\overline{RES}$: $\overline{RES}$ inputs the external reset signal.

ROM Interface

A0-A3: A0-A3 output address 0 to address 3 to an external ROM.

D0-D3: D0-D3 input data from an external ROM to internal registers.

PLL Circuit Interface

$\overline{CD}$: $\overline{CD}$ outputs the charge down signal to an external charge pump.

$\overline{CU}$: $\overline{CU}$ outputs the charge up signal to an external charge pump.

Table 2. Memory Type and MS1, MS0 Pins

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte memory
1	0	32-kbyte memory
1	1	64-kbyte memory

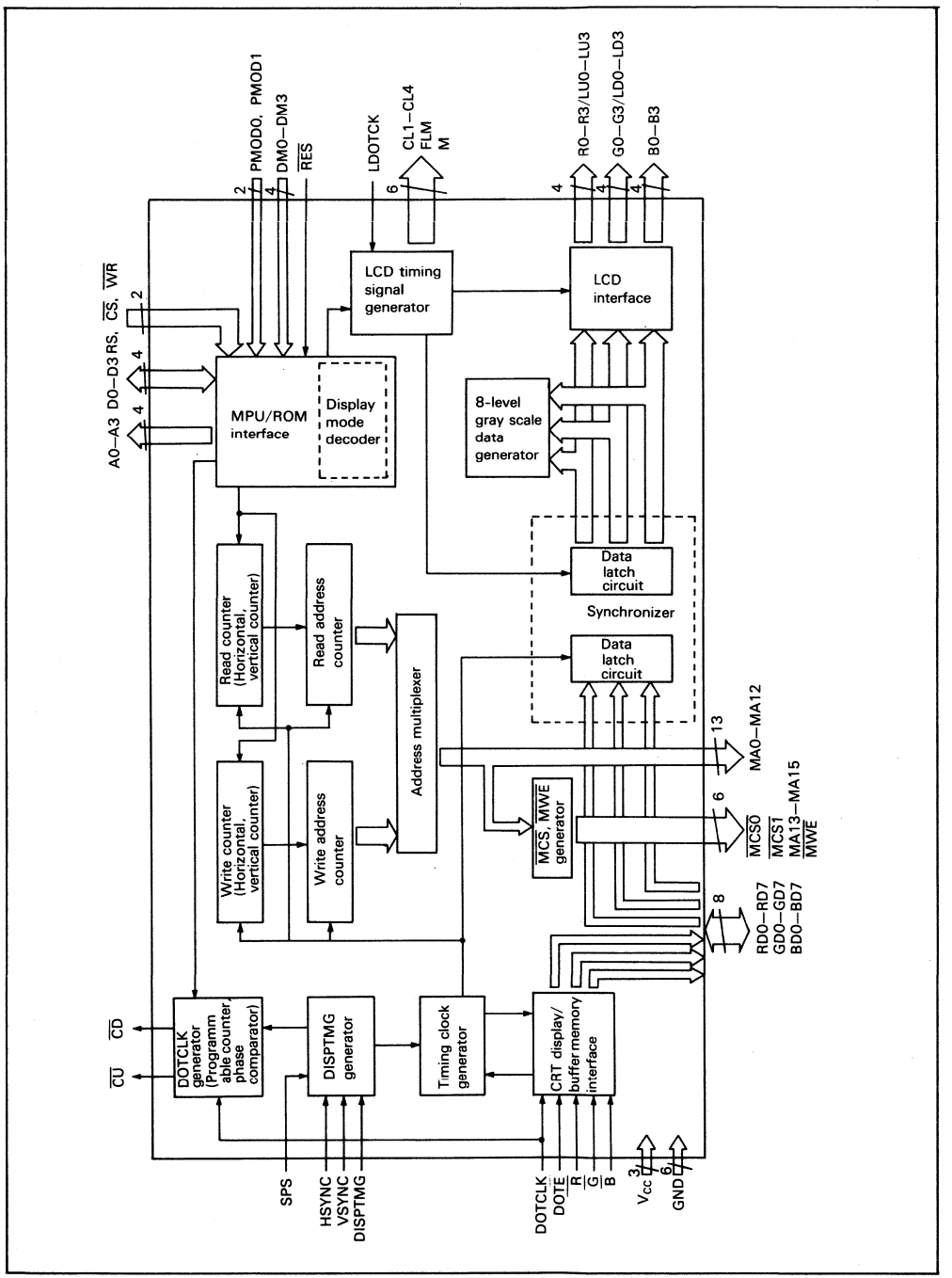
Table 3. Number of Vertical Displayed Lines and YL0-YL2 Pins

YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Prohibited
1	1	1	

Table 4. Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Lines Adjusted
0	0	0	0	± 0
0	0	0	1	+ 1
0	0	1	0	+ 2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+ 14
1	1	1	1	+ 15

Internal Block Diagram



Registers

Table 5 lists the internal registers and figure 1 illustrates the bit assignment to the registers.

Table 5. Register List

CS	RS	Address Register 3	2	1	0	Reg. No.	Register Name	Program Unit	Read/ Write
1	—	—	—	—	—	—	Invalid	—	—
0	0	—	—	—	—	AR	Address register[1]	—	W
0	1	0	0	0	0	R0	Control register 1	—	R/W
0	1	0	0	0	1	R1	Control register 2	—	R/W
0	1	0	0	1	0	R2	Vertical displayed lines register (middle-order)[2]	Line	R/W
0	1	0	0	1	1	R3	Vertical displayed lines register (low-order)[2]	Line	R/W
0	1	0	1	0	0	R4	Vertical displayed lines register (high-order)[2]	Line	R/W
							CL3 period register (high-order)[3]	Char	R/W
0	1	0	1	0	1	R5	CL3 period register (low-order)[3]	Char	R/W
0	1	0	1	1	0	R6	Horizontal displayed characters register (high-order)[4]	Char	R/W
0	1	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Char	R/W
0	1	1	0	0	0	R8	CL3 pulse width register	Char	R/W
0	1	1	0	0	1	R9	Fine adjust register[5]	Dot	R/W
0	1	1	0	1	0	R10	PLL frequency-dividing ratio register (high-order)[6]	—	R/W
0	1	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)[6]	—	R/W
0	1	1	1	0	0	R12	Vertical backporch register (high-order)[2,7]	Line	R/W
0	1	1	1	0	1	R13	Vertical backporch register (low-order)[2,7]	Line	R/W
0	1	1	1	1	0	R14	Horizontal backporch register (high-order)[2,7]	Dot	R/W
0	1	1	1	1	1	R15	Horizontal backporch register (low-order)[2,7]	Dot	R/W

Notes: 1. If you attempt to read data from the register with RS = 0, the bus is driven to high-impedance state and the output data is indefinite.
2. (The specified value − 1) should be written into these registers.
3. Valid only in 8-color display modes with horizontal stripes.
4. The most significant bit is invalid in dual screen configuration modes.
5. Valid only when the display timing signal is supplied externally.
6. Valid only when generating the dot clock.
7. Valid only when generating the display timing signal internally.

Register No.	Data Bit 3	2	1	0	
—					
AR	Address register				
R0			DSP	DCK	← Control register 1
R1	MC	DON	MS1	MS0	← Control register 2
R2	Vertical displayed lines register				
R3					
R4					
R5	CL3 period register				
R6	Horizontal displayed characters registor				
R7					
R8	CL3 pulse width register				
R9	Fine adjust register				
R10	PLL frequency-dividing ratio register				
R11					
R12	Vertical Backporch register				
R13					
R14	Horizontal Backporch register				
R15					

Note: ▨ indicates invalid bits. Attempting to read data from these register bits returns indefinite output data.

Figure 1. Register Bit Assignment

System Configuration

Figure 2 is the block diagram of a system in which the LVIC is used outside of a personal computer.

The LVIC converts the R, G, B serial data sent from the personal computer into parallel data and writes them into the buffer memories once. It reads out the data in turn and outputs them to LCD drivers to drive an LCD. Here the latch clock of the serial data, namely the dot clock (DOTCLK) is generated by a PLL circuit, using HSYNC as a basic clock. The frequency of the dot clock is specified by the PLL frequency-dividing ratio register (R10, R11).

The user may also configure a system without VCO and LPF if supplying the dot clock externally and may configure a system without the MPU if the LVIC is controlled by the pin programming method.

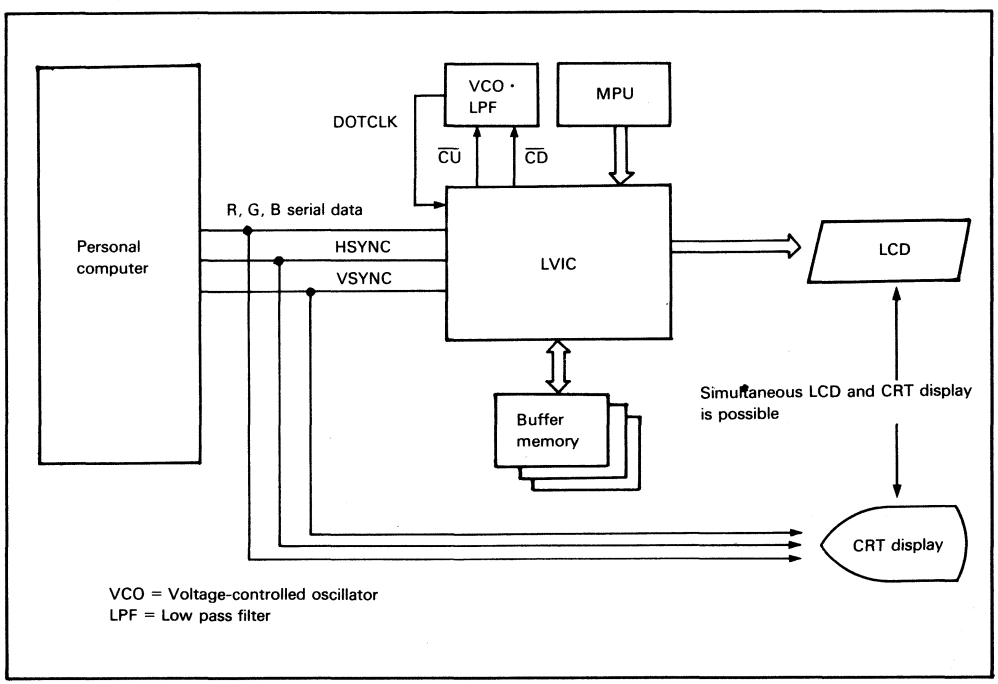


Figure 2. System Block Diagram (MPU Programming Method, Regenerates DOTCLK)

Functional Description

Programming Method

The user may select one of two methods to control the LVIC functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 6 lists the relation between programming method and pins.

Pin Programming Method: LVIC mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 3 illustrates the connections of MPU or ROM and the LVIC. Figure 3 (1) is an example of using a 4-bit microprocessor, but since the LVIC's MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 6. Programming Method Selection

Pins			
PMOD1	**PMOD0**	**Programming Method**	
0	0	Pin programming	
0	1	Internal register	With MPU
1	0	Programming	With ROM
1	1	Prohibited (Note)	

Note: This combination is for a test mode and disables display.

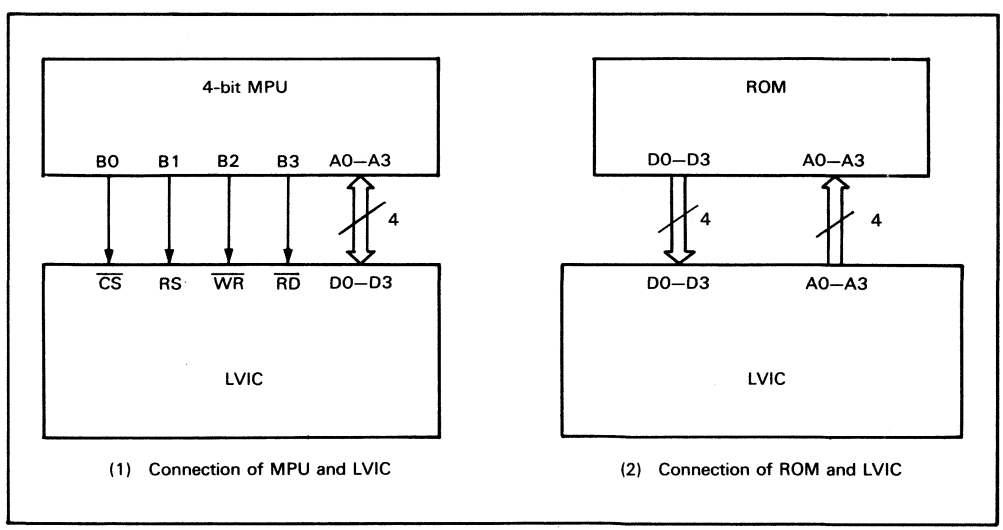


Figure 3. Connection of MPU or ROM and LVIC

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, the user may select either 640 dots or 720 dots (80 characters or 90 characters) as the number of horizontal displayed characters with the XDOT pin, and 200, 350, 400, 480, 512, or 540 lines as the number of vertical displayed lines with YL2-YL0 pins. The number of vertical displayed lines can be adjusted with ADJ and F3-F0 pins within +0 to +15 lines.

In the internal register programming method, the user may select any even number from 32 dots to 4048 dots (= 4 characters up to 506 characters) with the horizontal displayed characters register (R6, R7), and any even number from 4 lines up to 1028 lines with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, odd number of lines can also be selected when screen configuration is single and a Y-driver (scan driver) is set on one side of an LCD screen.

Figure 4 illustrates the relation between an LCD screen and pins and internal registers controlling screen size.

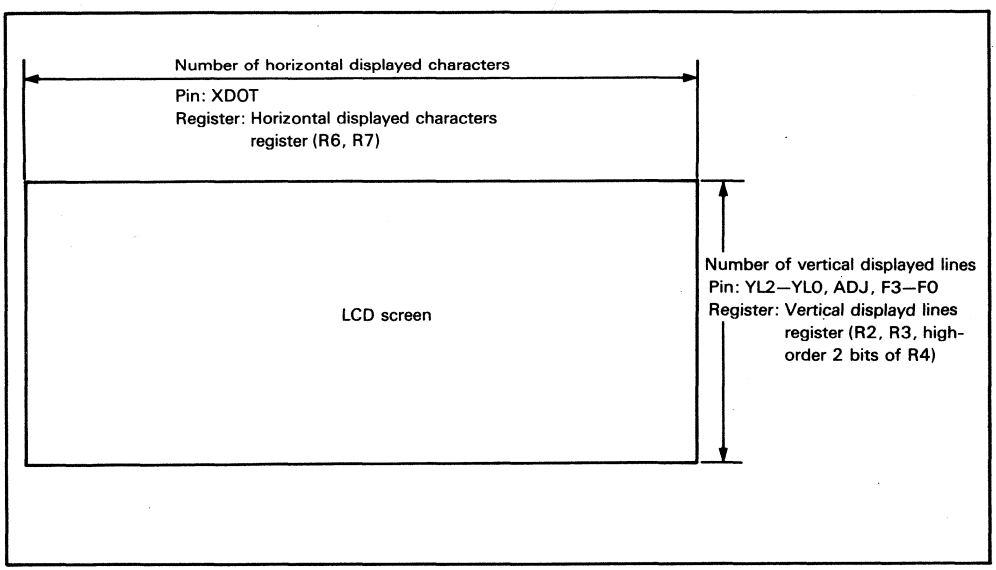


Figure 4. Relation between LCD Screen and Pins and Internal Registers

Memory Selection

The user may select 8-, 32-, or 64-kbyte SRAMs as buffer memory for the LVIC. Since the LVIC has a chip selector for these memories, no external decoder is required. The user selects the memory with pins MS1 and MS0 or with data bits MS1 and MS0 of the control register 2 (R1). Table 7 lists the kinds of memories and pin address assignments.

Memory capacity required depends on screen size and can be obtained with the following expression:

Memory capacity (bytes) = Nhd × Nvd

Nhd: number of horizontal displayed characters

Nvd: number of vertical displayed lines

For example, the screen of 640 × 200 dots requires 16-kbyte memory capacity since 80 characters × 200 lines is 16 kbytes. (8 dots compose a character.)
Therefore, each plane needs two HM6264s, which has 8-kbyte memory capacity, in 8-level gray scale display modes. Conncet $\overline{MCS0}$ with one of the memories of each plane and $\overline{MCS1}$ with the other (figure 5 (a)).

When the screen size is 640 × 400 dots, 32-kbyte memory capacity is required (figure 5 (b)).
Therefore, each plane needs a HM62256, which has 32-kbyte memory capacity.
Connect $\overline{MCS0}$ with $\overline{CS}$ of the memories here.

Table 7. Memories and Pin Address Assignment

Pins or Bits					
MS1	**MS0**	**Memory**	**Address Output Pins**	**Chip Select Pins**	**Address Assignment**
0	0	No memory[1]	—	—	—
0	1	8-kbyte	MA0-MA12	$\overline{MCS0}$	$0000-$1FFF
				$\overline{MCS1}$	$2000-$3FFF
				MA13	$4000-$5FFF
				MA14	$6000-$7FFF
				MA15	$8000-$9FFF
1	0	32-kbyte	MA0-MA14	$\overline{MCS0}$	$00000-$07FFF
				$\overline{MCS1}$	$08000-$0FFFF
				MA15	$10000-$17FFF
1	1	64-kbyte	MA0-MA15	$\overline{MCS0}$	$00000-$0FFFF
				$\overline{MCS1}$	$10000-$1FFFF

Note: 1. There are some limitations when the user uses no memory. Refer to "User Precautions."

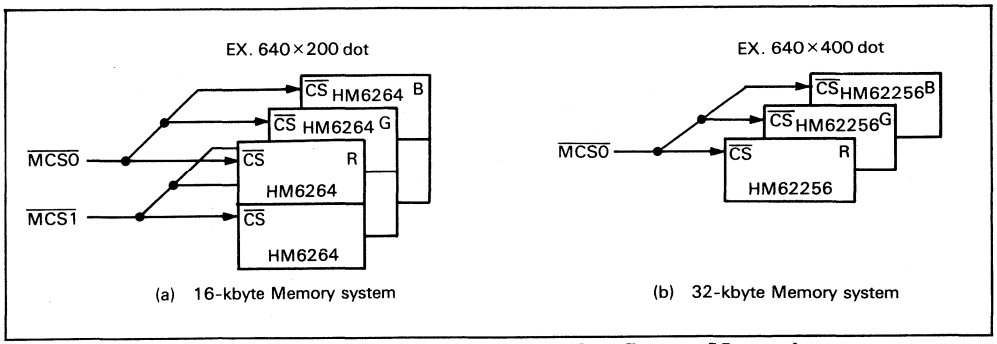


Figure 5. Relation between Display Screen Memories

Display Modes

The LVIC supports 16 display modes, depending on the state of the DM3-DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 8 lists display modes.

Table 8. Modes List

Mode	Pins				Display	LCD Data Output		LCD Driver Setting			
						Data	Screen				
No.	DM3	DM2	DM1	DM0	Color	Transfer	Config.	X-Driver[2]	Y-Driver[3]	Stripe[4]	Alternating
1	0	0	0	0	Monochrome	4-bit	Dual	One side	One side	—	Per frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bit			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level	4-bit	Dual		One side		
7	0	1	1	0	gray scale		Single				
8	0	1	1	1		8-bit					
9[1]	1	0	0	0	8-clolor	12-bit				Vertical	Per line
10[1]	1	0	0	1		(4 bits			Both sides		
11[1]	1	0	1	0		for R,G,B		Both sides	One side		
12[1]	1	0	1	1		each)			Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16[1]	1	1	1	1					Both sides		

Notes: 1. For TFT-type LCD.
2. Data output driver
3. Scan driver
4. Refer to "Display Color, 8-Color Display."

Display Color

The LVIC converts R, G, B, the color data for CRT display, into the monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to Mode 5): In monochrome modes 1-5, the LVIC displays two colors, namely black (= display on) and white (= display off). As shown in table 9, the OR of CRT display R, G, B data determines the display color.

8-Level Gray Scale Display (Mode 6 to Mode 8): In 8-level gray scale modes 6-8, the LVIC thins out data on certain lines to display an 8-level gray scale according to CRT display color (luminosity). Table 10 shows the relation between CRT display color (luminosity) and LCD color (contrast).

8-Color Display (Mode 9 to Mode 16): In 8-color modes 9-16, the LVIC displays 8 colors with red (R), green (G), and blue (B) filters on liquid crystal cells. The eight colors are the same as those provided by CRT display. As illustrated in figure 5, 8-color display has of two stripe modes: horizontal stripe mode and vertical stripe mode. In the former mode, the LVIC arranges R, G, B data horizontally, with horizontal filters. In the latter mode, the LVIC arranges R, G, B data vertically, with vertical filters. Three cells express a dot in both modes.

Table 9. Monochrome Display

CRT Display Data				LCD		
R	G	B	CRT Display Color	On/Off	Color	
1	1	1	White	On	Black	
1	1	0	Yellow	On	Black	
0	1	1	Cyan	On	Black	
0	1	0	Green	On	Black	
1	0	1	Magenta	On	Black	
1	0	0	Red	On	Black	
0	0	1	Blue	On	Black	
0	0	0	Black	Off	White	

Table 10. 8-Level Gray Scale Display

CRT Display Data			CRT		LCD		
R	G	B	Color	Luminosity	Color	Contrast	
1	1	1	White	High	Black	Strong	
1	1	0	Yellow				
0	1	1	Cyan				
0	1	0	Green				
1	0	1	Magenta				
1	0	0	Red				
0	0	1	Blue				
0	0	0	Black	Low	White	Weak	

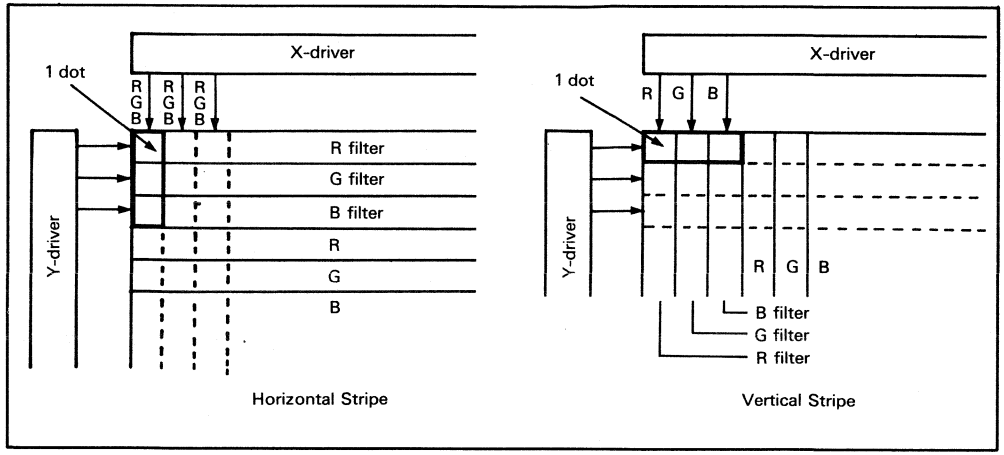


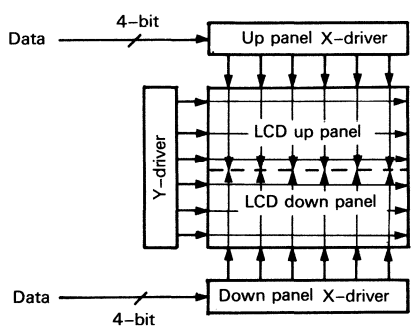
Figure 6. Stripe Modes in 8-Color Display

LCD System Configuration

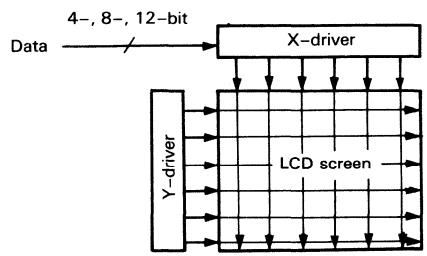
The LVIC supports the following system configurations for LCD:

- Types of LCD data output:
  —Data transfer: 4-bit, 8-bit, or 12-bits (4 bits for R, G, B each)
  —Screen configuration: Single or dual
- How to set LCD drivers around LCD screen:
  —X-driver: On one side or on both sides
  —Y-driver: On one side or on both sides

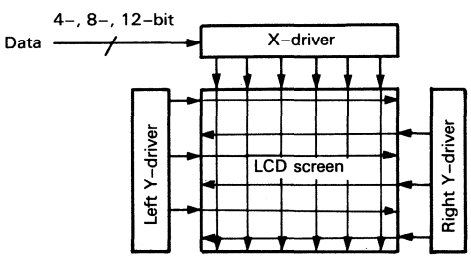
Figure 7 illustrates these system configurations by mode.



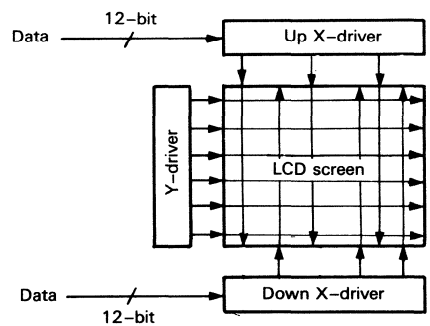
Svstem Configuration for Mode 1 and Mode 6 (4-Bit Data Transfer, Dual Screen, X-Driver and Y-Driver on One Side Each) (Note)



System Configuration for Modes 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on One Side Each)



System Configuration for Modes 3, 5, 10, and 14 (4-, 8-, or 12-Bit Data Transfer, Single Screen, X-Driver on One Side and Y-Driver on Both Sides)



System Configuration for Mode 11 and Mode 15 (12-Bit Data Transfer, Single Screen, X-Driver on Both Sides and Y-Driver on One Side)

Note: Although there are two X-drivers, the X-driver is considered to be set on one side, not on both sides, because the LCD up panel and down panel are each regarded as one screen.

Figure 7. System Configurations by Mode

Calculation of LDOTCK

LDOTCK frequency f_L is calculated from the following expression:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd : number of horizontal characters displayed on LCD

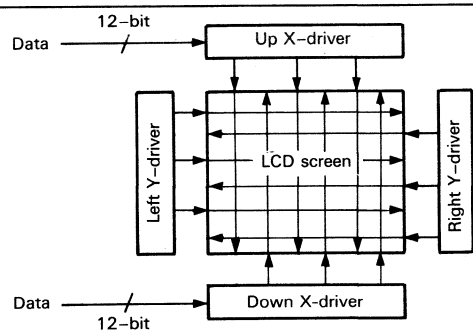
Nvd : number of virtical displayed lines on LCD

f_F : FLM frequency

Here f_L must hold the following relation, where f_D is frequency of dot clock for CRT display (= DOTCLK).

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (The LDOTCK phase must be inverse of the DOTCLK phase in this case)



System Configuration for Mode 12 and Mode 16
(12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on Both Sides Each)

Notes: 1. X-drivers on both sides: Data output wires run from up and down X-drivers alternately, which widens the interval between wires to twice that in case of an X-driver an one side (figure 8).

2. Y-drivers on both sides: Line select signal output wires run from right and left Y-drivers alternately, which widens the interval between wires to twice that in case of Y-driver on one side (figure 9).

Figure 7. System Configurations by Mode (cont)

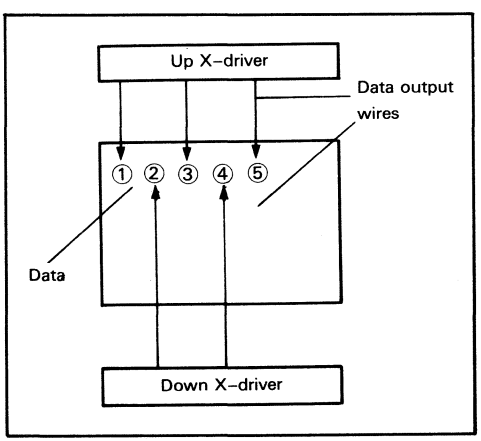


Figure 8. X-Drivers on Both Sides

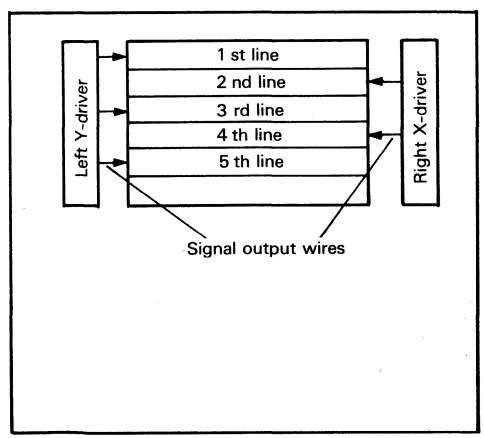


Figure 9. Y-Drivers on Both Sides

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the LVIC needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The LVIC can generate the display timing signal from HSYNC and VSYNC. Figure 10 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15) respectively.

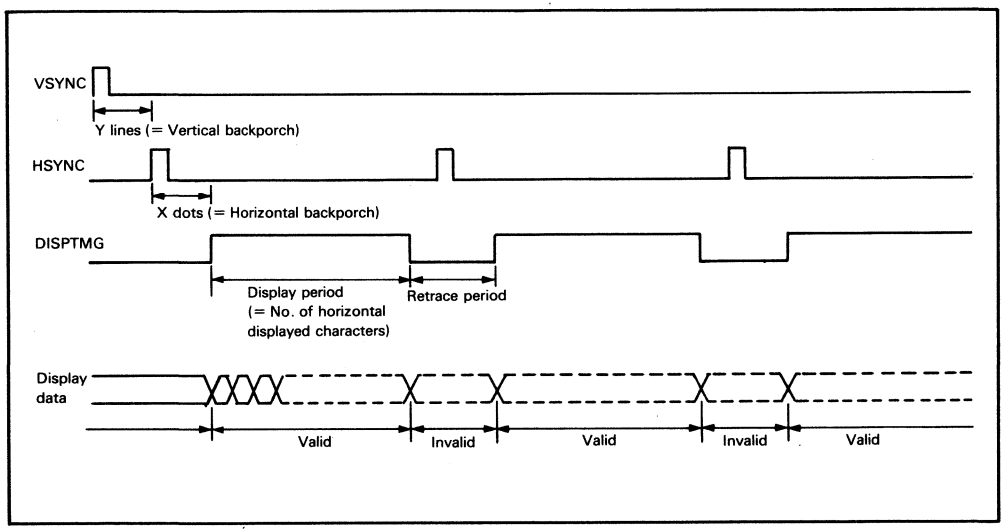


Figure 10. Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal and does not appear from the CRT display plug. Thus it is necessary to generate the dot clock. The LVIC has a programmable counter and a phase comparator which are parts of a PLL circuit, and can generate the dot clock from HSYNC if a charge pump, a low pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

Figure 11 is a block diagram of a PLL circuit. A PLL (phase-locked loop) circuit is a feedback controller regenerating a clock whose frequency and phase are the same as those of a basic clock. The basic clock is HSYNC here.

At power-on,VCO outputs to the programmable counter a signal whose frequency depends on the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock and HSYNC and outputs $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs $\overline{CU}$ when the frequency of the clock is lower than that of HSYNC or when the phase of the clock is behind that of HSYNC, while it outputs $\overline{CD}$ in the contrary case. The charge pump and LPF apply voltage to the VCO according to $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and the frequency of the frequency-divided clock coincide with those of HSYNC, making it a stable dot clock.

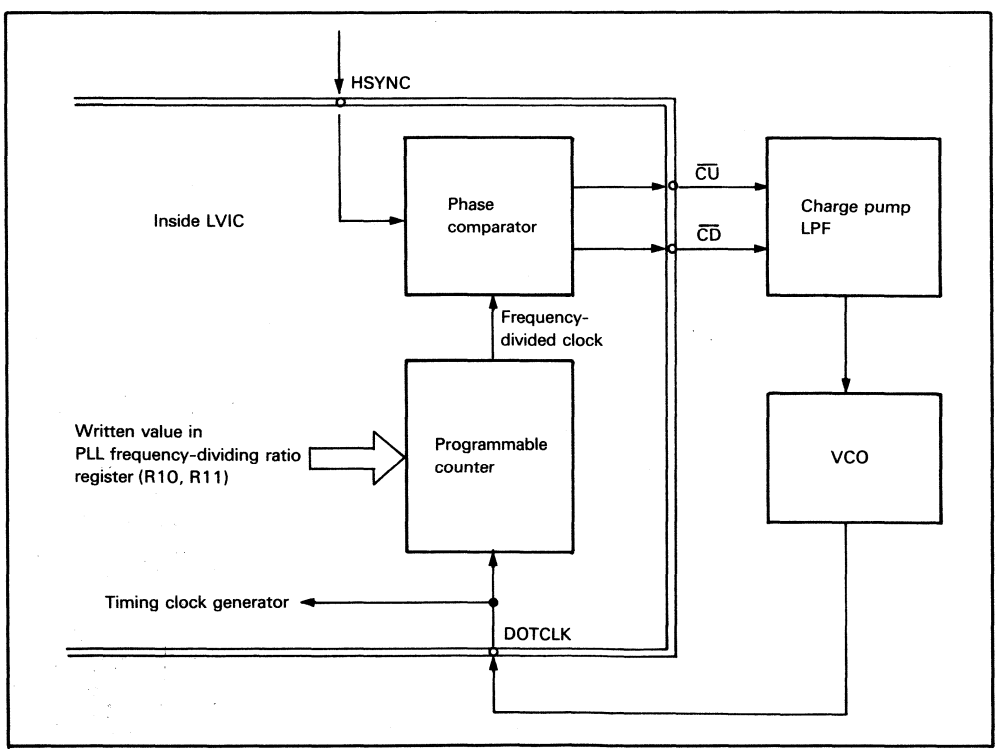


Figure 11. PLL Circuit Block Diagram

Doubled-in-Height Display

Doubled-in-height display doubles characters and pictures in height as illustrated in figure 12.

In TN-type LCD modes (= modes 1, 2, 4, 6, 7, and 8), CL3 frequency is twice as high as CL1 frequency (figure 13). As a result, using CL3 instead of CL1 as a shift clock (figure 14) enables two lines to be selected while an X-driver (data output driver) is outputting the same data, realizing doubled-in height display. However, the following procedures are necessary in this display since multiplexing duty ratio becomes twice as great as the value specified as the number of vertical displayed lines.

1. Halve the frequency of the LCD dot clock (= LDOTCK)
2. Halve the number of vertical displayed lines

This function is provided only for TN-type LCD.

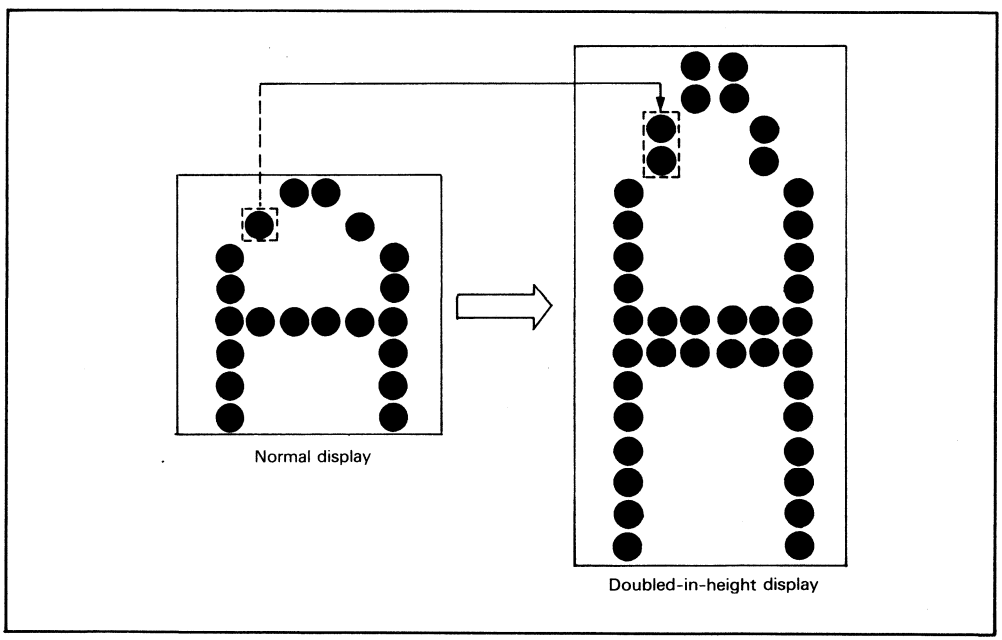


Figure 12. Doubled-in-Height Display Example

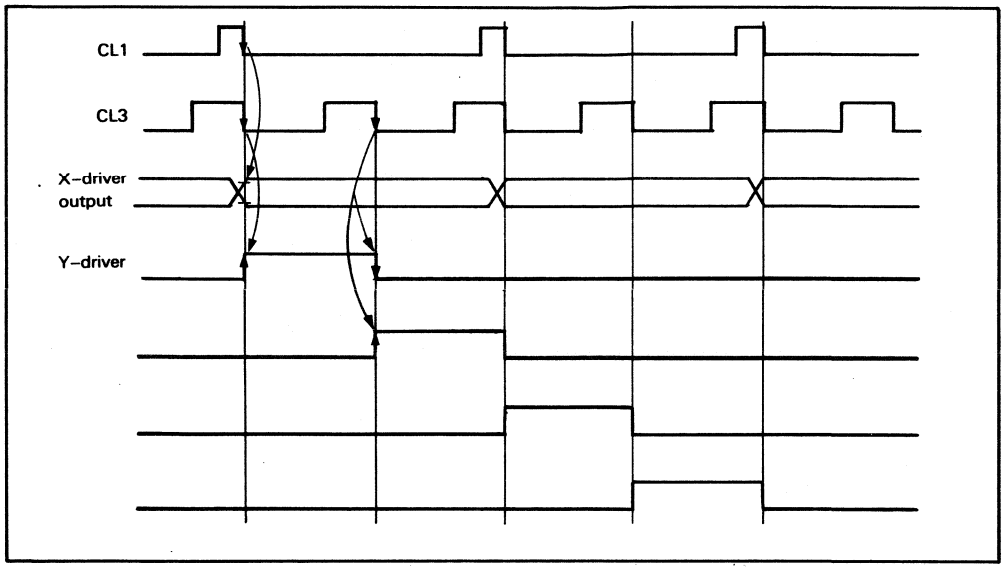


Figure 13. Relation between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

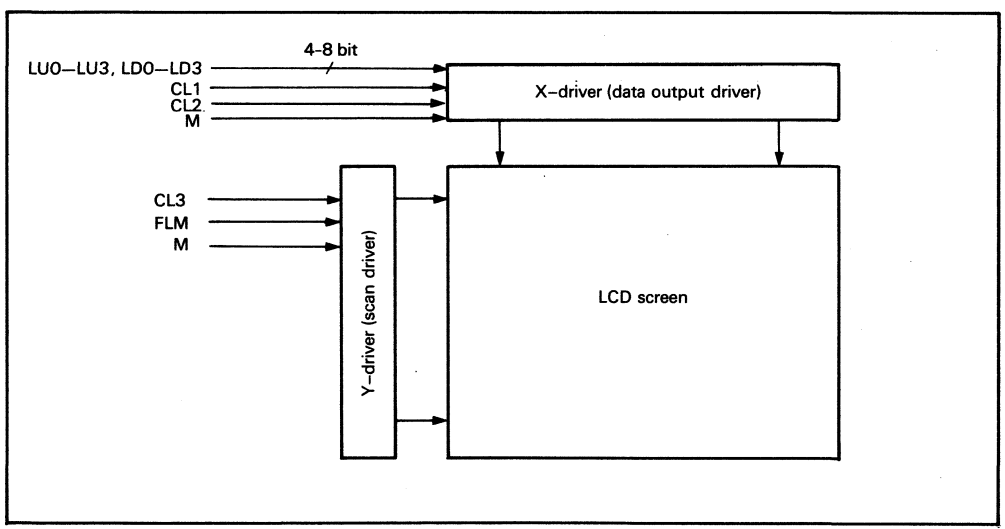


Figure 14. Connection for Doubled-in-Height Display

Display Timing Signal Fine Adjusment

When the display timing signal is supplied externally, a phase shift might appear between CRT data and the display timing signal. This is because each signal has its own peculiar lag. The LVIC can adjust the display timing signal with the F0-F3 pins or the fine adjust register (R9) to correct this phase shift.

Table 11 shows the relation between F3-F0 pins, data bit 3 to data bit 0 of the fine adjust register, and fine adjustment. Concerning the polarity of the number of dots adjusted, − indicates advancing the phase of the display timing signal and + indicates delaying it. F3 pin or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Figure 15 shows examples of adjusting the display timing signal. Since the signal is two dots ahead of the display start position in case (1), (F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) should be set to (1, 0, 1, 0) to delay the signal for two dots. Since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal for two dots. When there is no need to adjust the signal, settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 11. Pins, Data Bits of R9, and Fine Adjustment

Pin:	F3	F2	F1	F0	Number of Dots
R9 Bit:	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	− 1
		⋮	⋮	⋮	⋮
		1	1	0	− 6
		1	1	1	− 7
	1	0	0	0	0
		0	0	1	+ 1
		⋮	⋮	⋮	⋮
		1	1	0	+ 6
		1	1	1	+ 7

Note: When adjusting the display timing signal with pins, set ADJ pin to 1.

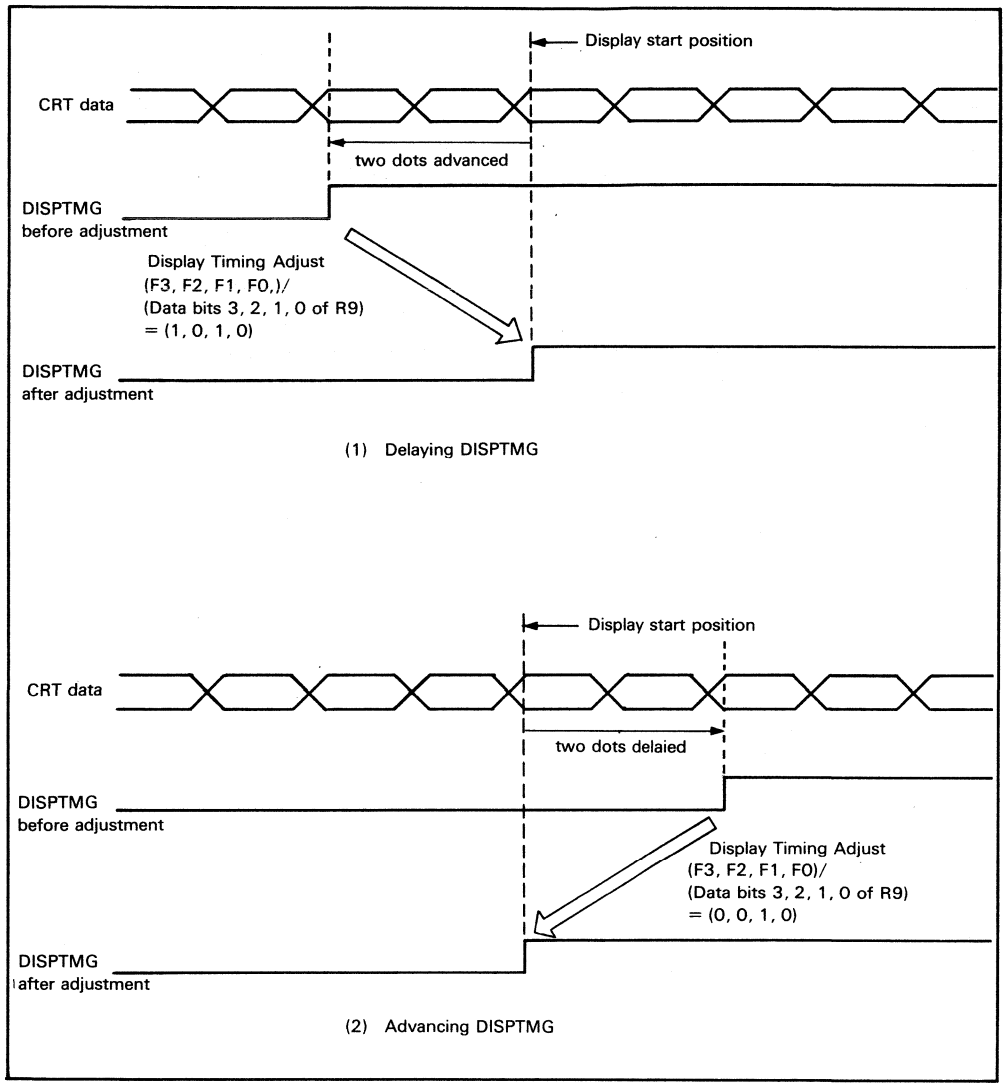


Figure 15. Adjustment of Display Timing Signal

Internal Registers

The LVIC has an address register (AR) and sixteen data registers (R0-R15). In order to specify one of the sixteen data registers, write its register address into the address register. The MPU transfers data to the data register corresponding to the written address.

All the registers are valid only when the LVIC is controlled by the internal register programming method and are invalid (don't care) when by the pin programming method.

Address Register (AR)

The address register (figure 16) is composed of four bits and specifies one data register out of sixteen. This register is selected by the MPU when RS pin is low and specifies any data register with the register address written by the MPU.

Control Register 1 (R0)

Control register 1 (figure 17) is composed of four bits, including two invalid bits. Each of two valid bits has its own function. Reading from and writing into invalid bits are passible. However, these operation does not affect the LSI function.

- DSP Bit
  —DSP = 1: LVIC generates the display timing signal
  —DSP = 0: LVIC does not generate the display timing signal
  (If DCK = 1, the display timing signal is generated in spite that DSP = 0)

- DCK Bit
  —DCK = 1: LVIC generates the dot clock
  —DCK = 0: LVIC does not generate the dot clock

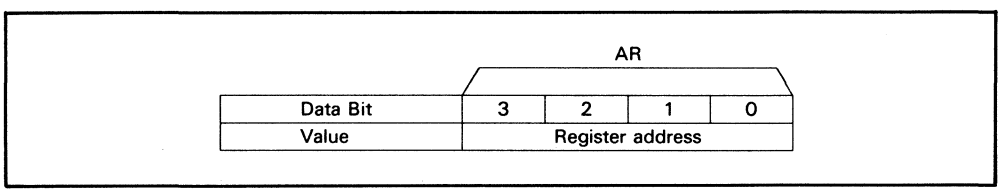


Figure 16. Address Register

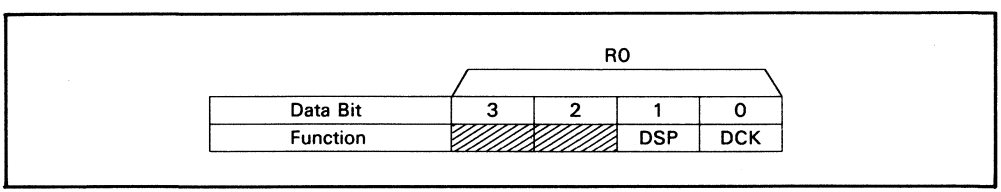


Figure 17. Control Register 1

Control Register 2 (R0)

Control register 2 (figure 18) is composed of four bits and has three functions.

- MC Bit
  —MC = 1: M signal alternates per line
  —MC = 0: M signal alternates per frame
- DON Bit
  —DON = 1: Display on
  —DON = 0: Display off
- MS1 and MS0 Bits
  —Select the memory type (table 12)

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4), CL3 Period Register (Low-order 2 Bits of R4, R5)

The vertical displayed lines register (figure 19) is composed of ten bits (R2 + R3 + high-order two bits of R4) and specifies the number of vertical displayed lines. This register can specify both even and odd numbers in modes for a Y-driver on one side and single screen configuration, but even numbers only in the other modes. The value to be written into this register is (Nvd − 1), where Nvd = number of vertical displayed lines.

The CL3 period register is composed of six bits (low-order two bits of R4 + R5) and specifies the period of CL3 in 8-color display modes with horizontal stripes. Thus this register is invalid in the other modes. CL3 is a clock for the LVIC to output R, G, B data separately to LCD drivers. The value to be written into this register is (Nhd + 6) × 1/3 − 1, where Nhd = number of horizontal displayed characters. When (Nhd + 6) is not divisible by 3, the quotient should be rounded up or rounded down.

Table 12. Memory Type and MS1, MS0

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte
1	0	32-kbyte
1	1	64-kbyte

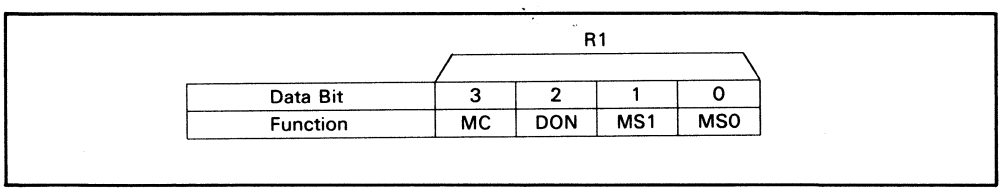


Figure 18. Control Register 2

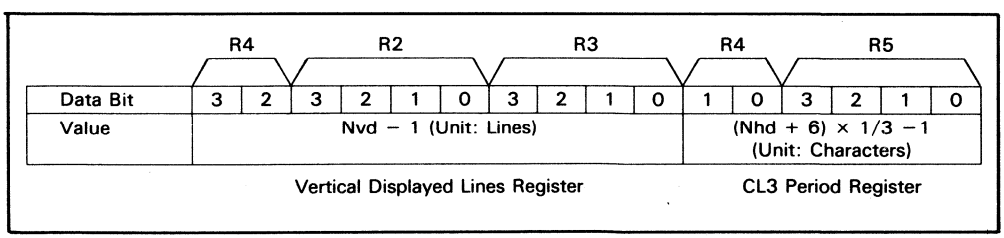


Figure 19. Vertical Displayed Lines Register and CL3 Period Register

Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 20) is composed of eight bits (R6 + R7) and specifies the number of horizontal displayed characters. This register can specify even numbers only. The most significant bit of R6 is invalid in the modes for dual screen configuration. When writing into this register, shift (Nhd − 1) in the low-order direction for one bit to cut off the least significant bit. Figure 20 shows how to write a value into the register when Nhd = 90.

CL3 Pulse Width Register (R8)

The CL3 period register (figure 22) is composed of four bits and specifies the high-level pulse width of CL3. When controlling TFT-type LCDs, each gate of the LCD has to hold data from the time a Y-driver outputs the line select and shift signal to the time an X-driver the outputs next display data. Data must be held while CL3 is high. However, even when the LVIC is not controlling TFT-type LCDs, CL3 appears with the high-level pulse width specified by this register.

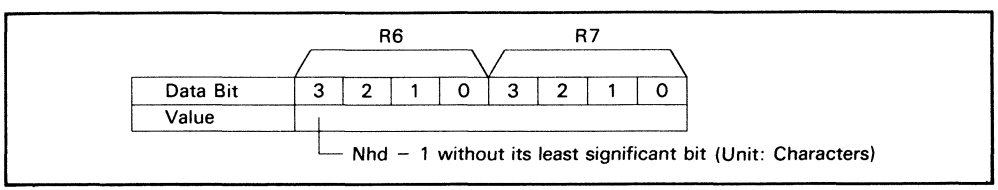


Figure 20. Horizontal Displayed Characters Register

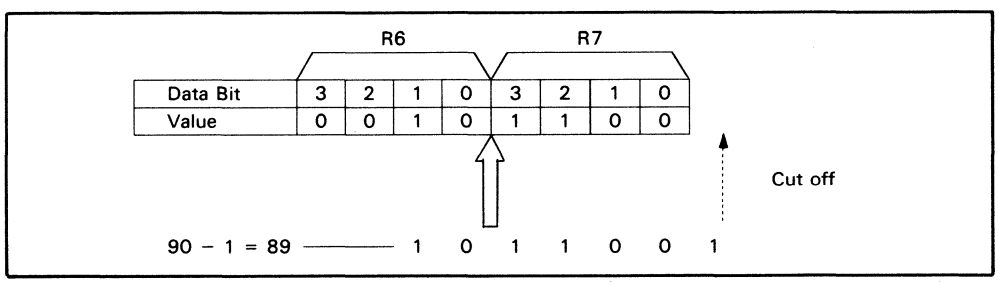


Figure 21. How to Write The Number of Horizontal Displayed Characters

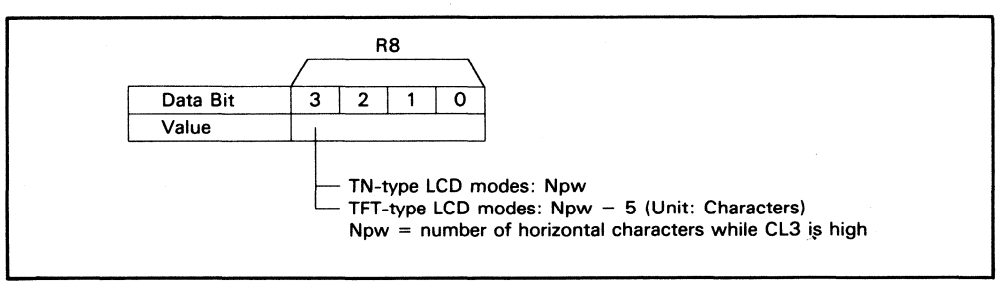


Figure 22. CL3 Pulse Width Register

Fine Adjust Register (R9)

The fine adjust register (figure 23) is composed of four bits and adjusts the externally supplied display timing signal to synchronize its phase with that of LCD data. The value to be written into this register is determined by the interval between the positive edge of the display timing signal and the display start position. For more details, refer to "Display Timing Signal Fine Adjustment." This register is invalid when the display timing signal is generated internally.

PLL Frequency-Dividing Ratio Register (R10, R11)

The PLL frequency-dividing ratio register (figure 24) is composed of eight bits (R10 + R11) and specifies the PLL frequency-dividing ratio for generating a dot clock by a PLL circuit. The value to be written into this register is determined by the ratio of the frequency of HSYNC to that of the dot clock which the user wants. This register is invalid when the dot clock is supplied externally and is valid only when the LVIC is controlled by the internal register programming method and the DCK bit of control register 1 (R0) is 1. The written value in this register (N_{PLL}) is obtained with the following expression:

N_{PLL} = Ncht × 8 − 731

Ncht: total number of characters for CRT

Ncht can be obtained as follows from the specifications of a CRT monitor:

Ncht = 1/8 × (DOTCLK frequency)/(HSYNC frequency)

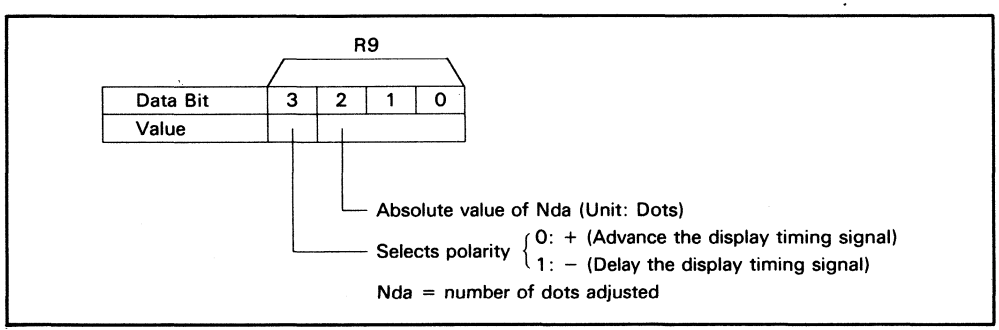


Figure 23. Fine Adjust Register

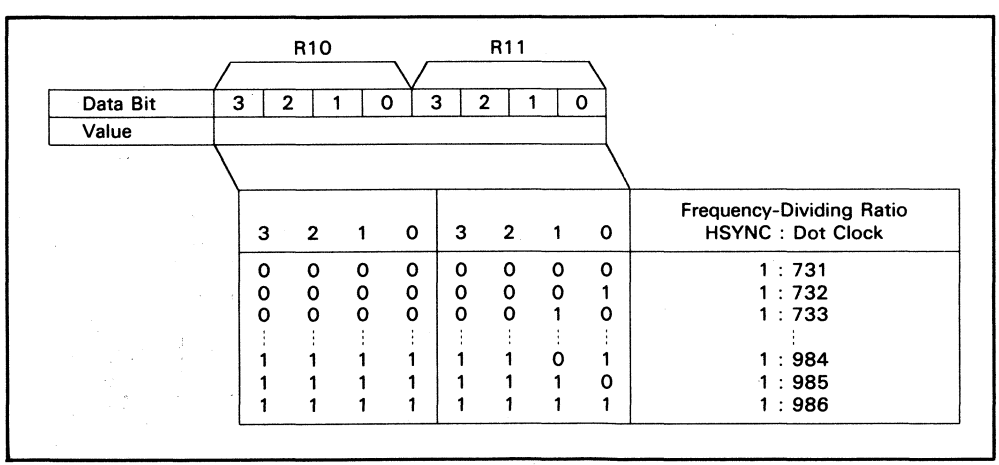


Figure 24. PLL Frequency-Dividing Ratio Register

Vertical Backporch Register (R12, R13)

The vertical backporch register (figure 25) is composed of eight bits (R12 + R13) and specifies the vertical backporch. The vertical backporch is the number of lines between the positive edge of VSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation." This register is invalid when the display timing signal is supplied externally and is valid only is a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be regenerated and the register is enabled even when DSP = 0.)

Horizontal Backporch Register (R14, R15)

The horizontal backporch register (figure 26) is composed of eight bits (R14 + R15) and specifies the horizontal backporch. The horizontal backporch is the number of characters between the posive edge of HSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation". This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be generated and this register is enabled even when DSP = 0.)

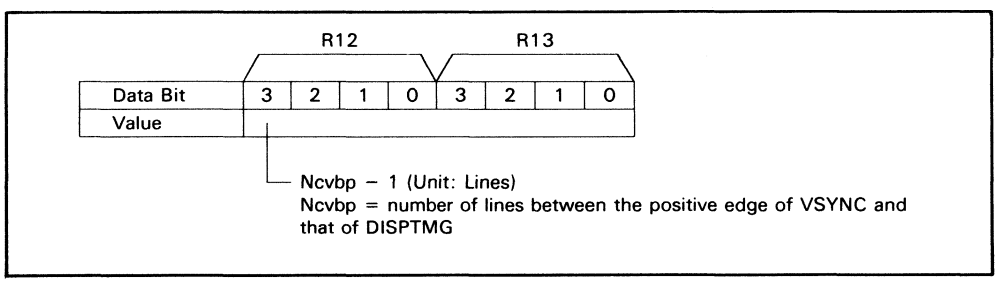


Figure 25. Vertical Backporch Register

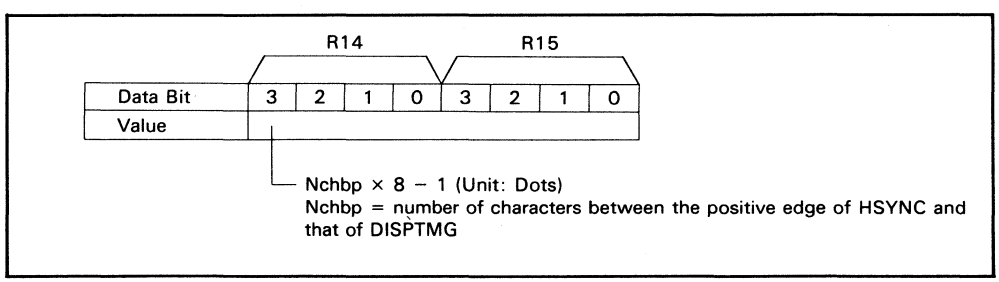


Figure 26. Horizontal Backporch Register

Reset

$\overline{RES}$ pin resets and starts the LVIC. Make sure to hold the reset signal low for at least 1 μs after power-on.

Reset is defined as shown in figure 27.

State of Pins During Reset

$\overline{RES}$ basically does not control output pins and operates regardless of the other input pins. Output pins can be classified into the following five groups depending on their reset state.

1. Keeps state before reset: CL2
2. Driven to high-impedance state (fixed low when using no memory): RD0-RD7, GD0-GD7, BD0-BD7
3. Fixed high: $\overline{MWE}$, CL4, M, $\overline{CD}$, $\overline{MCS1}$
4. Fixed low: MA0-MA12, R0-R3, G0-G3, B0-B3, $\overline{CS}$, CL1, CL3, FLM, A0-A3, $\overline{CU}$
5. Fixed high or low depending on the memory in use (table 13): MA13-MA15, $\overline{MCS0}$

State of Registers During Reset

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be both read and written by the MPU even during reset. Registers keep the contents they had before reset until they are rewritten.

Memory Clear Function

After reset, the LVIC writes 0 in the memory area specified by MSEL0 and MSEL1 (table 7) regardless of R, G, B data.

Table 13. Memory Type and State of Pins During Reset

Kind of Memories	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbyte memory	High	High	High	Low
32-kbyte memory	Low	Low	High	Low
64-kbyte memory	Low	Low	Low	Low

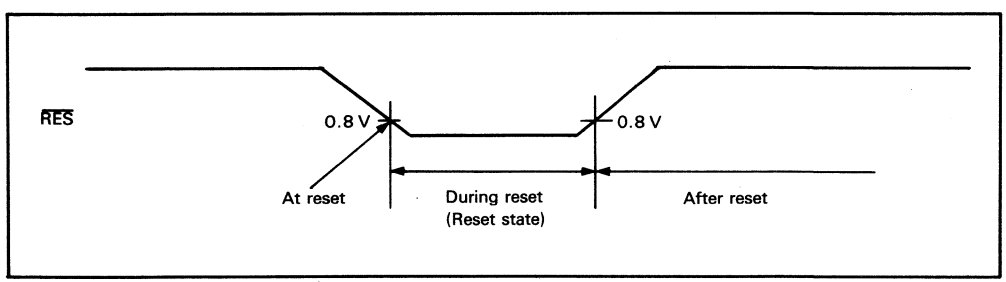


Figure 27. Reset Definition

User Precautions

1. There are following limitations when the user uses no memory. (MSEL0 = 0, MSEL1 = 1)
   - The display modes for dual screen configuration (= mode 1 and mode 6) are disabled.
   - The LVIC cannot support the LCD systems with Y-drivers on both sides. Even if the user selects the mode for the system with Y-drivers on both sides (= mode 3, 5, 10, 12, 14, or 16), the operation of the LVIC is exactly the same as that in the mode for the system with Y-driver on one side (= mode 2, 4, 9, 11, 13, or 15).
     And leave CL4 terminal disconnected in this usage.
2. The LVIC might operate irregularly until the internal registers have been written after reset in the system which controls the LVIC by internal register programming method.
3. Memory clear function might not work normally at power-on or after reset if MSEL0 and MSEL1 are not properly set to the value corresponding to the memories in use.
4. Since the LVIC is a CMOS LSI, input pins must not be left disconnected. Refer to table 1 concerning how to deal with each pin.

Programming

The values written in internal registers have the limit listed in table 14. The symbols in the table are difined as shown in table 15 and figure 27.

Table 14. Limit on Values Written in Registers

Function	Limit	Notes	Applicable Registers
Screen Configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$	1,8	R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$		
	$(Nhd + 6) \times n \times Nvd \times f_F \leqq f_D \leqq 30$ MHz	2,8	R2, R3, R4, R6, R7
CL3 Control	$1 \leqq Npw \leqq (Nhd + 6) \times 1/2 - 1$	3	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	4	
	$1 \leqq Npw \leqq Npc - 1$	5	
DISPTMG	$1 \leqq Nchbp \leqq 256$	6	R12, R13, R14, R15
Regeneration	$1 \leqq Ncvbp \leqq 256$	6	
Without Buffer Memory	$4 \leqq Nhd \leqq Nchsp - 4$	7	R2, R3, R4, R6, R7
	$4 \leqq Nvd \leqq Ncvsp - 4$	7	

Notes: 1. $Nhd \leqq 256$ in dual screen configuration (= mode 1 and mode 6)
2. f_F: FLM frequency, f_D: frequency of CRT dot clock, f_L: frequency of LCD dot clock for LCD
   $f_L < f_D \times 15/16$, or $f_L = f_D$
3. In modes 1, 2, 4, 6, 7, and 8
4. In modes 3, 5, 9, 10, 11, and 12 (Npw = (value in R8) + 5)
5. In modes 13, 14, 15, and 16 (Npw = (value in R8) + 5)
6. Value in R14, R15 $\leqq$ (Nchsp $\times$ n + Nchbp) $-$ Nhd $\times$ n $-$ 2
   Value in R12, R13 $\leqq$ (Ncvsp + Ncvbp) $-$ Nvd $-$ 2
7. Nht = Nchsp + Nchbp $\times$ 1/n, Nd = Ncvbp + Ncvsp
   (Nht = Nhd + 6, Nd = Nvd when using buffer memory)
8. n: Horizontal character pitch (the number of horizontal dots in one character).

Table 15. Symbol Definition

Symbol	Definition
Nchd	Number of horizontal displayed characters on CRT display
Nchsp	Number of characters between the positive edge of DISPTMG and that of HSYNC (= Horizontal sync position)
Nchbp	Number of dots between the positive edge of HSYNC and that of DISPTMG (= horizontal backporch)
Ncvbp	Number of lines between the negative edge (positive edge when VSYNC is high in active state) of VSYNC and the first positive edge of DISPTMG (= vertical backporch)
Ncvsp	Number of lines between the first positive edge of DISPTMG and the next negative edge of VSYNC (= vertical sync position)
Ncvd	Number of vertical displayed lines on CRT display
Nhd	Number of horizontal displayed characters (on LCD)
Npc	Number of characters during CL3 period (= CL3 pulse cycle)
Npw	Number of characters while CL3 is high (= CL3 pulse width)
Nht	Total number of horizontal characters
Nvd	Number of vertical displayed lines (on LCD)

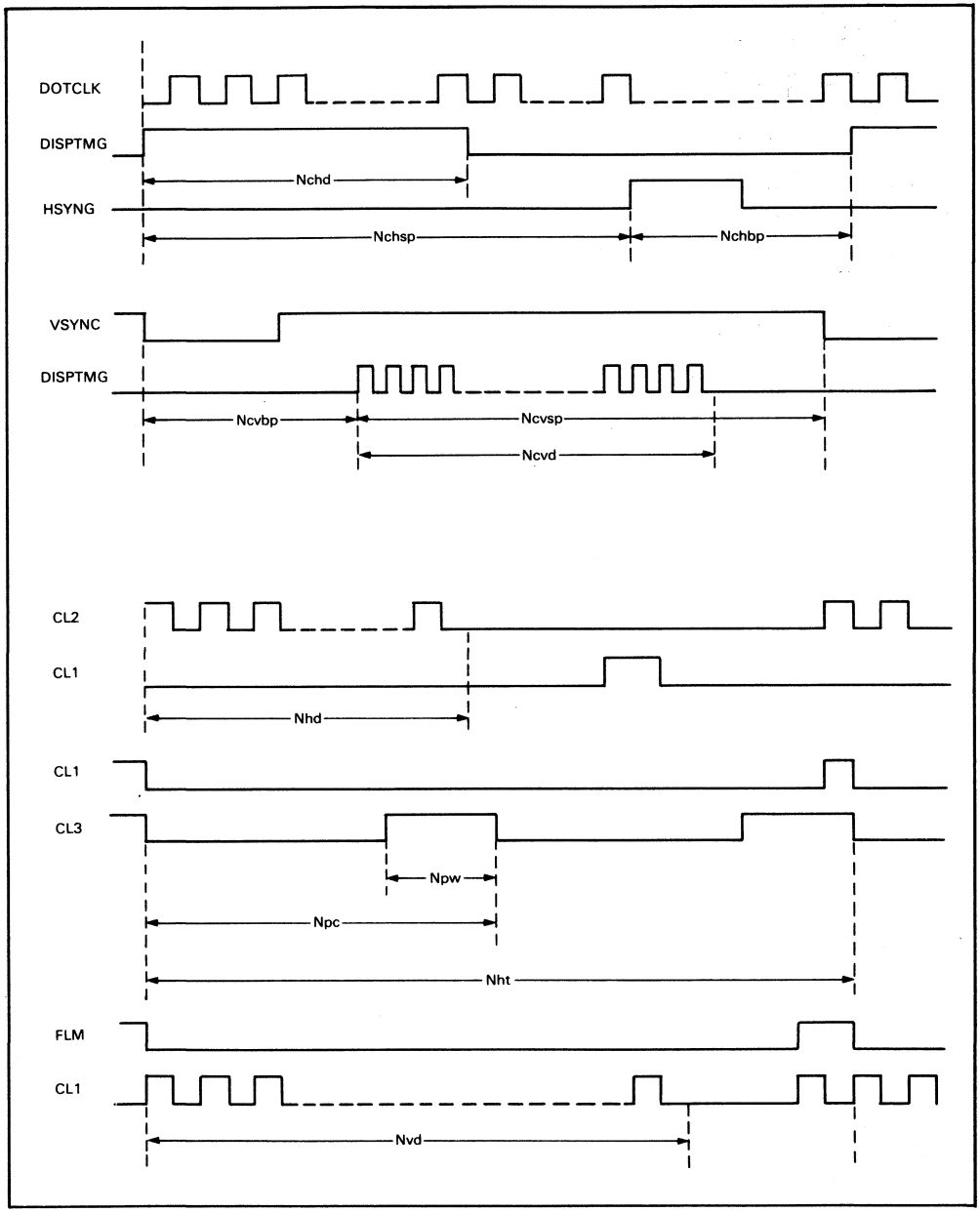


Figure 28. Symbol Definition

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	− 20 to + 75	°C
Storage temperature	T_{stg}	− 55 to + 125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of the LSI.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1]		2.0	V_{CC} + 0.3		
	TTL interface[4]		2.2	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	TTL interface[5]		−0.3	0.6		
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2
2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG
4. TTL interface: $\overline{WR}$/MS1, LDOTCK, DOTCLK
5. TTL interface: $\overline{WR}$/MS1

DC Characteristics 2 (V_{CC} = 5.0 V ± 5 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1]		2.0	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, DOTCLK, LDOTCK, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2

2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

AC Characteristics (V_{CC} = 5.0 V ±10 %, GND = 0 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Video Signal Interface (1) (HD66840F30: 30 MHz) (V_{CC} = 5.0 V ± 5 %)

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	33	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

Video Signal Interface (2) (HD66840F25 : 25MHz)

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	40	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

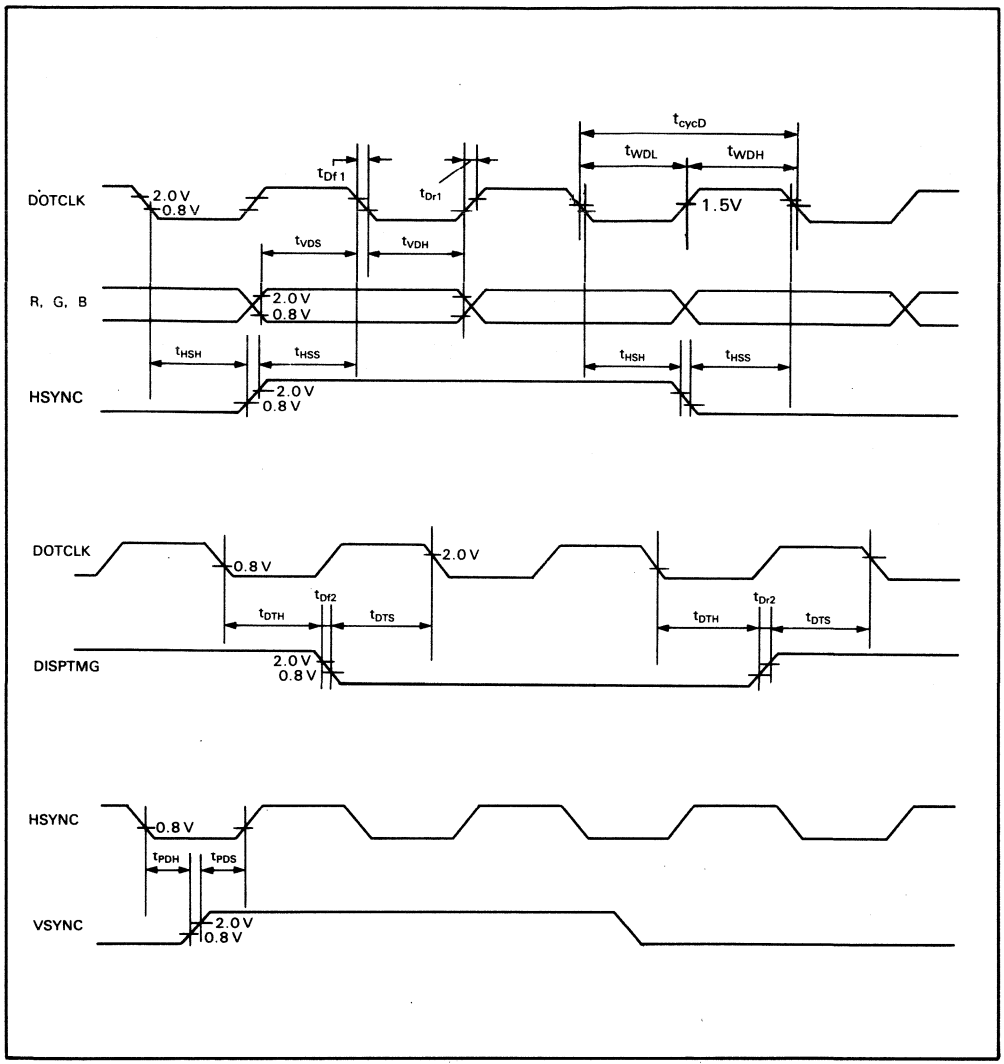


Figure 29. Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	5 t_{CYCD} – 50	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data setup time	t_{SMD}	25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	6 t_{CYCD} – 50	—	ns
Address setup time	t_{AS}	t_{CYCD} – 30	—	ns
Address hold time	t_{WR}	t_{CYCD} – 30	—	ns
Chip select time	t_{CW}	4 t_{CYCD} – 40	—	ns
Write pulse width	t_{WP}	4 t_{CYCD} – 40	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output setup time	T_{SMDW}	2 t_{CYCD} – 25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 33 ns, max 1000 ns).

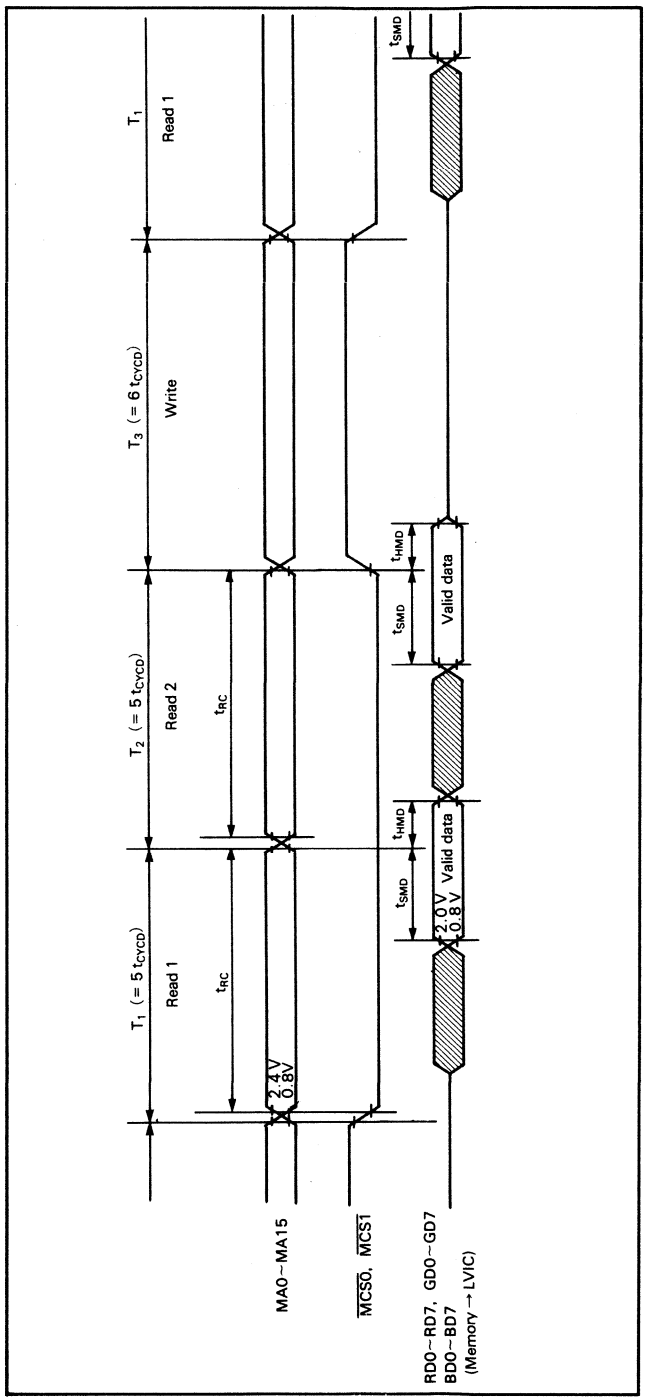


Figure 30. Buffer Memory Interface (RAM Read Timing)

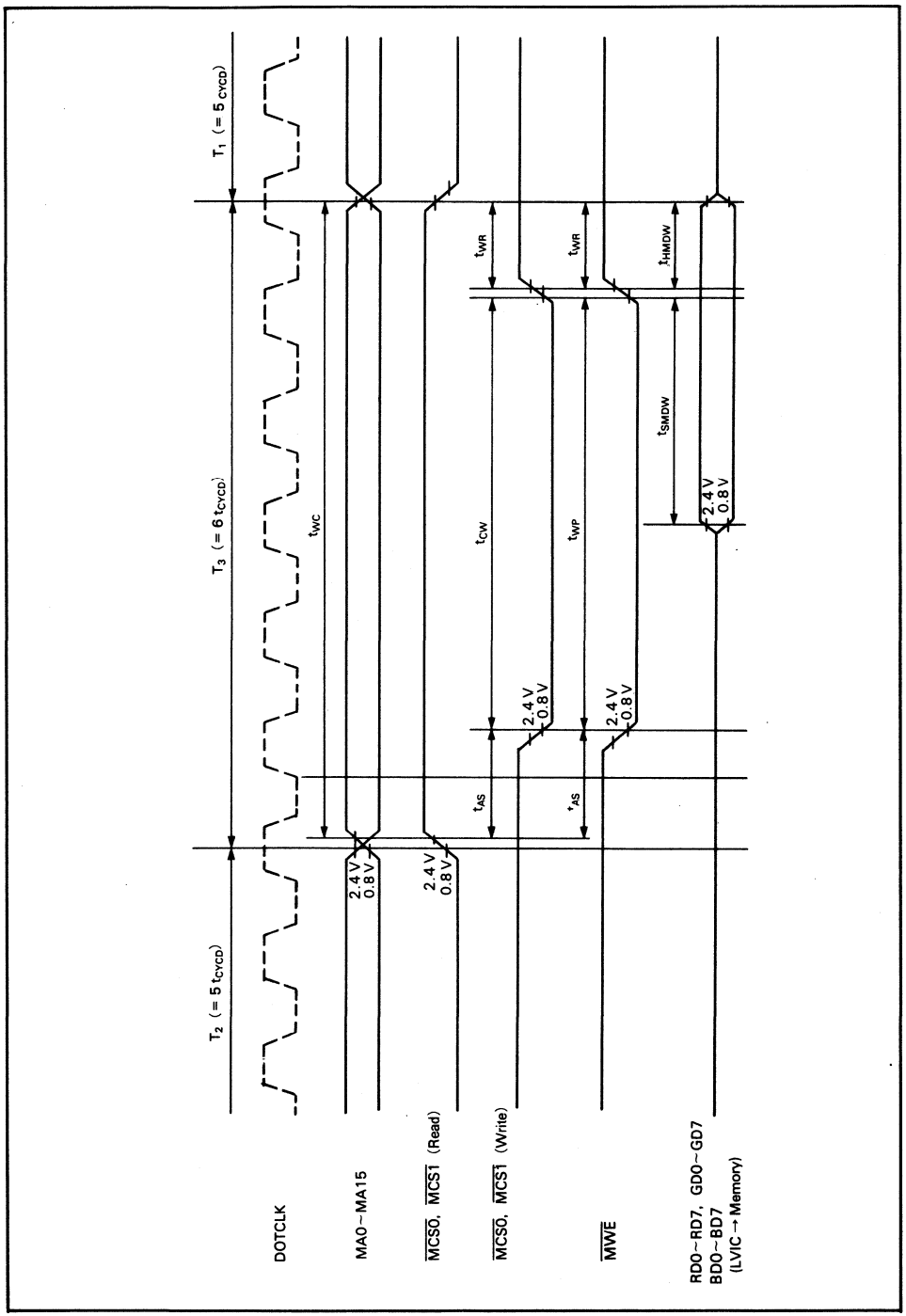


Figure 31. Buffer Memory Interface (RAM Write Timing)

LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t_{WCL2}	166	—	ns
CL2 high-level pulse width	t_{WCL2H}	50	—	ns
CL2 low-level pulse width	t_{WCL2L}	50	—	ns
CL2 rise time	t_{CL2r}	—	30	ns
CL2 fall time	t_{CL2f}	—	30	ns
CL1 high-level pulse width	t_{WCL1H}	200	—	ns
CL1 rise time	t_{CL1r}	—	30	ns
CL1 fall time	t_{CL1f}	—	30	ns
CL1 setup time	t_{SCL1}	500	—	ns
CL1 hold time	t_{HCL1}	200	—	ns
FLM hold time	t_{HF}	200	—	ns
M output delay time	t_{DM}	—	300	ns
Data delay time	t_{DD}	− 20	20	ns
LDOTCK cycle time	t_{WLDOT}	41	—	ns

Note: All the values are measureed at f_{CL2} = 6 MHz.

LCD Driver Interface (TFT-Type LCD Driver)

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X drivers on one side)	t_{TCL2S}	133		ns	Figure 34,35
CL2 high-level width (X drivers on one side)	t_{TCL2HS}	30		ns	
CL2 low-level width (X drivers on one side)	t_{TCL2LS}	30		ns	
CL2 cycle time (X drivers on both side)	t_{TCL2D}	266		ns	
CL2 high-level width (X drivers on both side)	t_{TCL2HD}	80		ns	
CL2 low-level width (X drivers on both side)	t_{TCL2LD}	80		ns	
CL2 rise time	t_{CL2r}		30	ns	
CL2 fall time	t_{CL2f}		30	ns	
CL1 high-level width	t_{TCL1H}	200		ns	
CL1 rise time	t_{CL1r}		30	ns	
CL1 fall time	t_{CL1f}		30	ns	
Data delay time	t_{DD1}	−20	20	ns	
Data set up time	t_{LDS}	15		ns	
Data hold time	t_{LDH}	15		ns	
CL1 setup time	t_{TSCL1}	500		ns	
CL1 hold time	t_{THCL1}	200		ns	
CL3 delay time	t_{DCL3}	50		ns	
M delay time	t_{DM}		300	ns	
FLM hold time	t_{TFH}	200		ns	
LDOTCK cycle time	t_{WLDOT}	33		ns	

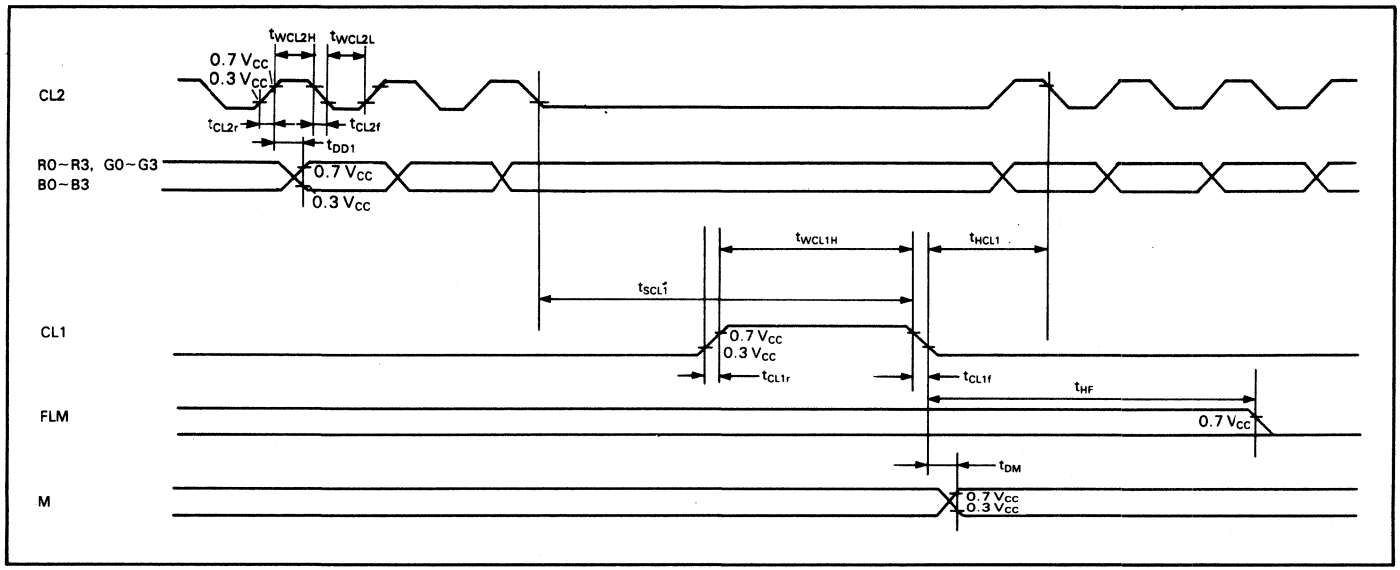


Figure 32. LCD Driver Interface (TN-Type LCD Driver Interface)

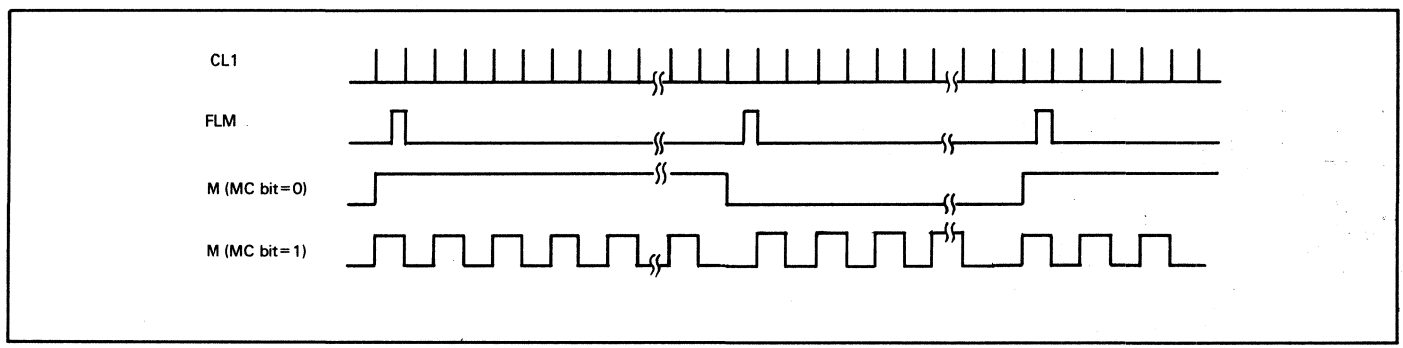


Figure 33. CL1, FLM and M (Reduced View of Figure 32)

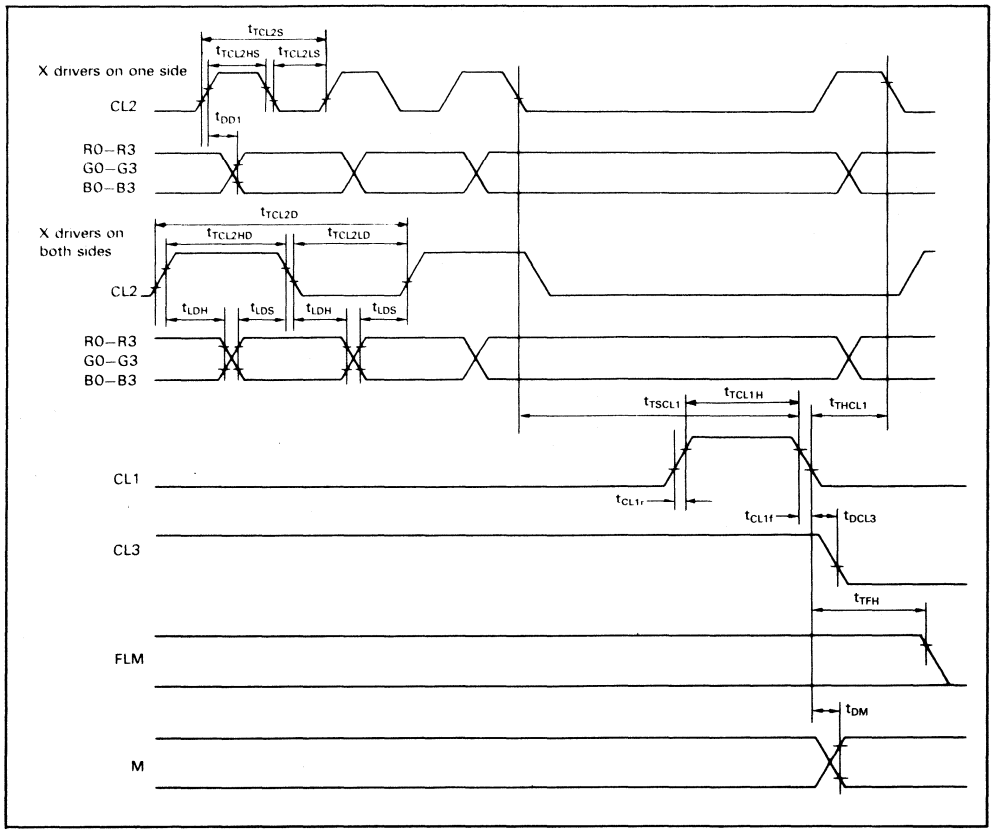


Figure 34. LCD Driver Interface (TFT-type LCD Driver Interface)

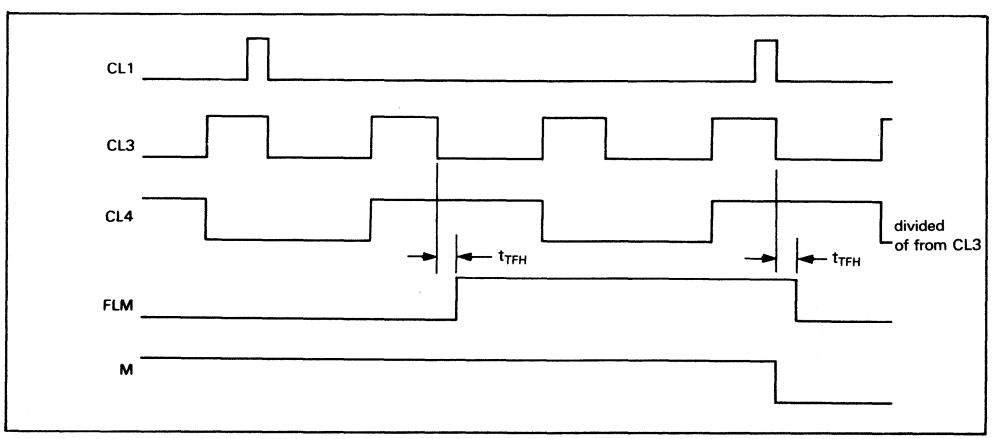


Figure 35. CL1, CL3, CL4, FLM, M (Reduced view of figure 34 at the horizontal stripe mode)

Register Progrmming, MPU Write

Item	Symbol	Min	Max	Unit
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns
$\overline{WE}$ high-level pulse width	t_{WWEH}	190	—	ns
$\overline{WE}$ low-level pulse width	t_{WWEL}	190	—	ns
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns
D0-D3 setup time	t_{DSW}	100	—	ns
D0-D3 hold time	t_{DHW}	0	—	ns
D0-D3 output delay time	t_{DDR}	—	150	ns
D0-D3 output hold time	t_{DHR}	10	—	ns

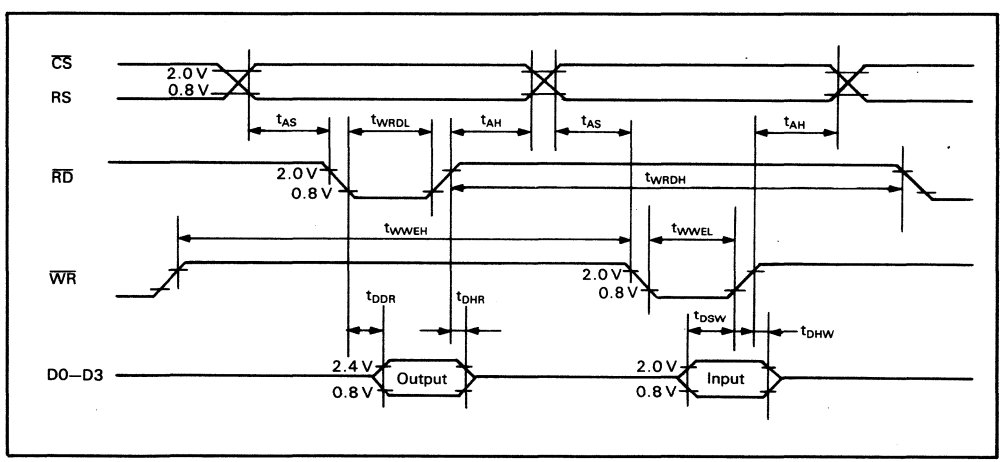


Figure 36. MPU Write Timing

Register Programming, ROM Write

Item	Symbol	Min	Max	Unit
A cycle time	t_{CYCA}	528	—	ns
A rise time	t_{Ar}	—	100	ns
A fall time	t_{Af}	—	100	ns
D ROM data setup time	t_{DSWD}	120	—	ns
D ROM data hold time	t_{DHWD}	0	—	ns

Note: $t_{CYCA} = 16\ t_{CYCD}$

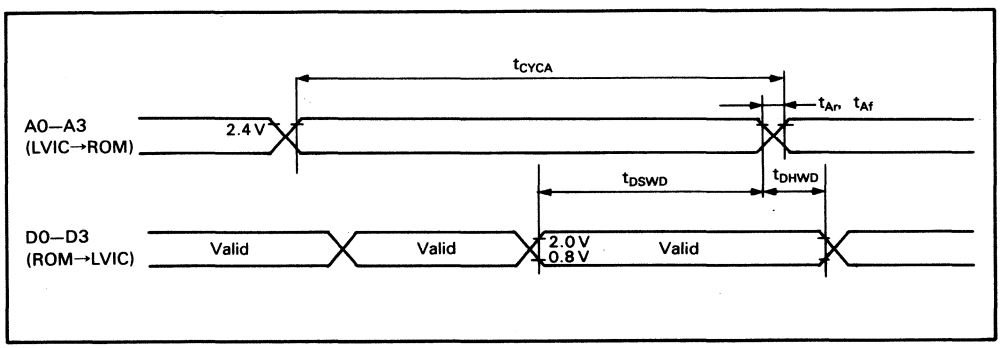


Figure 37. ROM Write Timing

PLL Interface

Item	Symbol	Min	Max	Unit
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns

Reset Input

Item	Symbol	Min	Max	Unit
$\overline{RES}$ input pulse width	$t_{\overline{RES}}$	1	—	μs

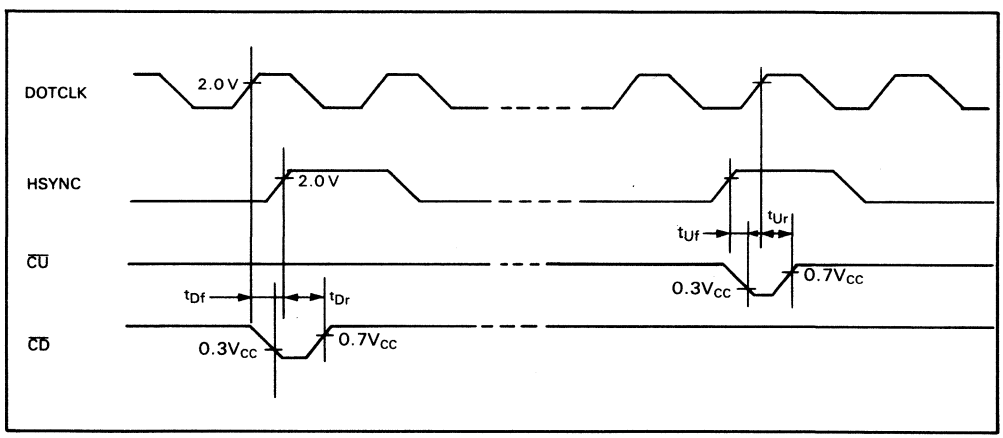


Figure 38. PLL Interface

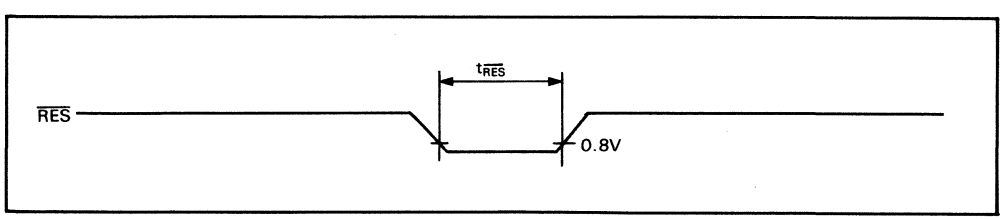


Figure 39. Reset Input

Load Circuits

TTL Load

Pin	R_L	R	C_L	Remarks
MA0-MA15, $\overline{MWE}$, $\overline{MCS0}$,$\overline{MCS1}$, RD0-RD7, GD0-GD7, BD0-BD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/RD/XDOT, A1/YL0-A3/YL2	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pin	C	Remarks
CL1, CL2, CL3, CL4	40 pF	tr, tf: Specified
R0-R3, G0-G3, B0-B3, FLM $\overline{CU}$, $\overline{CD}$	40 pF	tr, tf: Not specified

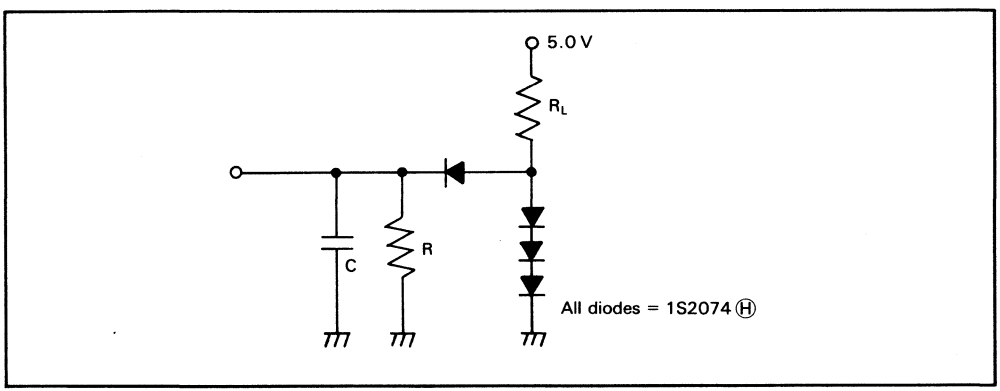


Figure 40. TTL Load Circuit

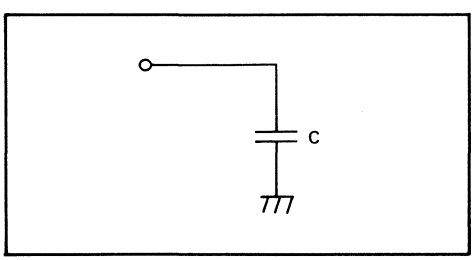


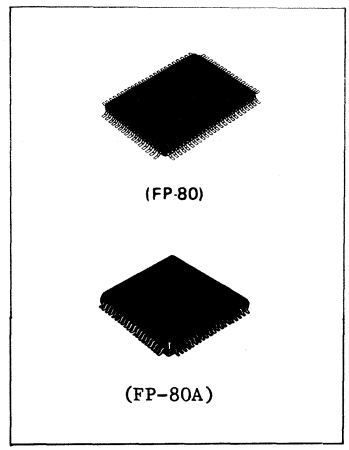
Figure 41. Capacitive Load Circuit

HD61602/HD61603
(Segment Type LCD Driver)

The HD61602 and the HD61603 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microcomputers such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for liquid crystal display driver. By the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.



■ FEATURES

- Wide-range operating voltage

  Operates in a wide range of supply voltage 2.2V to 5.5V.
  Compatible with TTL interface at 4.5V to 5.5V.

- Low current consumption

  Can drive from a battery power supply (100μA max. on 5V).
  Standby input enables a standby operation at lower current consumption (5μA max. on 5V).

- Internal power supply circuit for liquid crystal display driver (HD61602).

  Internal power supply circuit for liquid crystal display driver facilitates the connection to a microcomputer system.

- Versatile segment driving capacity

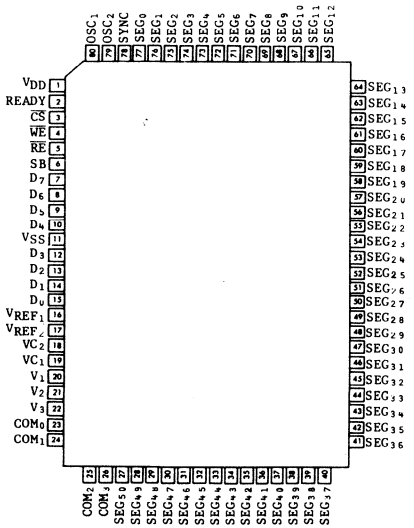
Type No.	Driving method		Display segments	Example of use	Frame freq.(Hz) at fosc=100kHz	Package
HD61602	Static		51	8 segments × 6 digits +3 marks	33	80-pin Plastic QFP (FP-80 FP-80A)
	1/2 bias	1/2 duty	102	8 segments × 12 digits +6 marks	65	
	1/3 bias	1/3 duty	153	9 segments × 17 digits	208	
		1/4 duty	204	8 segments × 25 digits +4 marks	223	
HD61603	Static		64	8 segments × 8 digits	33	80-pin Plastic QFP (FP-80)

■ ORDERING INFORMATION

Type No.	Package
HD61602R	80-pin plastic QFP (FP-80)
HD61602RH	80-pin plastic QFP (FP-80A)
HD61603R	80-pin plastic QFP (FP-80)

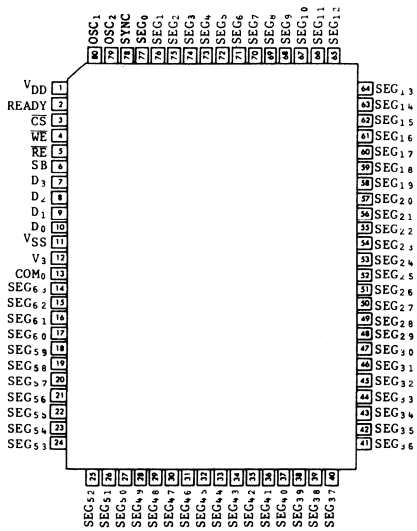
■ PIN ARRANGEMENT (TOP VIEW)

HD61602



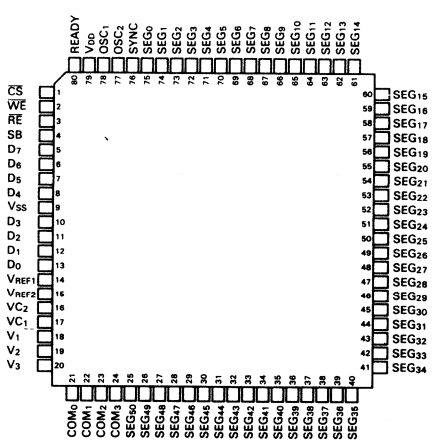
(FP-80)

HD61603



(FP-80)

HD61602



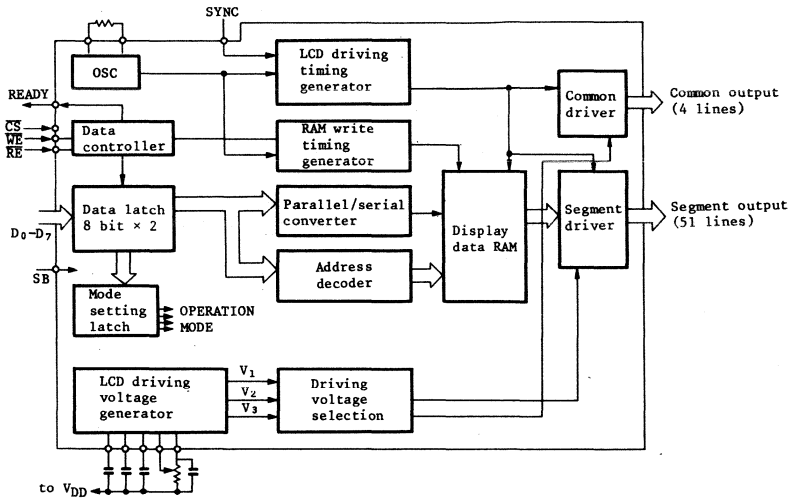
(FP-80A)

(Top View)

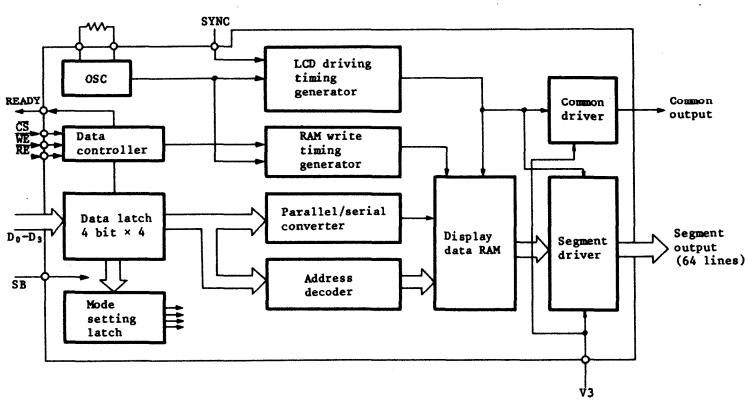
HITACHI

■ BLOCK DIAGRAM

HD61602



● HD61603



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V1, V2, V3	0.3 ∿ +7.0	V
Terminal voltage*	V_T	0.3 ∿ V_{DD} -0.3	V
Operating temperature	Topr	-20 ∿ +75	°C
Storage temperature	Tstg	-55 ∿ +125	°C

* Value referred to V_{SS}=0V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Limit			Unit
		Min.	Typ	Max.	
Power supply voltage	V_{DD}	2.2	-	5.5	V
	V1, V2, V3	0.3	-	$-V_{DD}$ +0.3	V
Terminal voltage*	V_T	0	-	$-V_{DD}$	V
Operating temperature	Topr	-20	-	75	°C

* Value referred to V_{SS}=0V.

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics (1)

(V_{SS}=0V, V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Input "High" voltage	OSC1	V_{IH1}		0.8V_{DD}	-	V_{DD}	V
	Others	V_{IH2}		2.0	-	V_{DD}	V
Input "Low" voltage	OSC1	V_{IL1}		0	-	0.2V_{DD}	V
	Others	V_{IL2}		0	-	0.8	V
Output leakage current	READY	I_{OH}	V_O=V_{DD}	-	-	5	µA
Output "Low" voltage	READY	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V
Input leakage current *1	Input terminal	I_{IL1}	V_{IN}=0∿V_{DD}	-1.0	-	1.0	µA
	V1	I_{IL2}	V_{In}=0∿V3	- 20	-	20	µA
	V2,V3	I_{IL3}		-5.0	-	5.0	µA
LCD driver voltage drop	COM0∿COM3	V_{d1}	±Id=3µA for each COM V3=V_{DD}−3V	-	-	0.3	V
	SEG0∿SEG50	V_{d2}	±Id=3µA for each SEG V3=V_{DD}−3V	-	-	0.6	V
Power supply current		I_{DD}	During display* Rosc=360kΩ	-	-	100	µA
		I_{DD}	At standby	-	-	5	µA
Internal Driving voltage drop	V1,V2,V3	V_{TR}	V_{REF2}=V_{DD}−1V, C_1∿C_4=0.3µF RL=3MΩ	-	-	0.4	V

* Except the transfer operation of display data and bit data.
*1 V1, V2 : applied only to HD61602.

● DC Characteristics (2)

(V_{SS}=0V, V_{DD}=2.2 to 3.8V, Ta=−20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Input "High" voltage		V_{IH}		0.8V_{DD}	-	V_{DD}	V
Input "Low" voltage		V_{IL}		0	-	0.1V_{DD}	V
Output leakage current	READY	I_{OH}	V_{IN}=V_{DD}	-	-	5	µA
Output "Low" voltage	READY	V_{OL}	I_{OL}=0.04mA	-	-	0.1V_{DD}	V
Input leakage current *1	Input terminal	I_{IL1}	V_{IN}=0∿V_{DD}	-1.0	0	1.0	µA
	V1	I_{IL2}	V_{In}=0∿V3	- 20	-	20	µA
	V2,V3	I_{IL3}		-5.0	-	5.0	µA
LCD driver voltage drop	COM0∿COM3	V_{d1}	±Id=3µA for each COM V3=V_{DD}−3V	-	-	0.3	V
	SEG0∿SEG50	V_{d2}	±Id=3µA for each SEG V3=V_{DD}−3V	-	-	0.6	V
Power supply current		I_{SS}	During display* Rosc=330kΩ	-	-	50	µA
		I_{SS}	At standby	-	-	5	µA
Internal Driving voltage drop	V1,V2,V3	V_{TR}	V_{REF2}=V_{DD}−1V, C1∿C4=0.3µF R_L=3MΩ, V_{DD}=3∿3.8V	-	-	0.4	V

* Except the transfer operation of display data and bit data.
*1 V1, V2 : applied only to HD61602.

- AC Characteristics (1)

(V_{SS}=0V, V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Oscillation frequency	OSC2	fosc	R_{osc}=360kΩ	70	100	130	kHz
External clock frequency	OSC1	f_{osc}		70	100	130	kHz
External clock duty	OSC1	Duty		40	50	60	%
I/O signal timing		t_S		400	-	-	ns
		t_H		10	-	-	ns
		t_{WH}		300	-	-	ns
		t_{WL}		400	-	-	ns
		t_{WR}		400	-	-	ns
		t_{DL}	Fig. 5	-	-	1.0	µs
		t_{EN}		400	-	-	ns
		t_{OP1}	For display data transfer	9.5	-	10.5	Clock
		t_{OP2}	For bit and mode data transfer	2.5	-	3.5	Clock
Input signal rise time and fall time		t_r,t_f		-	-	25	ns

- AC Characteristics (2)

(V_{SS}=0V, V_{DD}=2.2 to 3.8V, Ta=−20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Oscillation frequency	OSC2	f_{osc}	R_{osc}=330kΩ	70	100	130	kHz
External clock frequency	OSC1	f_{osc}		70	100	130	kHz
External clock duty	OSC1	Duty		40	50	60	%
I/O signal timing (V_{DD}=3.0∿3.8V)		t_S		1.5	-	-	µs
		t_H		1.0	-	-	µs
		t_{WH}		1.5	-	-	µs
		t_{WL}		1.5	-	-	µs
		t_{DL}	Fig. 6	-	-	2.0	µs
		t_{WR}		1.5	-	-	µs
		t_{EN}		2.0	-	-	µs
		t_{OP1}	For display data transfer	9.5	-	10.5	Clock
		t_{OP2}	For bit and mode data transfer	2.5	-	3.5	Clock
Input signal rise time and fall time		tr, tf		-	-	25	ns

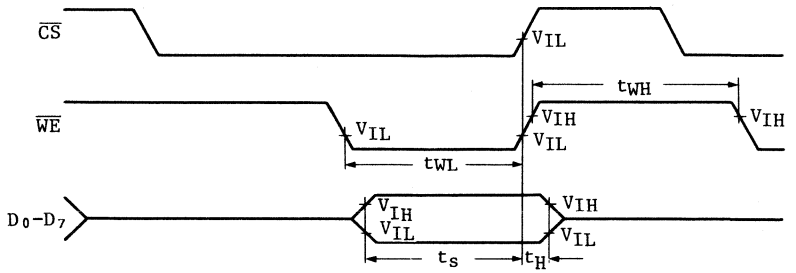


Fig. 1 Write Timing
($\overline{RE}$ is fixed on "High" level, and SYNC on "Low" level)

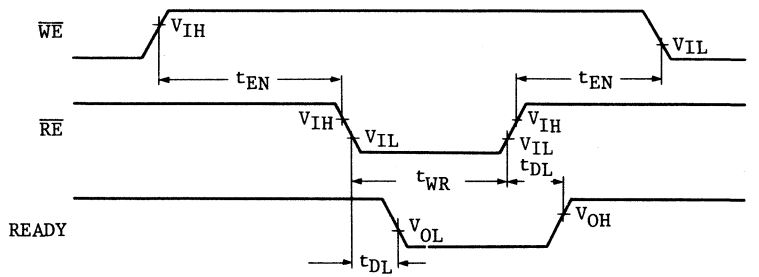


Fig. 2 Reset/Read Timing
($\overline{CS}$ and SYNC are fixed on "Low" level)

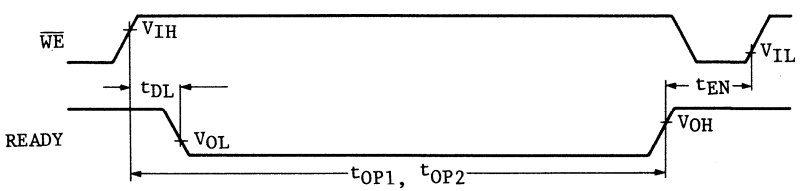


Fig. 3 READY Timing
(When the READY output is always available)

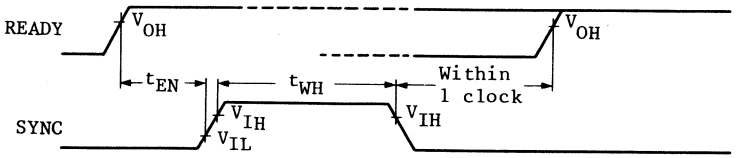


Fig. 4 SYNC Timing

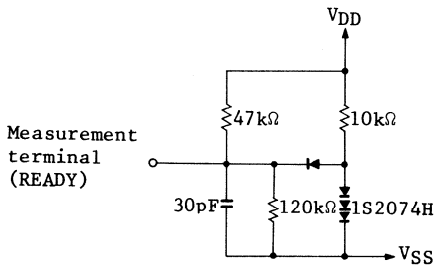


Fig. 5 Bus Timing Load Circuit (LS-TTL Load)

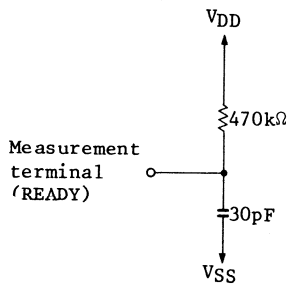


Fig. 6 Bus Timing Load Circuit (CMOS Load)

■ TERMINAL FUNCTIONS

• HD61602 Terminal Functions

Terminal name	No. of lines	Input/output	Connected to	Function
V_{DD}	1	Power supply		⊕ -side power supply
READY	1	NMOS open drain output	MCU	During setting data in the display data RAM and mode setting latch in the LSI after data transfer, "Low" is output to the READY terminal to inhibit the next data input. There are two types of modes: one in which "Low" is output only when both of $\overline{CS}$ and $\overline{RE}$ are "Low", and the other in which "Low" is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is "Low".
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are "Low", the first data is recognized as the 1st byte data.
SB	1	Input	MCU	"High" level input stops the LSI operations. (i) Stops oscillation and clock input. (ii) Stops LCD driver. (iii) Stops writing data into display RAM.
D0∿D7	8	Input	MCU	Data input terminal from where 8-bit × 2-byte data are input.
V_{SS}	1	Power supply		⊖ -side power supply
V_{REF1}	1	Output	External R	Reference voltage output. LCD driving voltage is generated by this voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2}=V1$
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}:

Terminal name	No. of lines	Input/output	Connected to	Function
V1, V2, V3	3	Output (Input)	External C	LCD driving voltages are output. An external C is connected to each terminal.
COM0∿COM3	4	Output	LCD	LCD common (backplate) driving output.
SEG0∿SEG50	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips application. LCD driver timing circuit is reset by "High" input. LCD is off.
OSC1 OSC2	2	Input Output	External R	Attaches external R to these terminals for oscillation. An external clock (100kHz) can be input from OSC1.

Note: Logic polarity is positive. "1"="H"=active.

o HD61603 Terminal Functions

Terminal name	No. of lines	Input/output	Connected to	Function
V_{DD}	1	Power supply		⊕ -side power supply
READY	1	NMOS open drain output	MCU	During setting data in the display data RAM and mode setting latch in the LSI after data transfer, "Low" is output to the READY terminal to inhibit the next data input. There are two types of modes: one in which "Low" is output only when both of $\overline{CS}$ and $\overline{RE}$ are "Low", and the other in which "Low" is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is "Low".
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D3 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Reset the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are "Low", the first data is recognized as the 1st byte data.

Terminal name	No. of lines	Input/output	Connected to	Function
SB	1	Input	MCU	"High" level input stops the LSI operations. (i) Stops oscillation and clock input. (ii) Stops LCD driver. (iii) Stops writing data into display RAM.
D0∿D3	4	Input	MCU	Data input terminal from where 4-bit X4 data are input.
V_{SS}	1	Power supply		⊖ -side power supply
V3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V3 is used as driving voltage.
COMO	1	Output	LCD	LCD common (backplate) driving output.
SEC0∿SEG63	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips application. LCD driver timing circuit is reset by "High" input. LCD is off.
OSC1 OSC2	2	Input Output	External R	Attaches external R to these terminals for oscillation. An external clock (100kHz) can be input from OSC1.

Note: Logic polarity is positive. "1"="H"=active.

■ DISPLAY RAM

< HD61602 Display RAM >

The HD61602 has an internal display RAM shown in Fig. 7. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to the 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

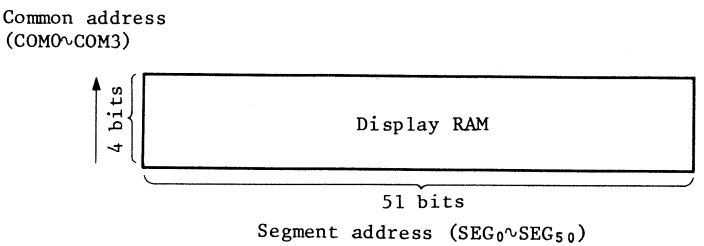


Fig. 7 Display RAM

- Reading Data from Display RAM

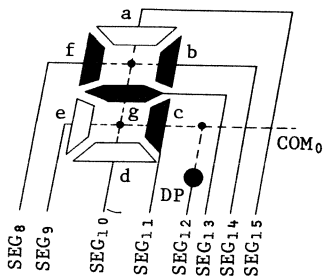
A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.
A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

(1) Static drive

In the static drive, only the column of COM0 of display RAM is output. COM1 to COM3 are not displayed.

LCD connection

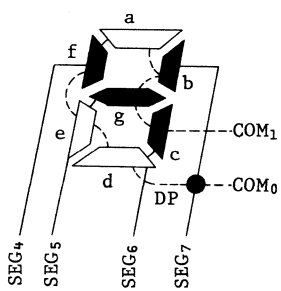


Display RAM

COM_3									
COM_2									
COM_1									
COM_0	f	e	d	c	DP	g	b	a	
	SEG_8	SEG_9	SEG_{10}	SEG_{11}	SEG_{12}	SEG_{13}	SEG_{14}	SEG_{15}	

(2) 1/2 duty drive

LCD connection



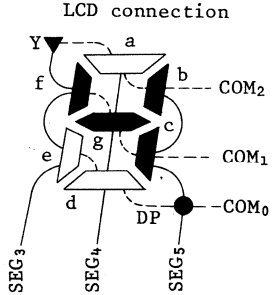
Display RAM

COM_3							
COM_2							
COM_1	a	g	c	b			
COM_0	f	e	d	DP			
	SEG_4	SEG_5	SEG_6	SEG_7	SEG_8	SEG_9	

In the 1/2 duty drive, the columns of COM0 and COM1 of display RAM are output in time sharing. The columns of COM2 and COM3 are not displayed.

(3) 1/3 duty drive

LCD connection



Display RAM

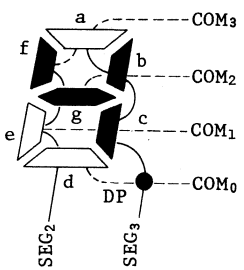
COM_3					
COM_2	Y	a	b		
COM_1	f	g	c		
COM_0	e	d	DP		
	SEG_3	SEG_4	SEG_5	SEG_6	

In the 1/3 duty drive, the columns of COM0 to COM2 are output in time sharing. No column of COM3 is displayed.

"Y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "Y".

(4) 1/4 duty drive

LCD connection



Display RAM

COM_3	f	a		
COM_2	g	b		
COM_1	e	c		
COM_0	d	DP		
	SEG_2	SEG_3	SEG_4	

In the 1/4 duty drive, all the columns of COM0 to COM3 are displayed.

- Writing Data into Display RAM

Data is written into the display RAM in the following five methods:

(1) Bit manipulation
Data is written into any bit of RAM on a bit basis.

(2) Static display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

(3) 1/2 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty drive.

(4) 1/3 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty drive.

(5) 1/4 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the driving methods as described in the selection of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty driving methods. The digits are allocated as shown Fig. 8 (allocation of digit). As the data can be transferred on a digit basis from a microcomputer, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Fig. 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Fig. 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty, or Ad25 of 1/4 duty, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

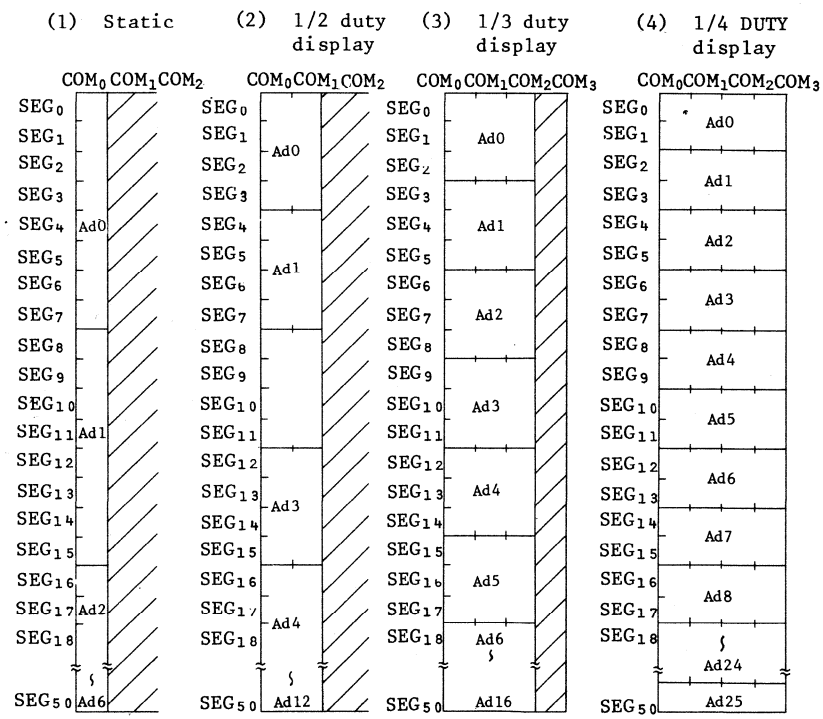


Fig. 8 Allocation of Digit (HD61602)

(1) Static display

	COM_0
SEG_8	Bit 7
SEG_{8n+1}	6
SEG_{8n+2}	5
SEG_{8n+3}	4
SEG_{8n+4}	3
SEG_{8n+5}	2
SEG_{8n+6}	1
SEG_{8n+7}	Bit 0

(2) 1/2 duty display

	COM_0	COM_1
SEG_{4n}	Bit 7	6
SEG_{4n+1}	5	4
SEG_{4n+2}	3	2
SEG_{4n+3}	1	Bit 0

(3) 1/3 duty display

	COM_0	COM_1	COM_2
SEG_{3n}	Bit 7	6	
SEG_{3n+1}	5	4	3
SEG_{3n+2}	2	1	Bit 0

(4) 1/4 duty display

	COM_0	COM_1	COM_2	COM_3
SEG_{2n}	Bit 7	6	5	4
SEG_{2n+1}	3	2	1	Bit 0

Fig. 9 Bit Assignment in an Adn (HD61602)

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

< HD61603 Display RAM >

The HD61603 has an internal display RAM as shown in Fig. 10. Display data is stored in the RAM and output to the segment output terminal.

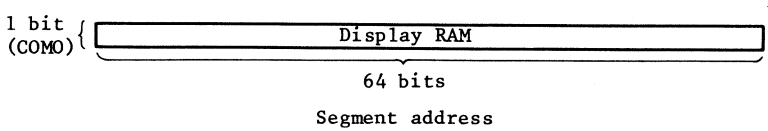


Fig. 10 Display RAM (HD61603)

- Reading Data from Display RAM

Each bit of the display RAM corresponds to each LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Fig. 11 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

LCD connection

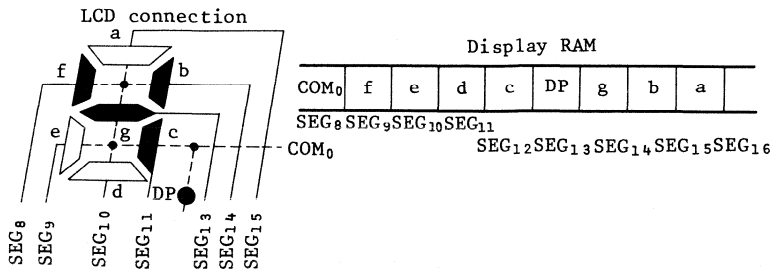


Fig. 11 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

- Writing Data into Display RAM

Data is written into the display RAM in the following two methods:

(1) Bit manipulation
Data is written into any bit of RAM on a bit basis.

(2) Static display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in Fig. 12. When data is transferred from a microcomputer, four 4 bit data are needed to specify the digit address and an 8-bit display data. Fig. 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

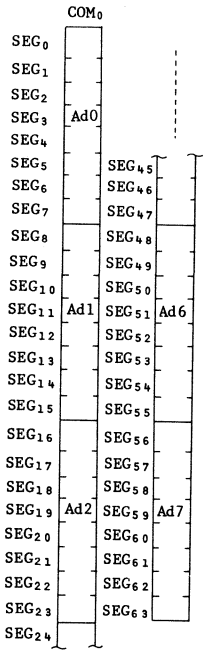


Fig. 12 Allocation of Digit (HD61603)

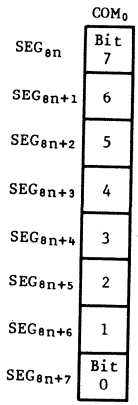


Fig. 13 Bit Assignment in an Adn (HD61603)

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

Operating Modes

< HD61602 Operating Modes >

The HD61602 has the following operating modes:

(1) LCD drive mode

Determines the LCD driving method.

(a) Static drive mode

LCD is driven statically.

(b) 1/2 duty drive mode
LCD is driven at 1/2 duty and 1/2 bias.

(c) 1/3 duty drive mode
LCD is driven at 1/3 duty and 1/3 bias.

(d) 1/4 duty drive mode
LCD is driven at 1/4 duty and 1/3 bias.

(2) Data display mode

Determines how to write display data into the data RAM.

(a) Static display mode
8-bit data is written into the display RAM according to the digit in the static drive.

(b) 1/2 duty display mode
8-bit data is written into the display RAM according to the digit in the 1/2 duty drive.

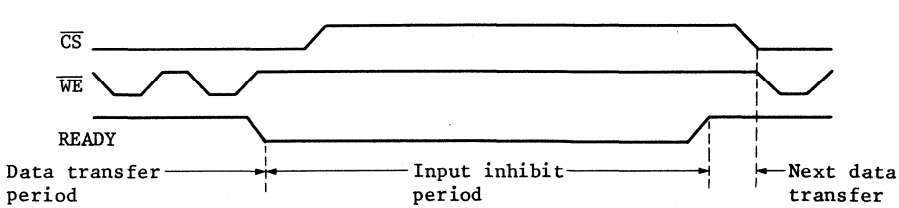
(c) 1/3 duty display mode
8-bit data is written into the display RAM according to the digit in the 1/3 duty drive.

(d) 1/4 duty display mode
8-bit data is written into the display RAM according to the digit in the 1/4 duty display drive.

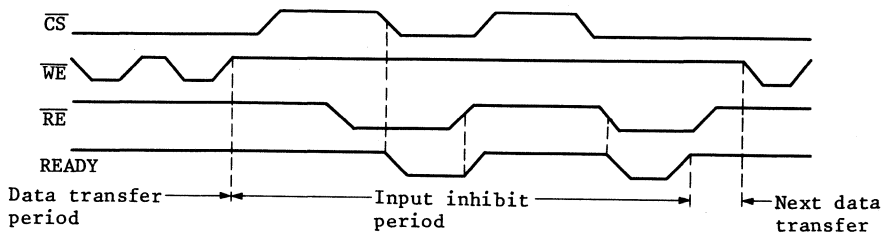
(3) READY output mode

Determines the READY output timing.
After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

(a) READY is always available.



(b) READY is available by $\overline{CS}$ and $\overline{RE}$.



(4) LCD OFF mode

In this mode, the HD61602 stops driving LCD and turns it off.

(5) External driving voltage mode

A mode for using external driving voltage (V1, V2 and V3).

The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

< HD61603 Operating Modes >

The HD61603 has the following modes:

(1) READY output mode

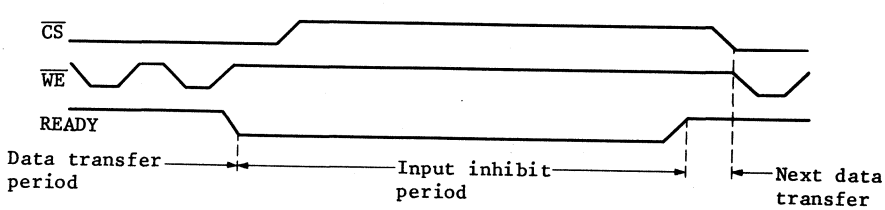
Determines READY output timing.

After data set is transferred, the data is processed internally.

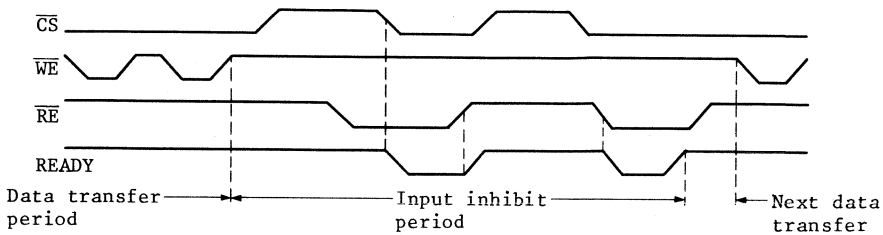
The next data cannot be acknowledged during the processing period.

The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

(a) READY is always available.



(b) READY is available by $\overline{CS}$ and $\overline{RE}$.



(2) LCD OFF mode

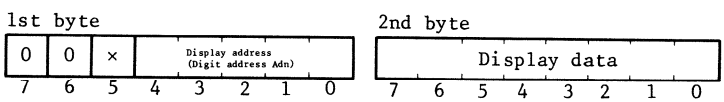
In this mode, the HD61603 stops driving LCD and turns it off.

INPUT DATA FORMATS

HD61602 Input Data Formats

Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output is changed from "Low" to "High" or "Low" pulse is entered into $\overline{RE}$ terminal.

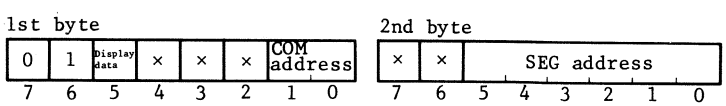
(1) Display data (Updates display on an 8-segment basis.)



(i) Display address: Digit address Adn in accordance with each display mode.

(ii) Display data : Pattern data that is written into the display RAM according to each display mode and the address.

(2) Bit manipulation data (Updates display on a segment basis.)

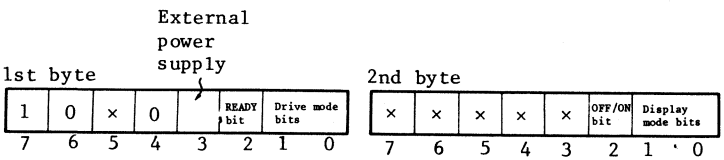


(i) Display data : Data that is written into 1 bit of the specified display RAM.

(ii) COM address : Common address of display RAM.

(iii) SEG address : Segment address of display RAM

(3) Mode setting data



(i) Display mode bits : 00; Static display mode
01; 1/2 duty display mode
10; 1/3 duty display mode
11; 1/4 duty display mode

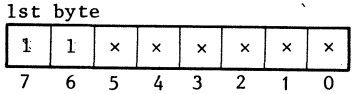
(ii) OFF/ON bit : 1; LCD OFF (It is set to "1" when SYNC is entered.)
0; LCD ON

(iii) Drive mode bits : 00; Static drive
01; 1/2 duty drive
10; 1/3 duty drive
11; 1/4 duty drive

(iv) READY bit : 0; READY outputs "0" only while $\overline{CS}$ and $\overline{RE}$ is "0". (It is reset to "0" when SYNC is entered.) ..... READY bus mode
1; READY outputs "0" regardless of $\overline{CS}$ and $\overline{RE}$. ..... READY port mode

(v) External power supply bit : 0; Driving voltage is generated internally.
1; Driving voltage is supplied from external. (It is set to "1" when SYNC is entered.)

(4) 1-byte instruction

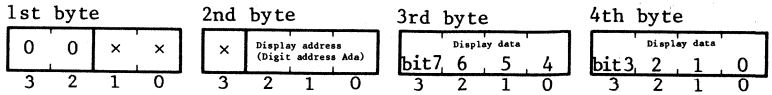


The first data (first byte) is ignored when the bit 6 and bit 7 in the byte are "1".

< HD61603 Input Data Formats >

Input data is composed of 4 bits × 4. Input them as four 4 bit data after READY output is changed from "Low" to "High" or "Low" pulse is entered into $\overline{RE}$ terminal.

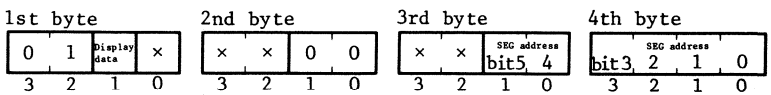
(1) Display data (Updates display on an 8-segment basis.)



(i) Display address: Digit address Adn shown in Fig. 12.

(ii) Display data : Pattern data that is written into the display RAM as shown in Fig. 13.

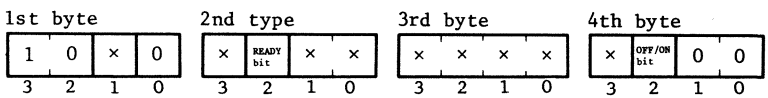
(2) Bit manipulation data (Updates display on a segment basis.)



(i) Display data : Data that is written into the 1 bit of the specified display RAM.

(ii) SEG address : Segment address of display RAM (segment output).

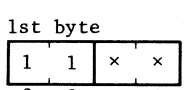
(3) Mode setting data



(i) OFF/ON bit : 1; LCD OFF (It is set to "1" when SYNC is entered.)
0; LCD ON

(ii) READY bit : 0; READY outputs "0" only while $\overline{CS}$ and $\overline{RE}$ are "0". (It is reset to "0" when SYNC is entered).
..... READY bus mode
1; READY outputs "0" regardless of $\overline{CS}$ and $\overline{RE}$.
..... READY port mode

(4) 1-byte instruction



The first data (4 bits) is ignored when the bit 3 and 2 in the data are "1".

■ HOW TO INPUT DATA

< How to Input HD61602 Data >

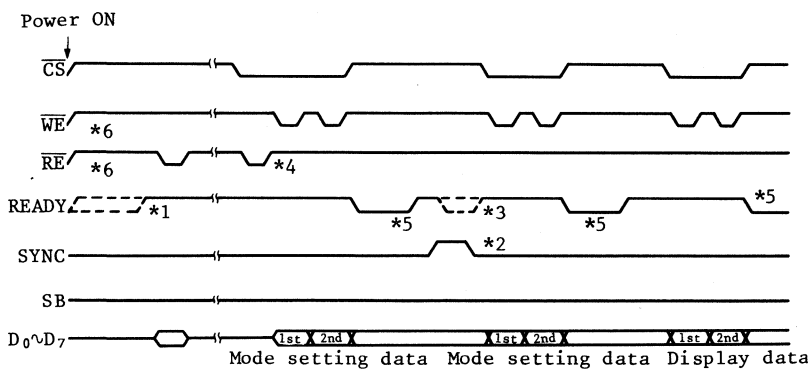
Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted. Because the first 8-bit data is distinguished from the second one depending on the sequence only.

If data transfer is interrupted or at the power ON the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

(1) Set $\overline{CS}$ and $\overline{RE}$ inputs in "Low" (no display data changes).

(2) Input 2 or more "1-byte instruction data" which bit 7 and 6 are "1" (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, DO to D7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and Fig. 14.



*1: READY output is indefinite during 12 clocks after the oscillation start when power ON (clock: OSC_2 clock).

*2: "High" pulse should be applied to SYNC terminal when using two or more chips synchronously.

*3: In the mode in which READY is always available, READY output is indefinite while "High" is being applied to SYNC.

*4: Reset the byte counter after power ON.

*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.

*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.

*7: It is not always necessary to follow this example.

Fig. 14 Example of Data Transfer Sequence

< How to Input HD61603 Data >

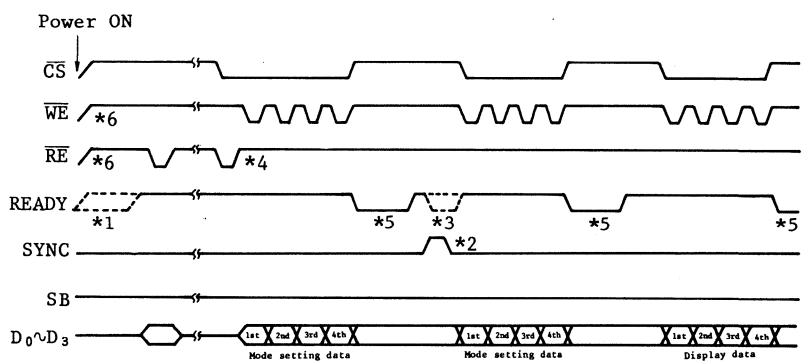
Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted. Because the first 4-bit data to the fourth 4-bit data are distinguished from each other depending on the sequence only.

If data transfer is interrupted or at the Power ON, the following two methods can be used to reset the count of the number of data (count of the first 4 bit data to the fourth 4-bit data):

(1) Set $\overline{CS}$ and $\overline{RE}$ in "Low".

(2) Input 4 or more "1-byte instruction" data (4-bit data) which bit 3 and 2 are "1" (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, DO to D3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and Fig. 15.



*1: READY output is indefinite during 12 clocks after the oscillation start when power ON (clock: OSC_2 clock).

*2: "High" pulse should be applied to SYNC terminal when using two or more chips synchronously.

*3: In the mode in which READY is always available, READY output is indefinite while "High" is being applied to SYNC.

*4: Reset the 4-bit data counter after power ON.

*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.

*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.

*7: It is not always necessary to follow this example.

Fig. 15 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes.

(1)READY bus mode (READY bit = 0)

(2)READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose REDAY bus mode, (1) a will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61602 and HD61603.

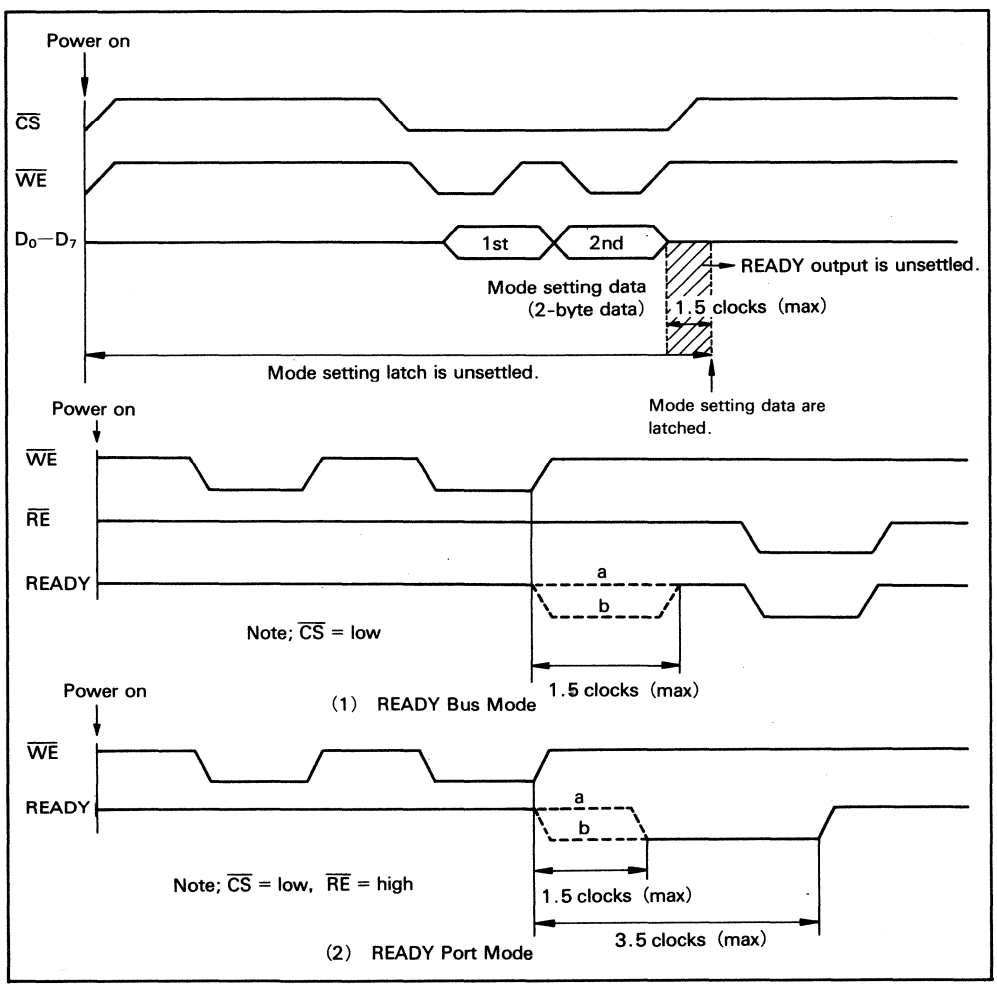


Figure 16. READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows.

(a) LCD driver is stopped (LCD is off)
(b) Display data and operating mode are held.
(c) The operation is suspended while changing display (= while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
(d) Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi-Chip Operation

When an LCD is driven with two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input causes the change of the mode setting data (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used. connect pin SYNC to V_{SS}.

In the case SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geqq$ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61602)

What is LCD Voltage?

HD61602 drives liquid crystal display using four levels of voltages; V_{DD}, V_1, V_2 and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to liquid crystal displays. V_3 always needs to be supplied power regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61602.

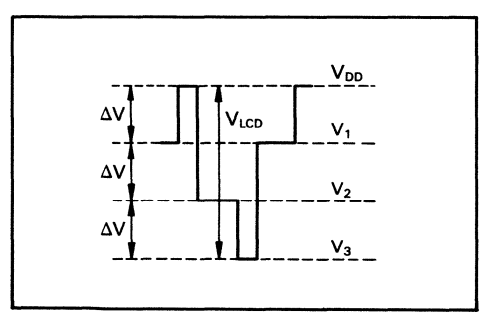


Figure 17. LCD Output Waveform and Output Levels

When internal drive power supply is used.

When the internal drive power supply is used, attach C_1-C_4 for charge pump circuits and variable resistance R_1 for deciding display drive voltage to HD61602 as shown in figure 18.
Internal voltage is available by setting external voltage switching bits of mode setting data "0".

Figure 19 shows voltage characteristics between V_{DD} and V_{REF1}.
Voltage is divided at R_1, and then into V_{REF2}. Voltage between V_{DD} and V_{REF2} is equivalent to ΔV in figure 19, and so V_{LCD} can be change by regulating the voltage.

V_{REF2} is usually regurlated by variable reistance, but in case of replacing R_1 with two invariable resistance take V_{REF1} between max and min into consideration as shown in figure 19.

Internal drive power supply is genarated by using capacity, and so much current cannot be streamed. When large liquid crystal display panel is used, examine the external drive power supply.

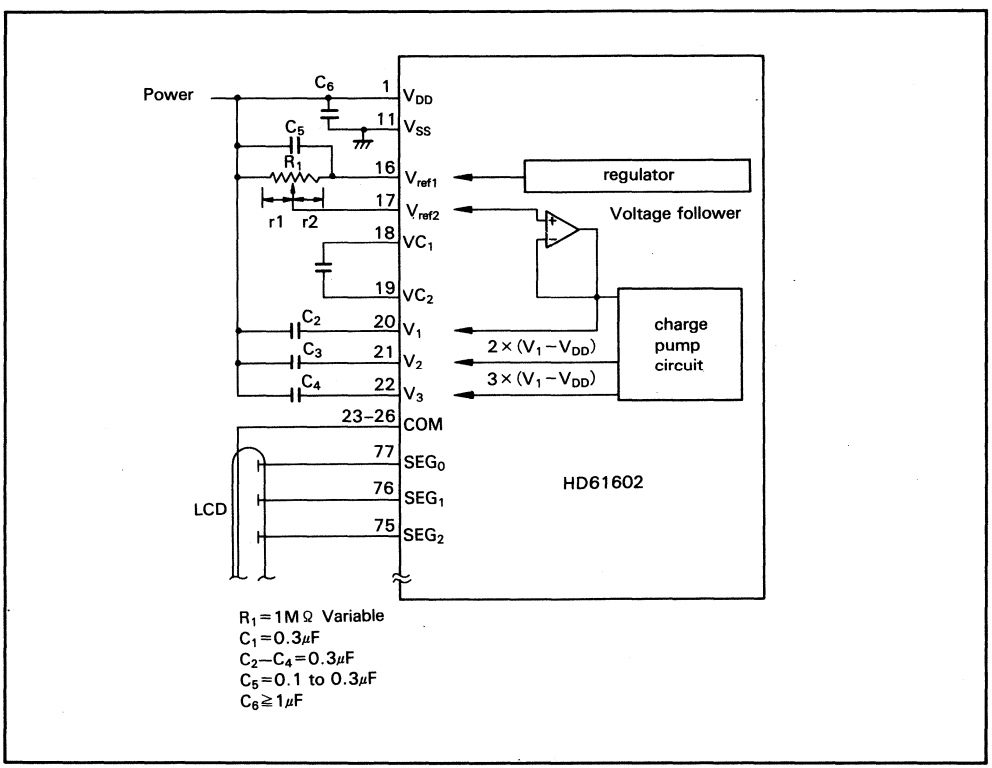


Figure 18. Example

When external drive power supply is used.

External power supply can be used by setting external voltage switching bits of mode setting data "1". When large liquid crystal display panel is used, in case of multi chip, on in need of accurate liquid crystal drive voltage, used the external power supply.

R_2-R_5 is connected in series between V_{DD} and V_{SS}, and by these resistance ratio each voltage of ΔV and V_{LCD} is generated and then supplied to V_1, V_2 and V_3. C_2-C_4 are capacities for smoothing.

When regulating shining degree, change the resistance value by setting R_5 variable resistance.

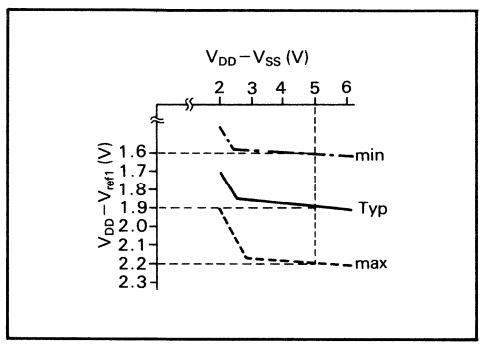
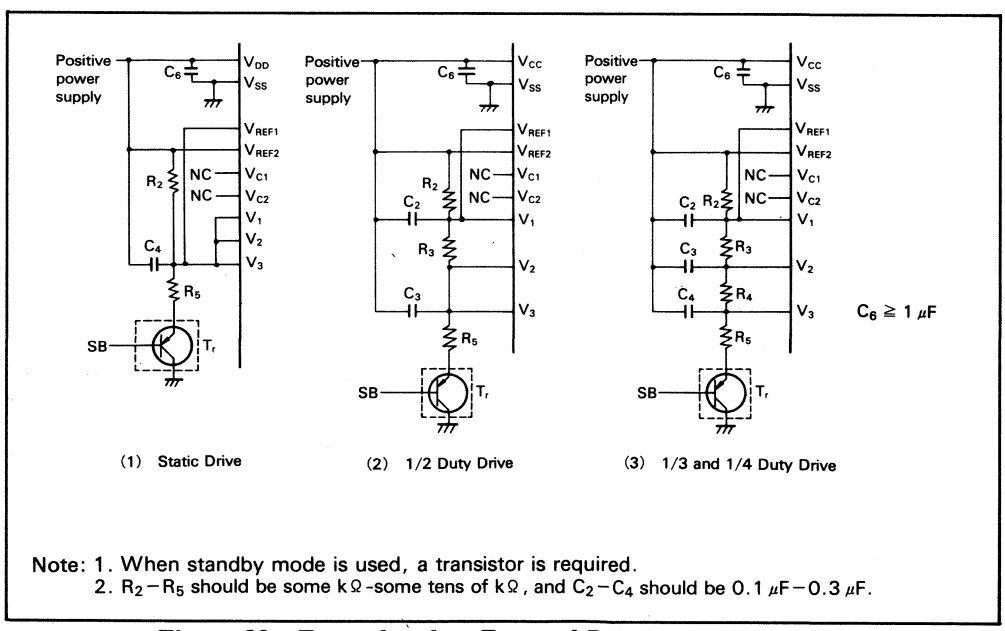


Figure 19. Voltage characteristics between V_{DD} and V_{ref1}



Note: 1. When standby mode is used, a transistor is required.
2. R_2-R_5 should be some kΩ-some tens of kΩ, and C_2-C_4 should be 0.1 μF−0.3 μF.

Figure 20. Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61603)

As shown in figure 21 apply LCD drive voltage from the external power supply.

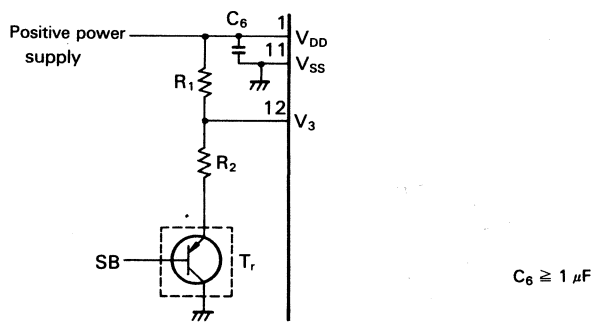
Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation cirucit is used, attach an external resistor R_{OSC} as shown in figure 22. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.



Note: When standby mode is used, a transistor is required.

Figure 21. Example of Drive Voltage Generator

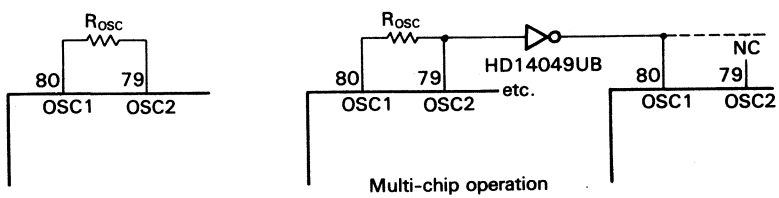


Figure 22. Example of Oscillation Circuit

Applications

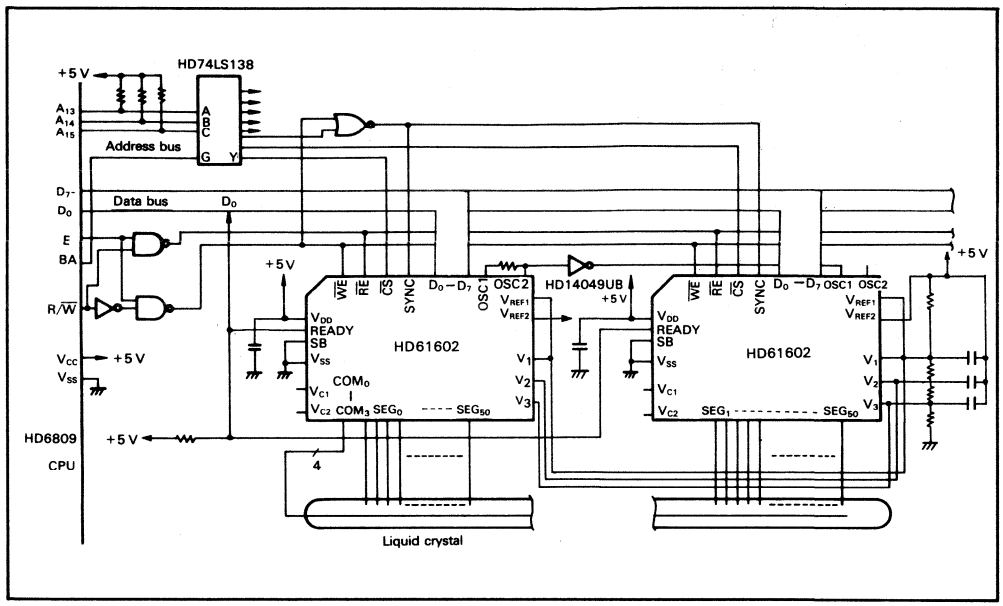


Figure 23. Example (1)

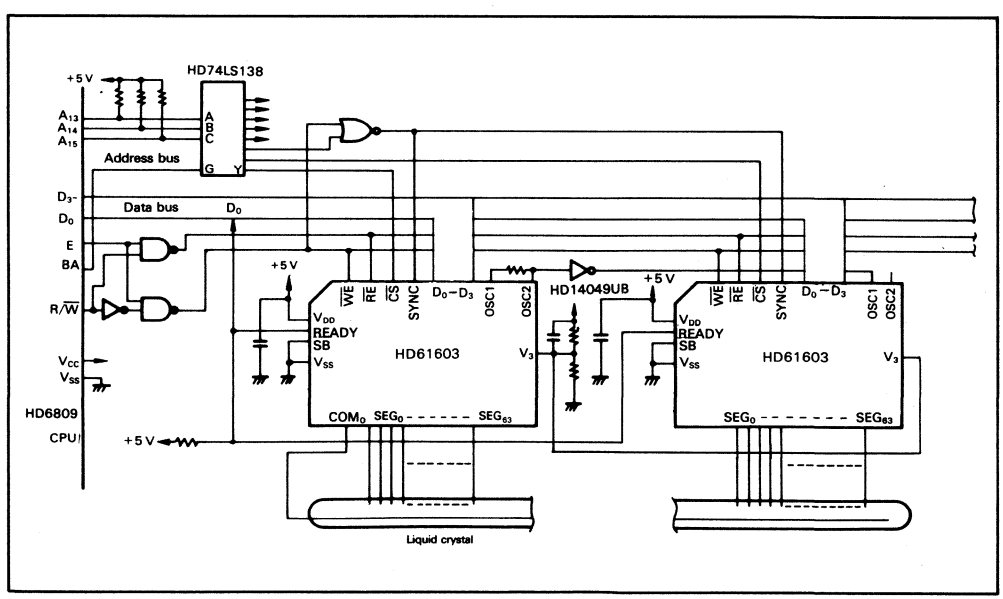


Figure 24. Example (2)

HD61604/HD61605
(Segment Type LCD Driver)

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microcomputers such as the HMCS6800 series.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal dispay drive method.

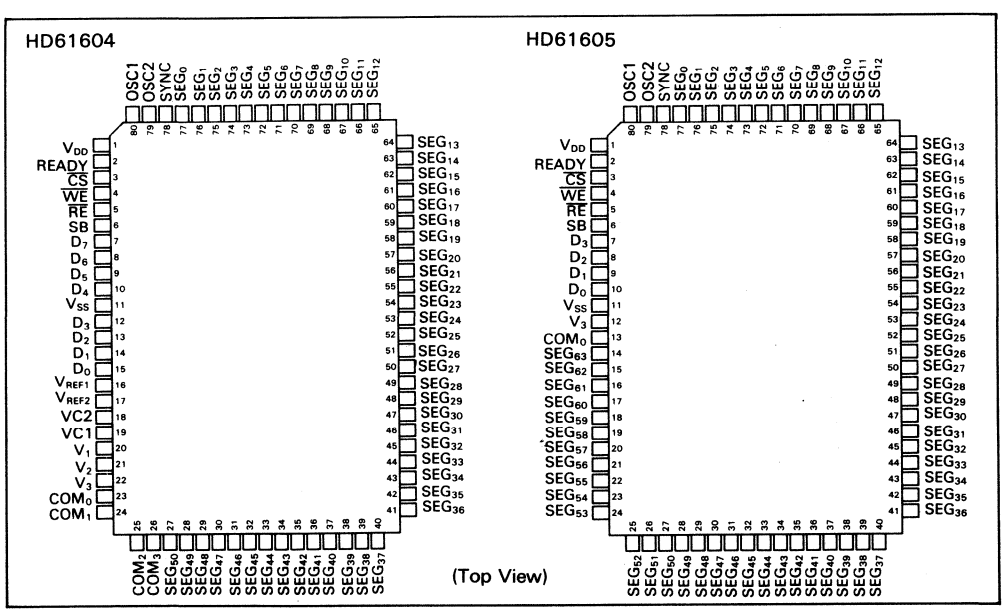
The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  —Can drive from a battery power supply (100 μA max on 5 V).
  —Standby input enables a standby operation at lower current consumption (5 μA max on 5 V).
- Versatile segment drive capacity

Type No.	Drive Method		Display Segments	Example of Use	Frame Freq (Hz) at fosc=100 kHz
HD61604	Static		51	8 segments × 6 digits + 3 marks	98
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	195
	1/3 bias	1/3 duty	153	9 segments × 17 digits	521
		1/4 duty	204	8 segments × 25 digits + 4 marks	781
HD61605	Static		64	8 segments × 8 digits	98

Pin Arrangement



Block Diagram

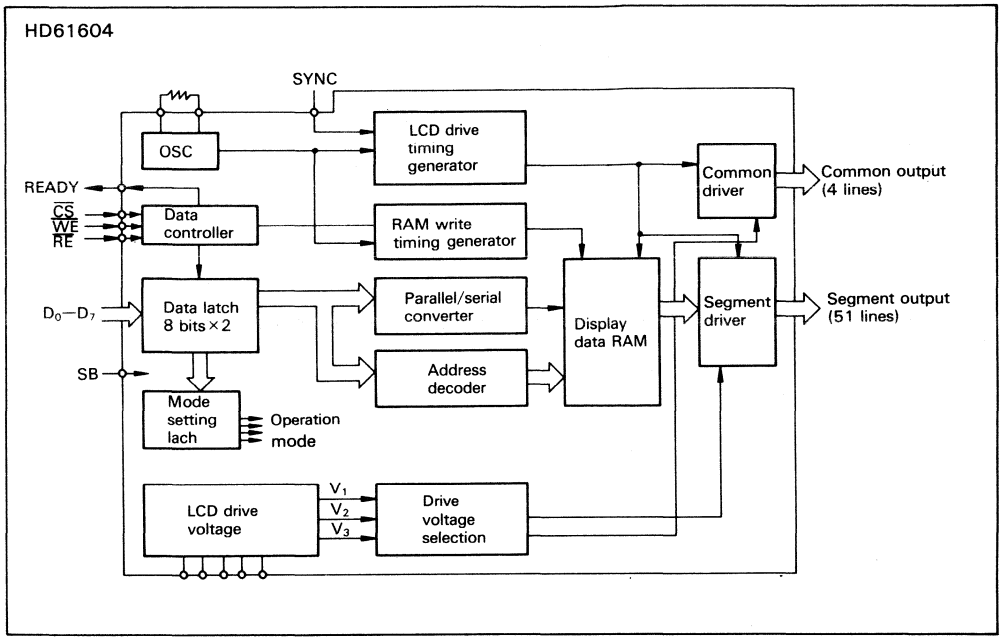


Figure 1. HD61604 Block Diagram

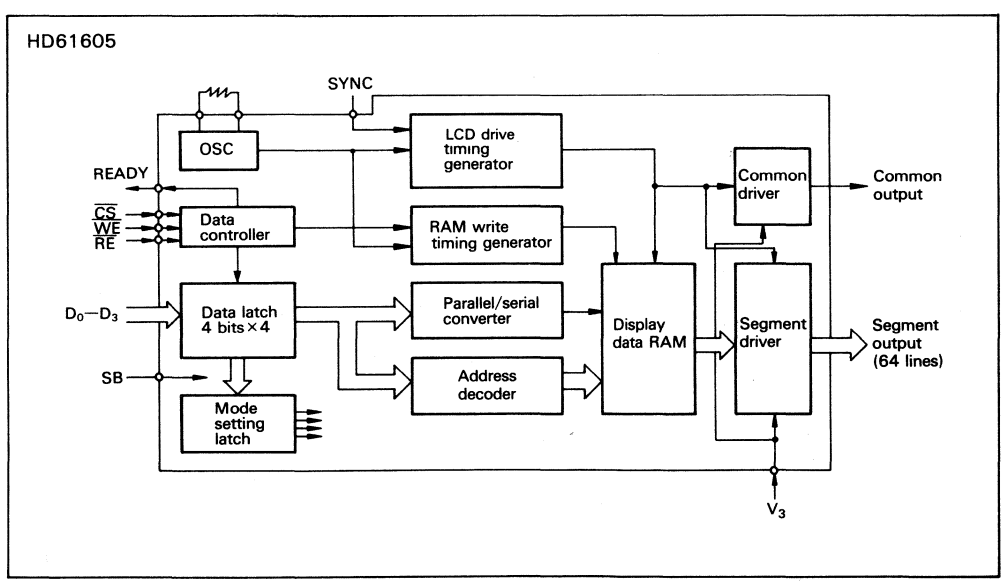


Figure 2. HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During setting data in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two types of modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_7 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

(i) Stops oscillation and clock input.
(ii) Stops LCD driver.
(iii) Stops writing data into display RAM.

D_0-D_7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0-COM_3 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{50} (Segment): LCD segment drive output.

V_1, V_2, V_3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attaches external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_{C1}, V_{C2}: Do not connect any wire.

V_{REF1}: Connect this pin to V1 pin.

V_{REF2}: Hold V_{DD} level.

V_{DD}: Positive power supply.

V_{SS}: Negative power supply.

HD61605 Pin Function

READY (Ready): During setting data in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two types of modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_3 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operations.

(i) Stops oscillation and clock input.
(ii) Stops LCD driver.
(iii) Stops writing data into display RAM.

D_0-D_3: Data input pin from which 4-bit × 4 -byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{63} (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attaches external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_3 (LCD Voltage): Power supply input for LCD drive.

Voltage between V_{DD} and V_3 is used as drive voltage.

V_{SS}: Negative power supply.

V_{DD}: Positive power supply.

Table 1. HD61604 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0-D_7	8	Input	MCU
SYNC	1	Input	MCU
COM_0-COM_3	4	Output	LCD
SEG_0-SEG_{50}	51	Output	LCD
V_1, V_2, V_3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
V_{C1}, V_{C2}	2	Output	
V_{REF1}	1	Input	V_1
V_{REF2}	1	Input	V_{DD}
V_{DD}	1	Power supply	
V_{SS}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2. HD61605 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0-D_3	4	Input	MCU
SYNC	1	Input	MCU
COM_{01}	Output	LCD	
SEG_0-SEG_{63}	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V_3	1	Input	Power supply
V_{SS}	1	Power supply	
V_{DD}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to the 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

Reading Data from HD61604 Display RAM

A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

(1) **Static Drive:** In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 4).

(2) **1/2 Duty Drive:** In the 1/2 duty drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 5).

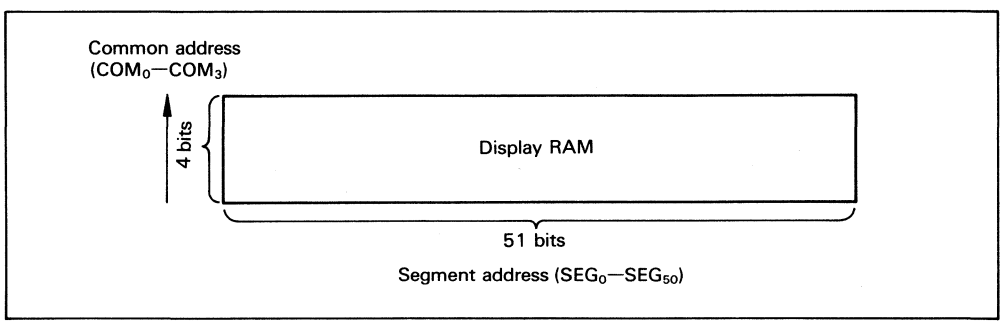


Figure 3. Display RAM (HD61604)

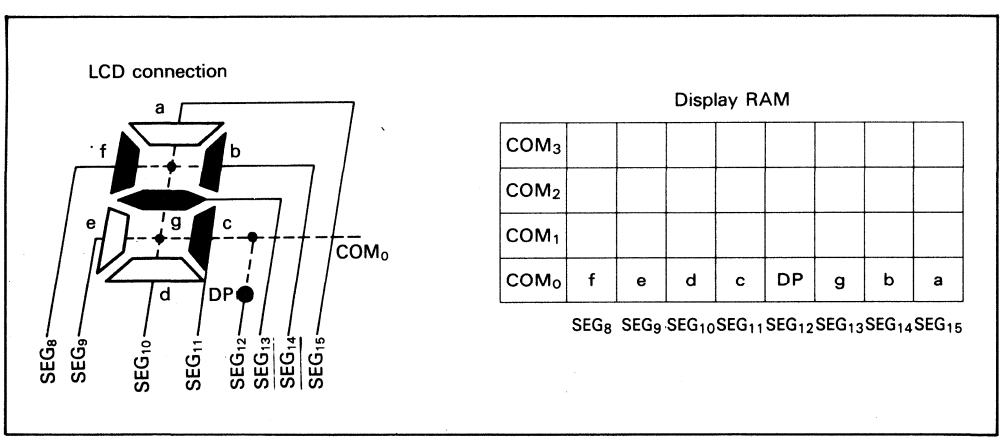


Figure 4. Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

(3) **1/3 Duty Drive:** In the 1/3 duty drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed. "y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "y"(figure 6).

(4) **1/4 Duty Drive:** In the 1/4 duty drive, all the columns of COM_0 to COM_3 are displayed (figure 7).

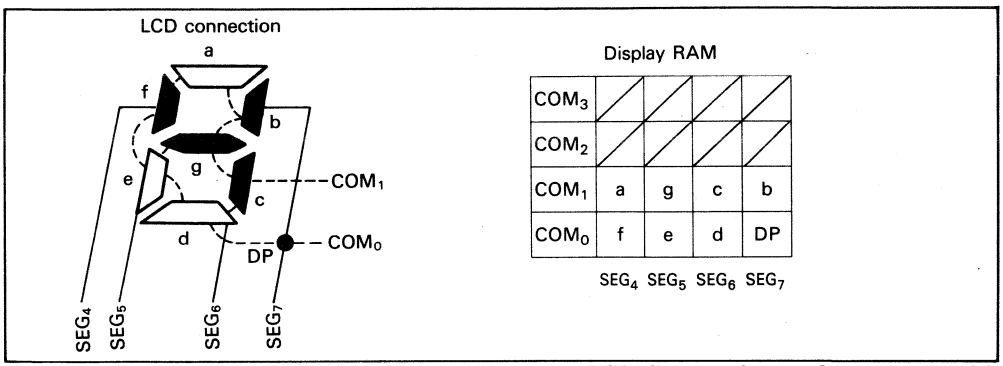


Figure 5. Example of Correspondence between LCD Connection and Display RAM (1/2 Duty, HD61604)

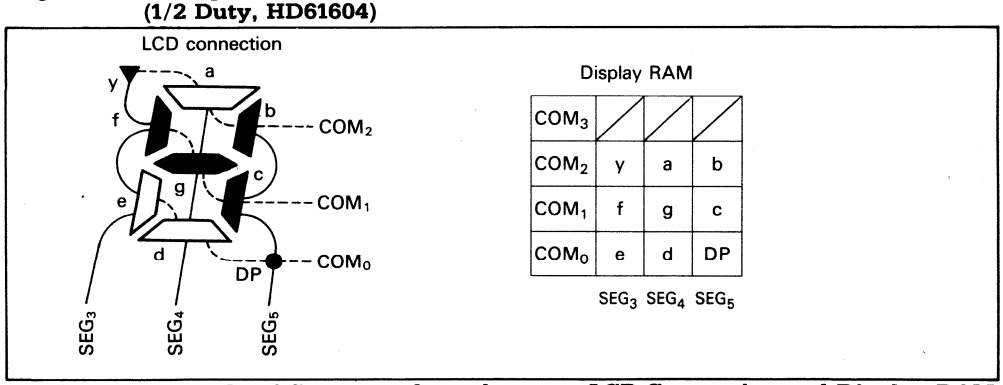


Figure 6. Example of Correspondence between LCD Connection and Display RAM (1/3 Duty, HD61604)

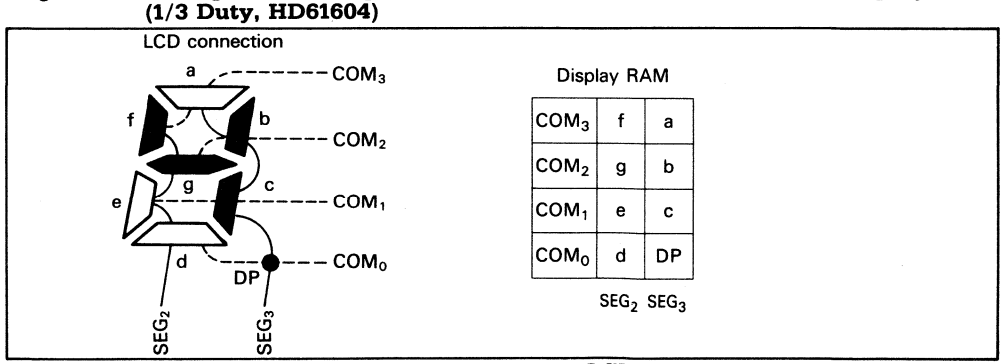


Figure 7. Example of Correspondence between LCD Connection and Display RAM (1/4 Duty, HD61604)

Writing Data into HD61604 Display RAM

Data is written into the display RAM in the following five methods:

(1) **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.

(2) **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

(3) **1/2 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty drive.

(4) **1/3 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty drive.

(5) **1/4 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty drive methods. The digits are allocated as shown in figure 8.

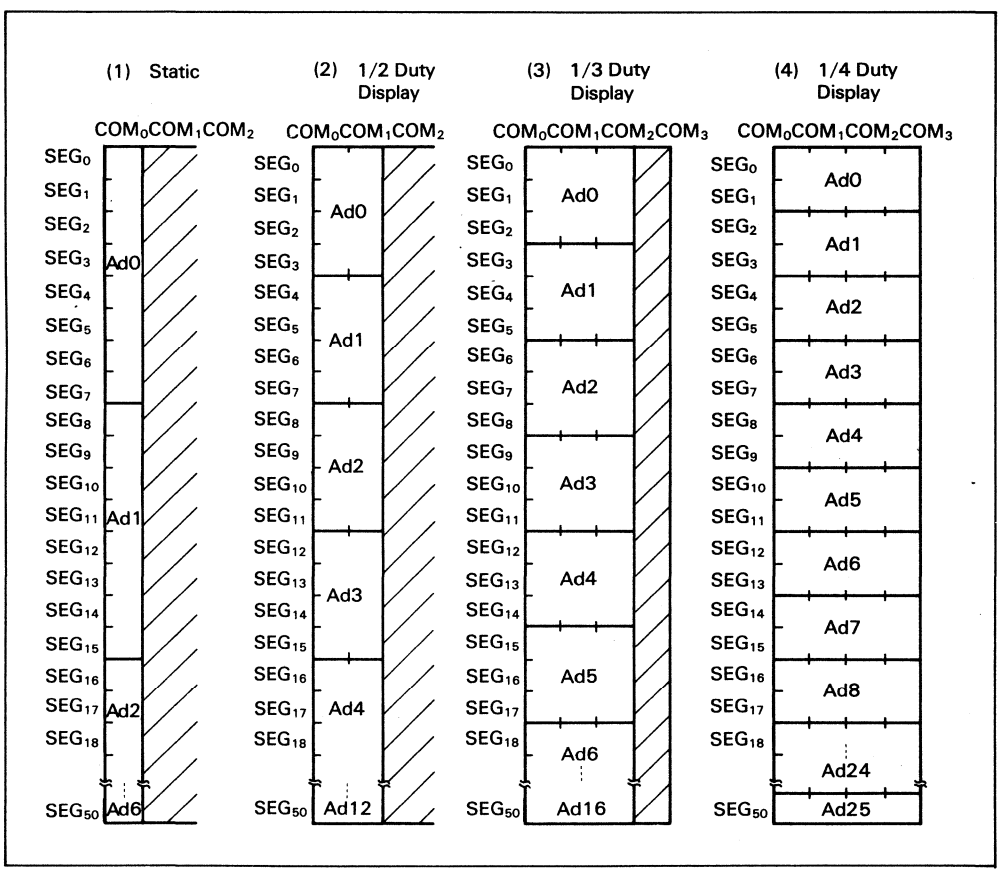


Figure 8. Allocation of Digit (HD61604)

As the data can be transferred on a digit basis from a microcomputer, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty, or Ad25 of 1/4 duty, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in figure 10. Display data is stored in the RAM and output to the segment output pin.

(1) Static Display

	COM_0
SEG_8	Bit 7
SEG_{8n+1}	6
SEG_{8n+2}	5
SEG_{8n+3}	4
SEG_{8n+4}	3
SEG_{8n+5}	2
SEG_{8n+6}	1
SEG_{8n+7}	Bit 0

(2) 1/2 Duty Display

	COM_0	COM_1
SEG_{4n}	Bit 7	6
SEG_{4n+1}	5	4
SEG_{4n+2}	3	2
SEG_{4n+3}	1	Bit 0

(3) 1/3 Duty Display

	COM_0	COM_1	COM_2
SEG_{3n}	Bit 7	6	
SEG_{3n+1}	5	4	3
SEG_{3n+2}	2	1	Bit 0

(4) 1/4 Duty Display

	COM_0	COM_1	COM_2	COM_3
SEG_{2n}	Bit 7	6	5	4
SEG_{2n+1}	3	2	1	Bit 0

Figure 9. Bit Assignment in an Adn (HD61604)

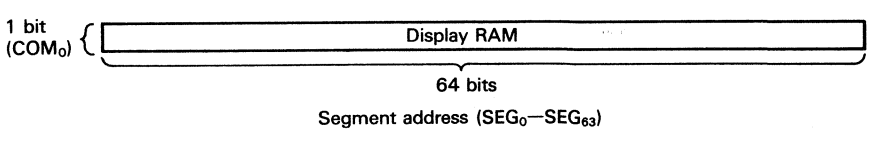


Figure 10. Display RAM (HD61605)

Reading Data from HD61605 Display RAM

Each bit of the display RAM corresponds to each LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM .

Writing Data into HD61605 Display RAM

Data is written into the display RAM in the following two methods:

(1) **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.

(2) **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microcomputer, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

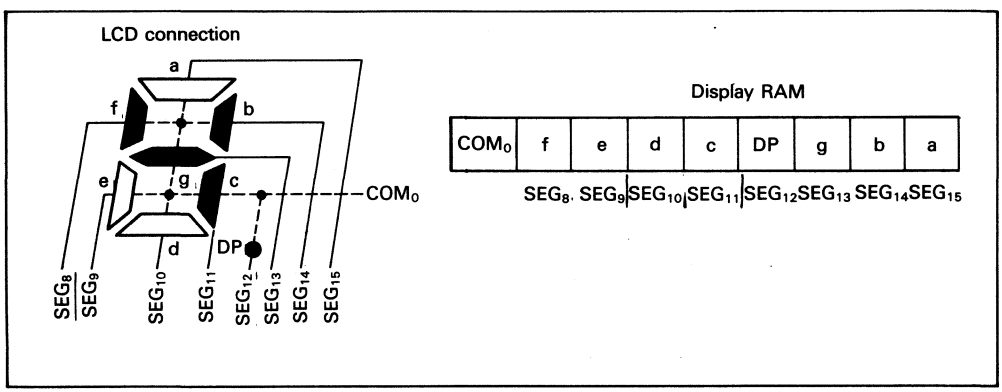


Figure 11. Example of Correspondence between LCD Connection and Display RAM (HD61605)

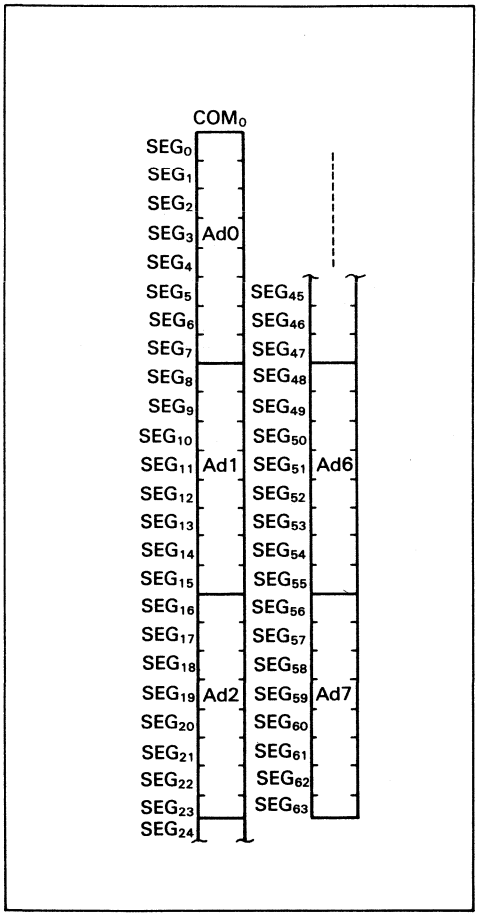


Figure 12. Allocation of Digit (HD61605)

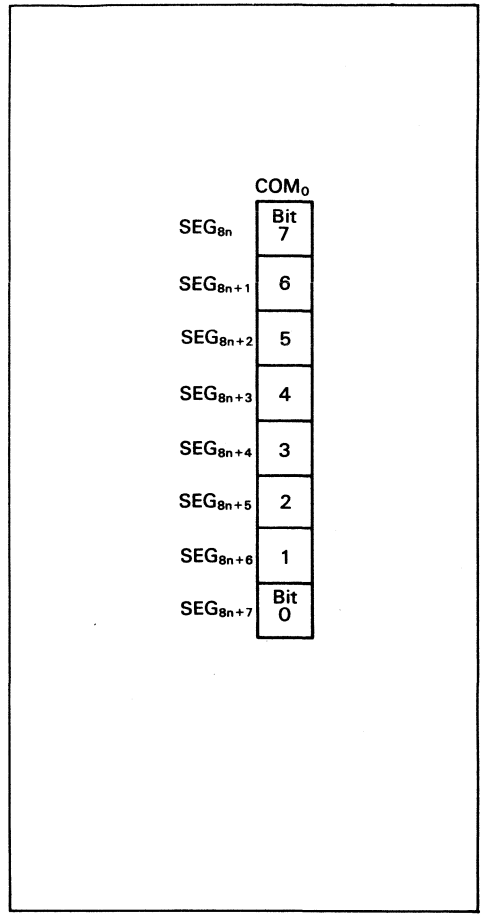


Figure 13. Bit Assignment in an Adn (HD 61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

(1) **LCD Drive Mode:** Determines the LCD drive method.

- Static drive mode: LCD is driven statically.
- 1/2 duty drive mode: LCD is driven with 1/2 duty and 1/2 bias.
- 1/3 duty drive mode: LCD is driven with 1/3 duty and 1/3 bias.
- 1/4 duty drive mode: LCD is driven with 1/4 duty and 1/3 bias.

(2) **Data Display Mode:** Determines how to write display data into the data RAM.

- Static display mode: 8-bit data is written into the display RAM according to the digit in the static drive.
- 1/2 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/2 duty drive.
- 1/3 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/3 duty drive.
- 1/4 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/4 duty display drive.

(3) **READY Output Mode:** Determines the READY output timing.

After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 14).
- READY is available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

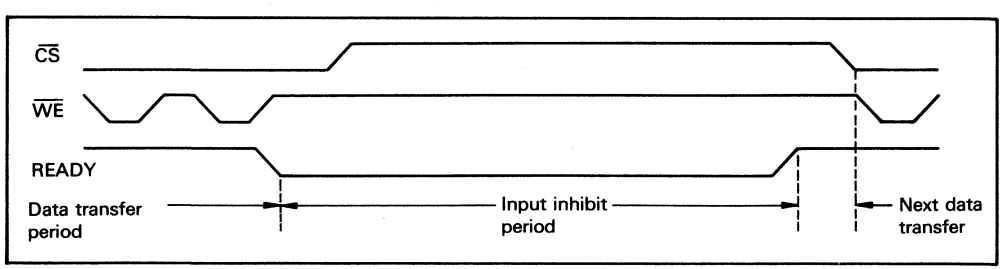


Figure 14. READY Output Timing (When It is Always Available)

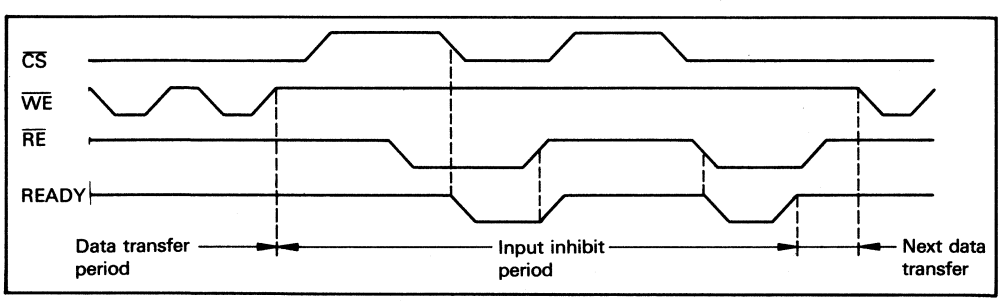


Figure 15. READY Output Timing (When It is Available by $\overline{CS}$ and $\overline{RE}$)

(4) **LCD Off Mode:** In this mode, the HD61604 stops driving LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

HD61605 Operating Modes

The HD61605 has the following operating modes:

(1) **READY Output Mode:** Determines the READY output timing.

After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 16).
- READY is available by $\overline{CS}$ and $\overline{RE}$ (figure 17).

(2) **LCD Off Mode:** In this mode, the HD61605 stops driving LCD and turns it off.

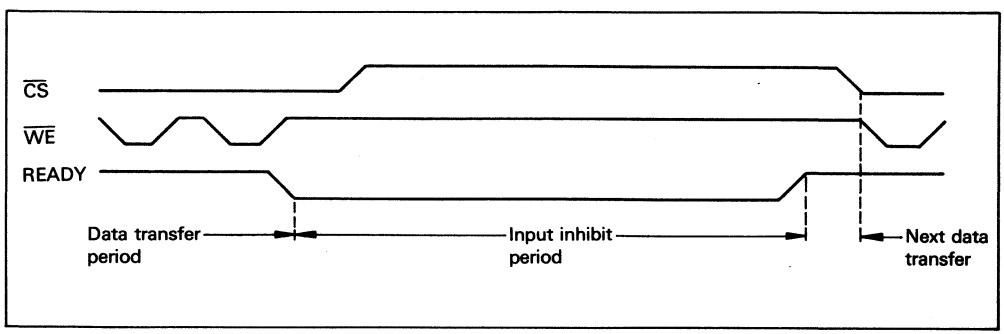


Figure 16. READY Output Timing (When It is Always Available)

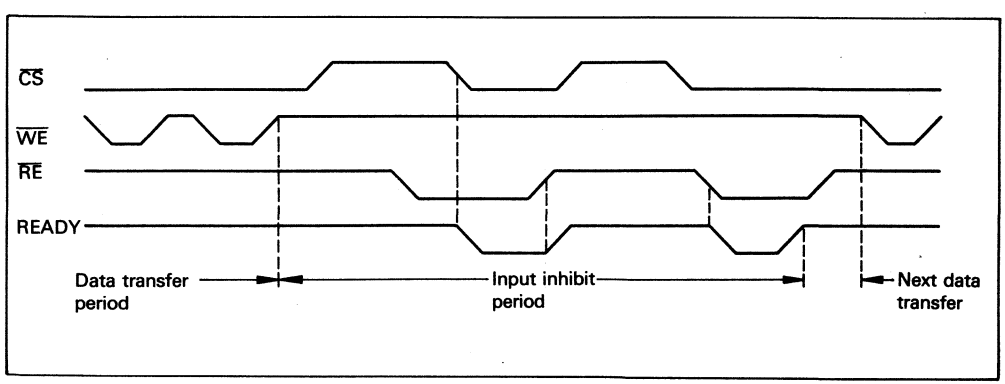


Figure 17. READY Output Timing (When It is Available by $\overline{CS}$ and $\overline{RE}$.)

Input Data Formats

HD61604 Input Data Formats

Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

(1) **Display Data:** Updates display on an 8-segment basis.

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

- Display address: Digit address Adn in accordance with each display mode
- Display data: Pattern data written into the display RAM according to each display mode and the address

(2) **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

- Display data: Data written into 1 bit of the specified display RAM
- COM address: Common address of display RAM
- SEG address: Segment address of display RAM

(3) **Mode Setting Data:**

1st byte

7	6	5	4	3	2	1	0
1	0	×	0	1	READY bit	Drive mode bits	

2nd byte

7	6	5	4	3	2	1	0
×	×	×	×	×	OFF/ON bit	Display mode bits	

- Display mode bits:
  00: Static display mode
  01: 1/2 duty display mode
  10: 1/3 duty display mode
  11: 1/4 duty display mode
- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered.)
  0: LCD on
- Drive mode bits:
  00: Static drive
  01: 1/2 duty drive
  10: 1/3 duty drive
  11: 1/4 duty drive
- READY bit:
  0: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (It is reset to 0 when SYNC is entered.) ···READY bus mode
  1: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$. ···READY port mode

Note: Input the same data to display mode bits and drive mode bits.

(4) **1-Byte Instruction:** The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

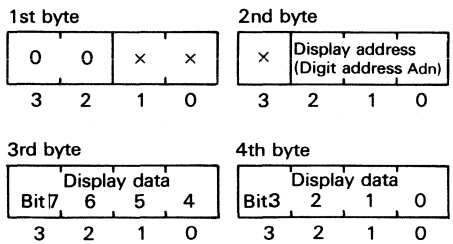
1st byte

7	6	5	4	3	2	1	0
1	1	×	×	×	×	×	×

HD61605 Input Data Formats

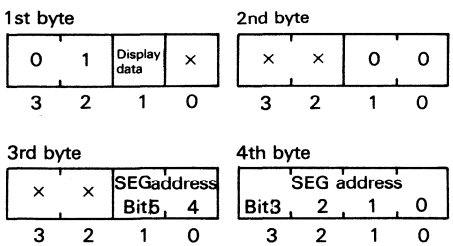
Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

(1) **Display Data:** Updates display on an 8-segment basis.



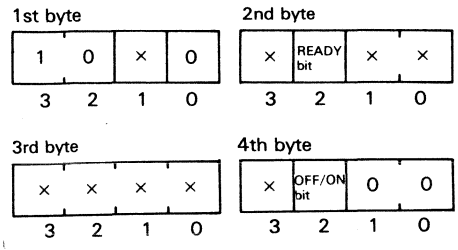
- Display address: Digit address Adn shown in figure 12.
- Display data: Pattern data written into the display RAM as shown in figure 13.

(2) **Bit Manipulation Data:** Updates display on a segment basis.



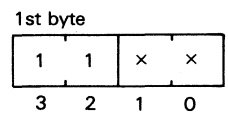
- Display data: Data written into the 1 bit of the specified display RAM.
- SEG address: Segment address of display RAM (segment output).

(3) **Mode Setting Data:**



- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered.)
  0: LCD on
- READY bit:
  0: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (It is reset to 0 when SYNC is entered). ···READY bus mode
  1: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$. ···READY port mode

(4) **1-Byte Instruction:** The first data (4 bits) is ignored when the bit 3 and bit 2 in the data are 1.



How to Input Data

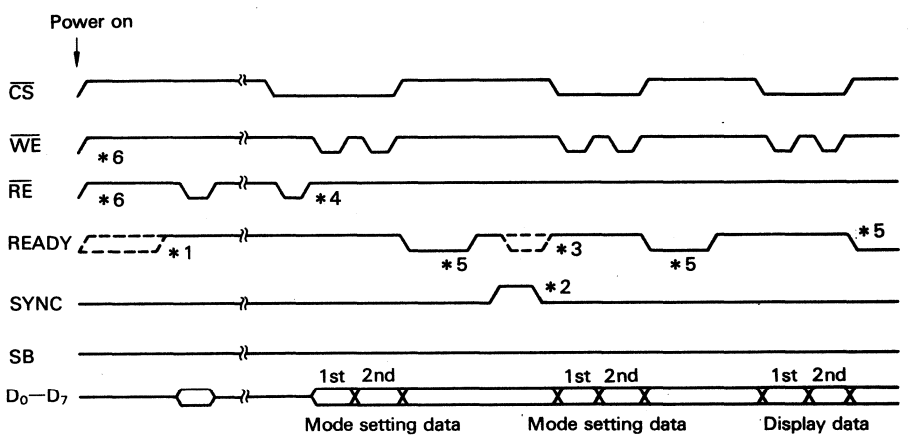
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted because the first 8-bit data is distinguished from the second one depending on the sequence only.

When data transfer is interrupted, or at the power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

(1) Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
(2) Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and figure 18.



*1: READY output is indefinite during 12 clocks after the oscillation starts when power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being appliad to SYNC.
*4: Reset the byte counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 18. Example of Data Transfer Sequence

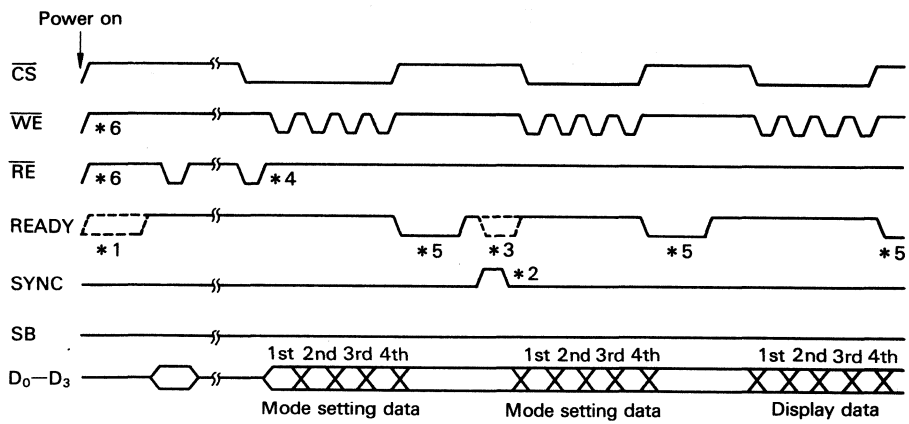
How to Input Data into HD61605

Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other depending on the sequence only.

When data transfer is interrupted, or at the power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

(1) Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes.)
(2) Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$ D_0 to D_3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and figure 19.



*1: READY output is indefinite during 12 clocks after the oscillation starts when power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
*4: Reset the 4-bit data counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 19. Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending on the modes.

(1) READY bus mode (READY bit = 0)

(2) READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605..

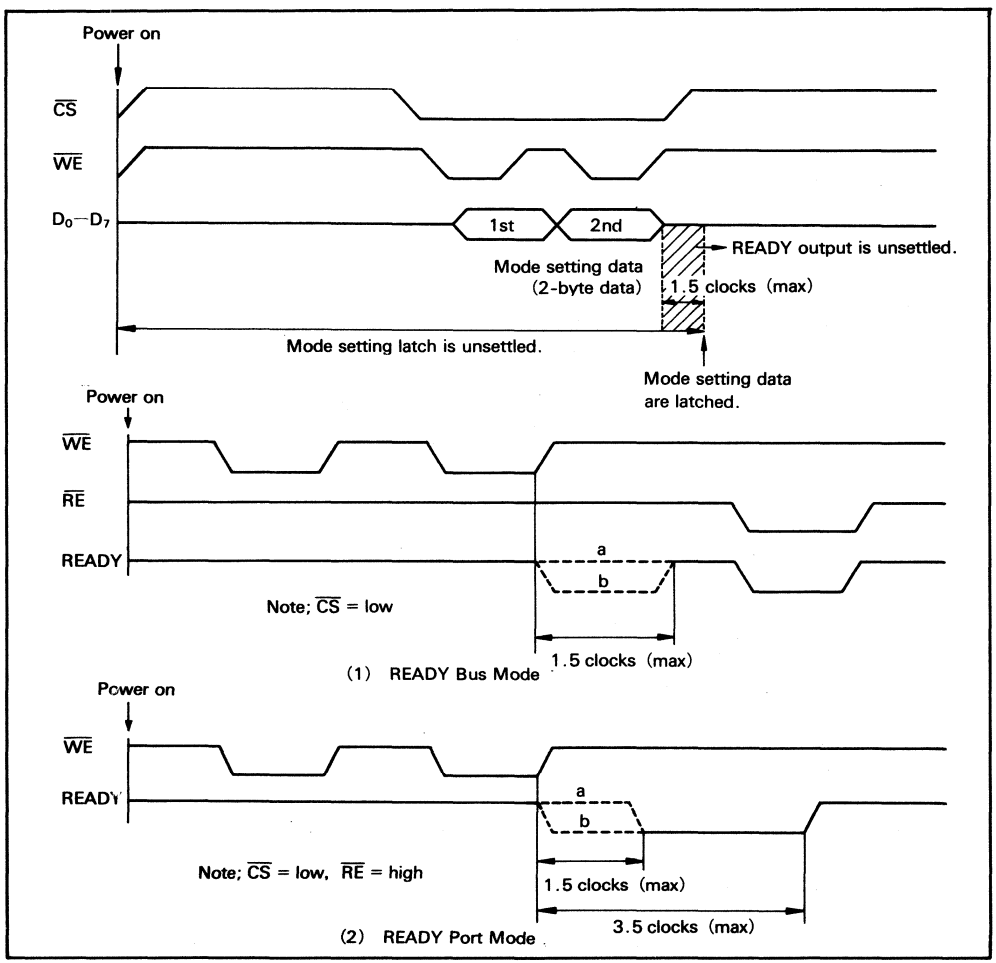


Figure 20. READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

(a) LCD driver is stopped (LCD is off).
(b) Display data and operating mode are held.
(c) The operation is suspended while changing display (= while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
(d) Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi-Chip Operation

When an LCD is driven with two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input causes the change of the mode setting data (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

In the case SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geqq 1\ \mu F$) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages; V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to liquid crystal displays. V_3 always needs to be supplied power regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2−R5 in series between V_{DD} and V_{SS} generates ΔV or V_{LCD} by using this resistance ratio to supply these voltage to pins V_1, V_2, V_3. C2−C4 are the capacitors for smoothing. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

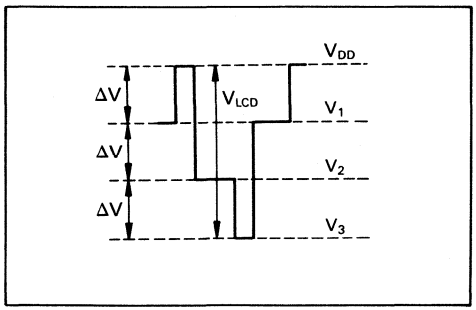
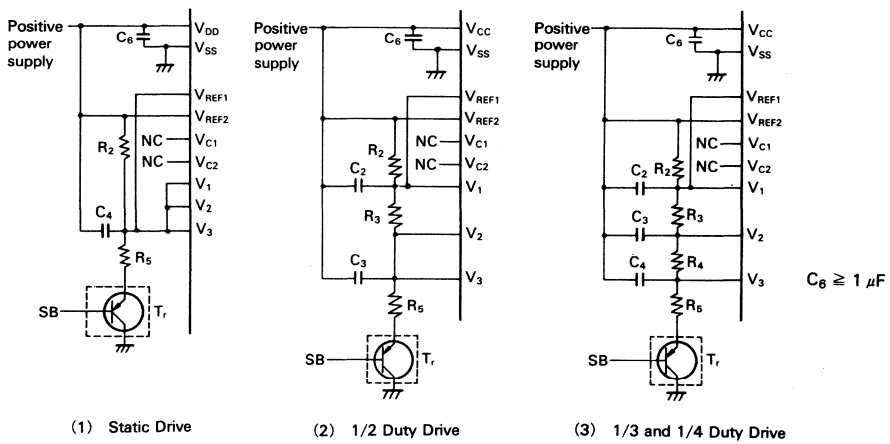


Figure 21. LCD Output Waveform and Output Levels (1/3 Duty, 1/3 Bias)



Note: 1 When standby mode is used, a transistor is required.
2 R2–R5 should be some kΩ~some tens of kΩ, and C2–C4 should be 0.1 μF–0.3 μF.

Figure 22. Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61605)

As shown in figure 23, apply LCD drive voltage from the external power supply.

Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.

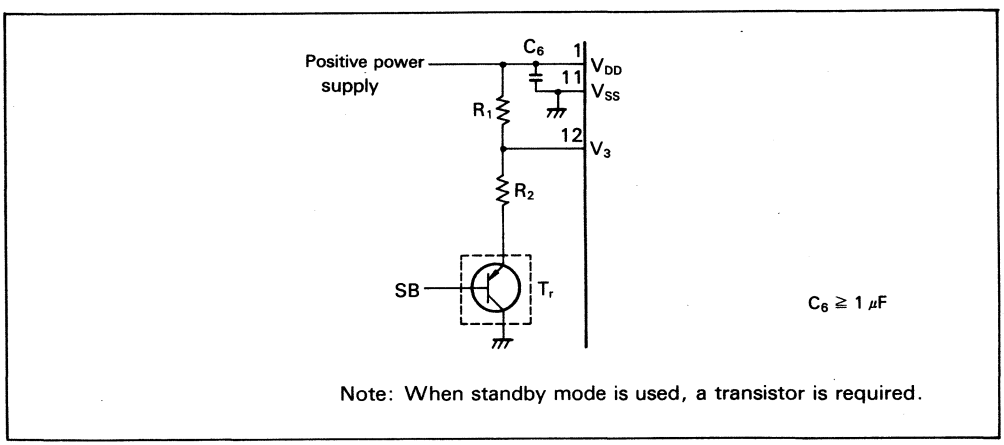


Figure 23. Example of Drive Voltage Generator

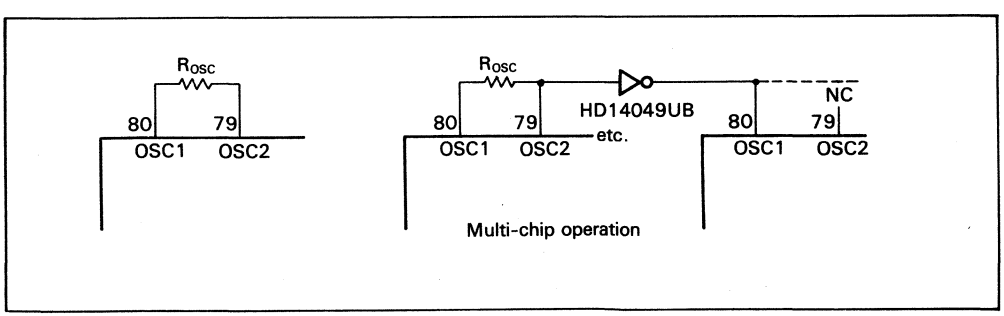


Figure 24. Example of Oscillation Circuit

Applications

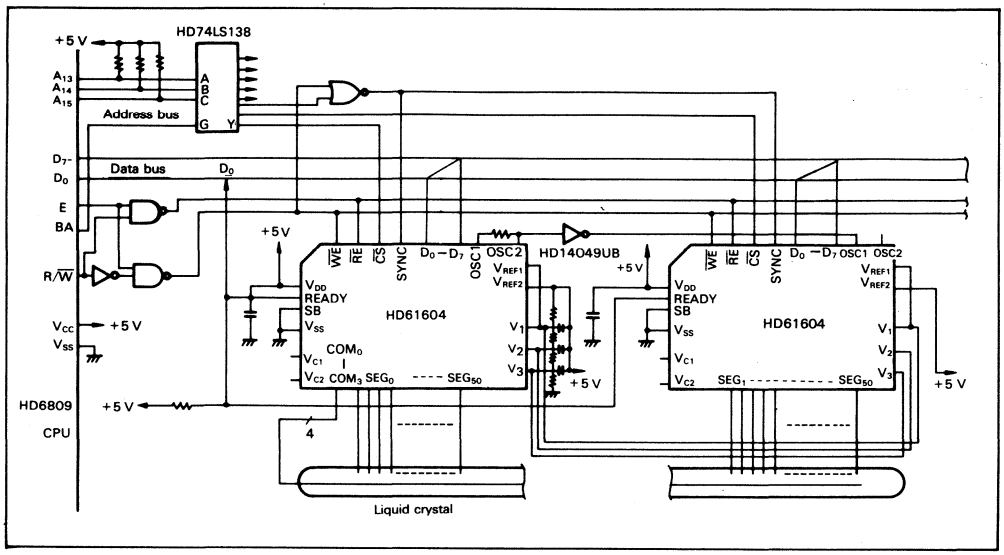


Figure 25. Example (1)

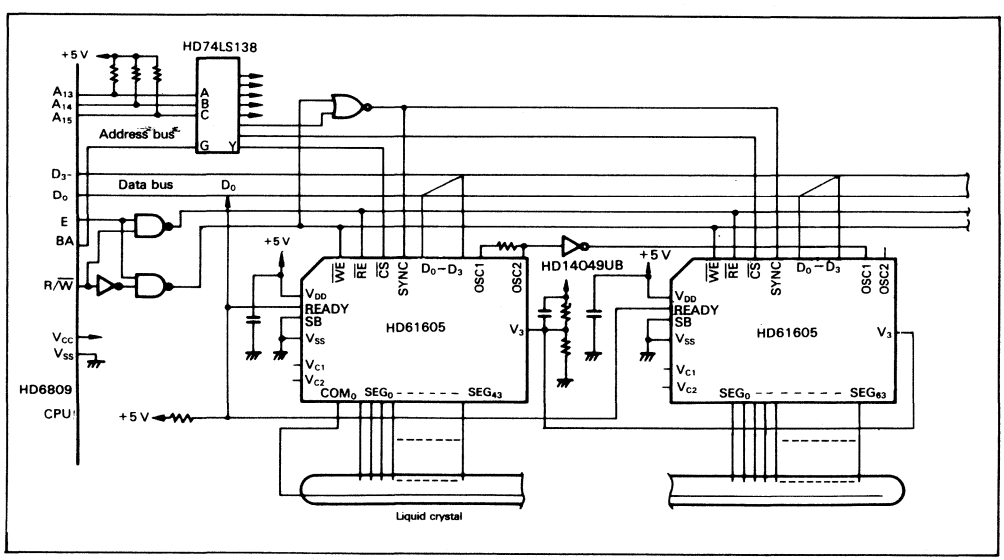


Figure 26. Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	−0.3 to + 7.0	V
Pin voltage *	V_T	−0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

*Value referred to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

Item	Symbol	Limit			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	4.5	–	5.5	V
	V_1, V_2, V_3	0.3	–	V_{DD}	V
Pin voltage*	V_T	0	–	V_{DD}	V
Operating temperature	Topr	−20	–	+75	°C

*Value referred to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta= −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Input high voltage	OSC1	V_{IH1}	0.8V_{DD}	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC1	V_{IL1}	0	–	0.2V_{DD}	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	Pull up the pin to V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL}=0.4 mA
Input leakage current *1	Input pin	I_{IL1}	−1.0		1.0	μA	V_{IN}=0 to V_{DD}
	V_1	I_{IL2}	−20	–	20	μA	V_{IN}=V_{DD} to V_3
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0−COM_3	V_{d1}	–	–	0.3	V	±Id=3 μA for each COM, V_3=V_{DD} to 3 V
	SEG_0−SEG_{50}	V_{d2}	–	–	0.6	V	±Id=3 μA for each SEG, V_3=V_{DD} to 3 V
Current consumption *2		I_{DD}	–	–	100	μA	During display * R_{OSC}=360 kΩ
		I_{DD}	–	–	5	μA	At standby

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: applied only to HD61604.
*2 Do not connect any wire to the output pins and connect the input pins to V_{DD} or V_{SS}.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC2	f_{OSC}	70	100	130	kHz	R_{OSC} = 360 kΩ
External clock frequency	OSC1	f_{OSC}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	–	–	ns	
		t_H	10	–	–	ns	
		t_{WH}	300	–	–	ns	
		t_{WL}	400	–	–	ns	
		t_{WR}	400	–	–	ns	
		t_{DL}	–	–	1.0	μs	Figure 31
		t_{EN}	400	–	–	ns	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

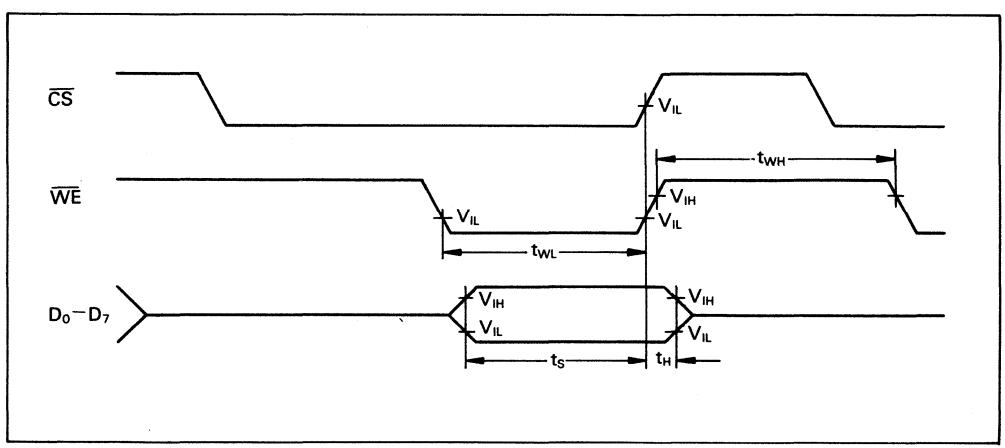


Figure 27. Write Timing ($\overline{RE}$ is fixed high and SYNC low)

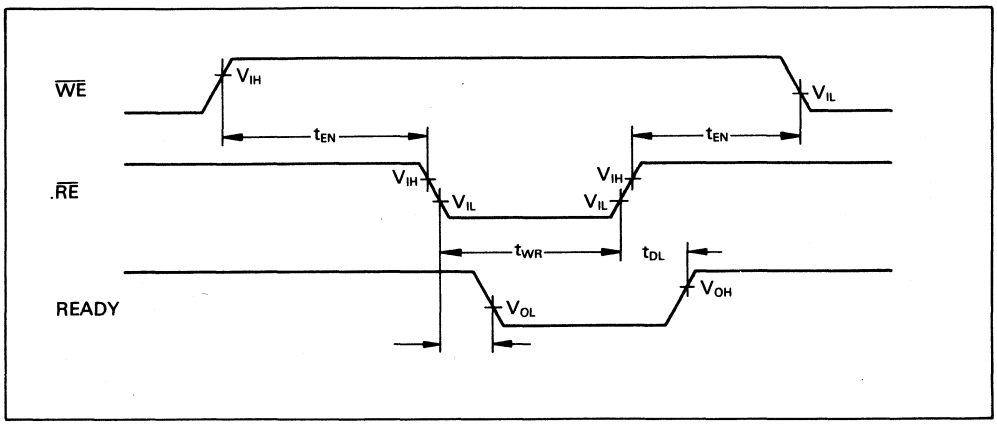


Figure 28. Reset/Read Timing ($\overline{CS}$ and SYNC are fixed low)

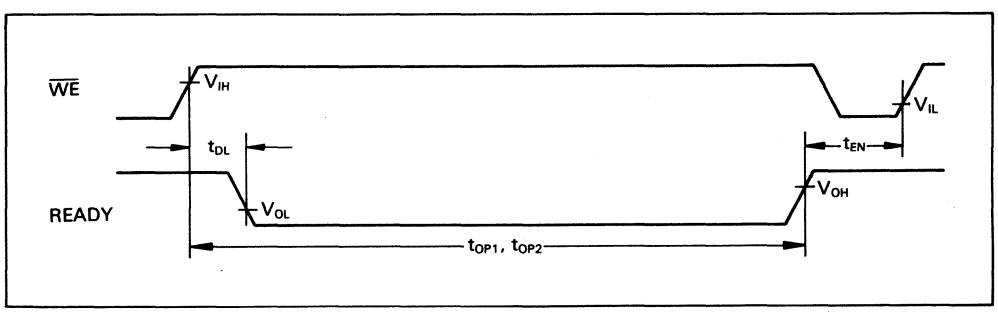


Figure 29. READY Timing (When the READY Output is Always Available)

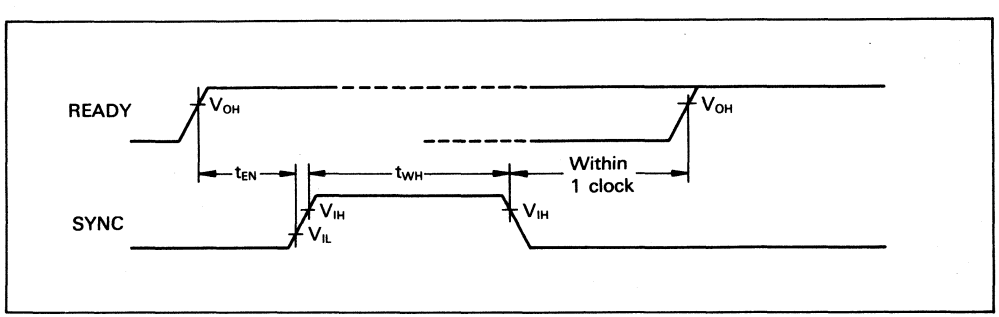


Figure 30. SYNC Timing

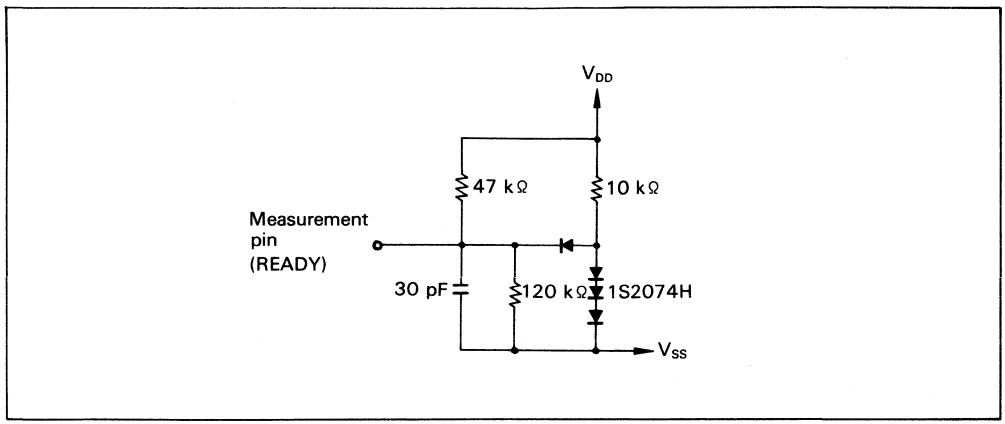
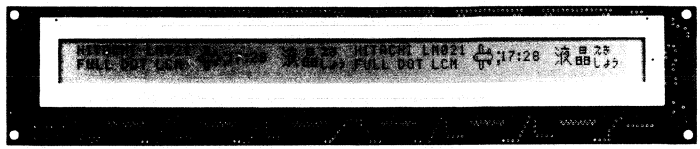


Figure 31. Bus Timing Load Circuit (LS-TTL Load)

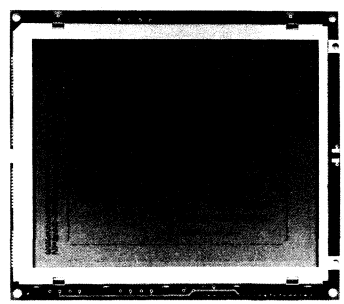
LCD Module
Line up

Graphic Display LCD Module

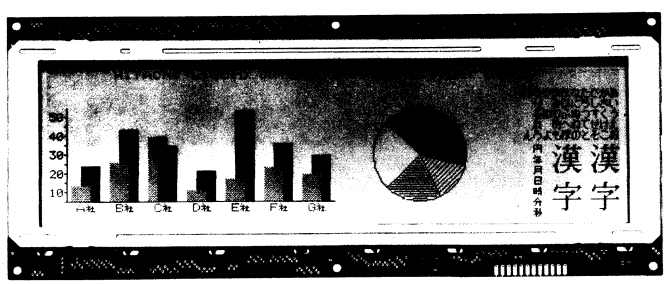


●LM021

●LM221B, LM238B

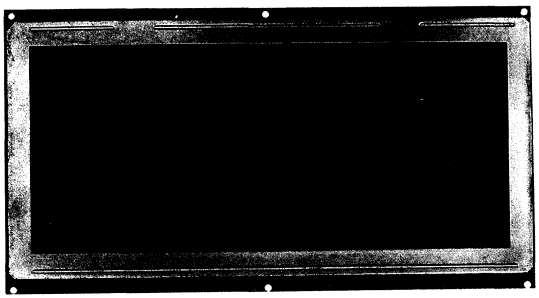


●LM246X

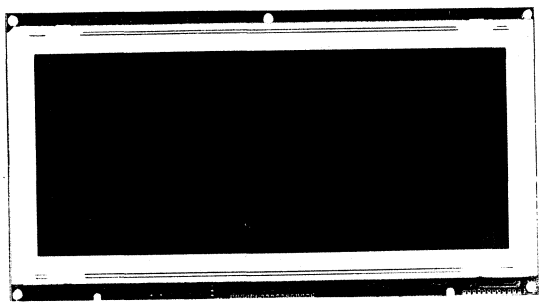


●LM215B, LM224B

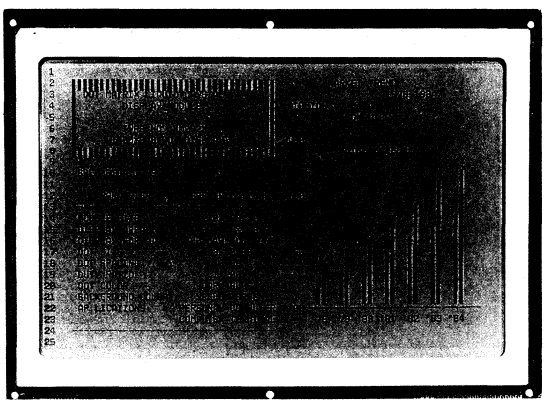
LCD Module Line up



●LM225S, LM225X



●LM250X

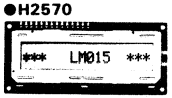


●LM252X

Character Display LCD Module (built in Controller)

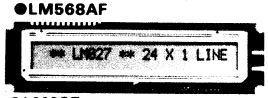
●LM054

●H2570



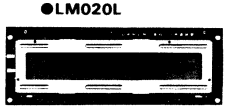
●LM015

●LM568AF



●LM027

●LM020L



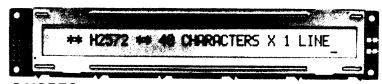
●LM070L

●LM052L

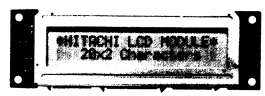
●LM016L

●LM038

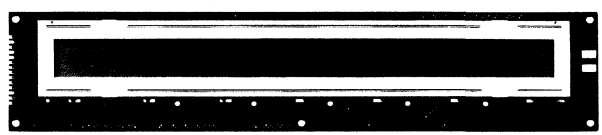
●H2571



●H2572



●LM032



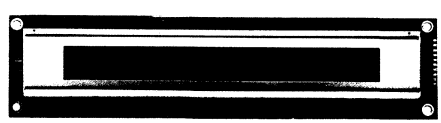
●LM058

●LM017L

●LM018L

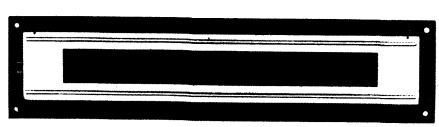
Character Display LCD Module (external Controller)

●H2532A



●H2538A

●H2535



●H2539

LCD Module Line up

Quick Reference

Type			Model	Screen Size w×h	Module Size w×h×t (mm)	Effective Screen Size w×h (mm)	Character Dimensions w×h (mm)	Duty
Graphic Display LCD module			LM021	479×24 (dot)	290×60×13max.	245×19	(0.43×0.55)	1/24
			LM221B	240×128 (dot)	180×120×13.8max.	148×75	(0.50×0.50)	1/64
			LM238B	240×128 (dot)	180×120×14max.	148×75	(0.50×0.50)	1/64
			LM246X†	320×256 (dot)	168×150×13.5max.	142×115	(0.43×0.43)	1/128
			LM215B	480×128 (dot)	270×110×11.5max.	242×69	(0.43×0.43)	1/64
			LM215SB■	480×128 (dot)	270×110×11.5max.	242×69	(0.43×0.43)	1/64
			LM224B	480×128 (dot)	Note 1		(0.43×0.43)	1/64
			LM225S■	640×200 (dot)	270×150×13max.	239×104	(0.32×0.46)	1/100
			LM225X†	640×200 (dot)	270×150×13max.	239×104	(0.32×0.46)	1/100
			LM250X†	640×200 (dot)	270×150×13max.	239×104	(0.32×0.46)	1/200
			LM252X†	640×400 (dot)	270×198×13max.	236×153.6	(0.33×0.33)	1/200
Character Display LCD module	Built in Controller type	1 Line	LM054	8×1 (Char.×Line.)	84×44×13max.	61×15.8	6.45×9.4	1/8
			H2570	16×1 (Char.×Line.)	80×36×12max.	64.5×13.8	3.15×7.9	1/11
			LM015	16×1 (Char.×Line.)	80×36×12max.	64.5×13.8	3.15×5.5	1/8
			LM568AF	16×1 (Char.×Line.)	122×33×12max.	99.0×13.0	4.84×8.06	1/8
			LM020L	16×1 (Char.×Line.)	80×36×12max.	64.5×13.8	3.07×5.73	1/16
			LM070L	20×1 (Char.×Line.)	105×39.0×11max.	84.0×13.0	3.2×5.2	1/8
			LM038	20×1 (Char.×Line.)	182×35.5×13max.	154.0×15.3	6.7×9.4	1/8
			LM027	24×1 (Char.×Line.)	126×36×12max.	100×13.8	3.15×7.9	1/11
			H2571	32×1 (Char.×Line.)	174.5×33×13.4max.	132.5×14	3.15×7.9	1/11
			H2572	40×1 (Char.×Line.)	182×35.5×13max.	154.0×15.3	3.15×7.9	1/11
			LM058	40×1 (Char.×Line.)	290×60×13max.	245.0×19.0	4.82×8.18	1/8
		2 Line	LM052L	16×2 (Char.×Line.)	80×36×12max.	64.5×13.8	2.95×3.8	1/16
			LM016L	16×2 (Char.×Line.)	84×44×12max.	61×15.8	2.95×4.85	1/16
			LM032L	20×2 (Char.×Line.)	116×39×13max.	83×18.6	3.2×4.85	1/16
			LM060L	24×2 (Char.×Line.)	116×39×13max.	83×18.6	2.7×4.85	1/16
			LM017L	32×2 (Char.×Line.)	174.5×33×13.4max.	141.2×16.75	3.45×4.85	1/16
			LM018L	40×2 (Char.×Line.)	182×35.5×13max.	154.0×15.3	3.2×4.85	1/16
	External Controller Type		H2523A	16×1 (Char.×Line.)	84×44×15max.	61×15.8	2.9×5.5	1/8
			H2535	16×2 (Char.×Line.)	84×44×15max.	61×15.8	2.9×4.1	1/16
			H2538A	40×1 (Char.×Line.)	220×50×15max.	163×17	3.15×5.5	1/8
			H2539	40×2 (Char.×Line.)	220×50×15max.	163×17	3.15×4.45	1/16

Notes:
■ :High Contrast
† :High Contrast and wide viewing angle
( ):dot size
1. Display LM224B is half display LM215B.

Recommended Voltage		Power Consumption	Operating	Strage				
V_{DD}-V_{SS} (V)	V_{EE}-V_{SS} (V)	Typ. (mW)	Temperature (C)	Temperature (C)	Weight (g)	Power Supply	LSIs used	Controller
+5	−5	30	0 to +50	−20 to +60	150	Double	HD44100	(HD61830)
+5	−10	130	0 to +40	−20 to +60	210	Double	HD61100/03	(HD61830)
+5	−9	250	0 to +40	−20 to +60	220		HD61100/03	Internal
+5	−20	76	0 to +40	−20 to +60	265		HD61104/105	HD63645F
+5	−10	100	0 to +40	−20 to +60	320		HD61100/03	HD61830
+5	−10	100	0 to +40	−20 to +60	320		+HD61830	
+5	−10	100	0 to +40	−20 to +60	320		HD61100/03	HD61830B
+5	−13.5	400	0 to +50	−20 to +60	450		HD61100/03	HD61830B
+5	−13.5	400	0 to +40	−20 to +60	450		HD61100/03	HD61830B
+5	−21.5	190	0 to +40	−20 to +60	450		HD61104/105	HD63645F
+5	−21.5	240	0 to +40	−20 to +60	540		HD61104/105	HD63645F
+5	−	10	0 to +50	−20 to +70	35	Single		Internal
+5	−	10	0 to +50	−20 to +70	25		HD44780	
+5	−	10	0 to +50	−20 to +70	25		HD44780+	
+5	−	10	0 to +50	−20 to +70	50		HD44100	
+5	−	10	0 to +50	−20 to +70	25		HD44780	
+5	−	10	0 to +50	−20 to +70	40		HD44780+	
+5	−	10	0 to +50	−20 to +70	65		HD44100	
+5	−	10	0 to +50	−20 to +70	40			
+5	−	10	0 to +50	−20 to +70	60			
+5	−	10	0 to +50	−20 to +70	65			
+5	−	10	0 to +50	−20 to +70	150			
+5	−	15	0 to +50	−20 to +70	25	Single	HD44780+	Internal
+5	−	15	0 to +50	−20 to +70	35		HD44100	
+5	−	15	0 to +50	−20 to +70	50			
+5	−	15	0 to +50	−20 to +70	60			
+5	−	15	0 to +50	−20 to +70	60			
+5	−	15	0 to +50	−20 to +70	65			
+5	−5	15	0 to +50	−20 to +70	35	Double	HD44100	HD43160AH
+5	−5	10	0 to +50	−20 to +70	25			
+5	−5	10	0 to +50	−20 to +70	100			
+5	−5	10	0 to +50	−20 to +70	100			

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